

Slice Test Results of the ATLAS Barrel Muon Level-1 Trigger

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Abstract

The muon spectrometer of the ATLAS experiment makes use of the Resistive Plate Chambers detectors for particle tracking in the barrel region. The level-1 muon trigger system has to measure and discriminate muon transverse momentum, perform a fast and coarse tracking of the muon candidates, associate them to the bunch crossing corresponding to the event of interest, measure the second coordinate in the non-bending projection. The on-detector electronics first collects front-end signals coming from the two inner RPC stations on the low- p_T PAD boards, each one covering a region of $\Delta\eta \times \Delta\phi = 0.2 \times 0.2$, and hosting four Coincidence Matrix ASICs. Each CMA performs the low- p_T trigger algorithm and data readout on a region of $\Delta\eta \times \Delta\phi = 0.2 \times 0.1$. Data coming from the four CMAs are assembled by the low- p_T PAD logic. Each low- p_T PAD board sends data to the corresponding high- p_T PAD boards, located on the outer RPC station. Four CMA on each board make use of the low- p_T trigger result and of the front-end signals coming from the outer RPC stations to perform the high- p_T algorithm. The overall results are assembled by the high- p_T PAD logic and sent via optical fibre to the off-detector electronics. Each optical receiver board collects data from six or seven fibres, covering a region of $\Delta\eta \times \Delta\phi = 1.0 \times 0.1$. Trigger data are sent to the local Sector Logic, which elaborates trigger data and sends them to the Muon Central Trigger Processor Interface via dedicated copper links. Readout data are sent to the Read-Out Drivers Boards.

Laboratory and muon beam test on the readout and trigger chains are presented.

I. INTRODUCTION

The barrel muon trigger system uses Resistive Plate Chambers (RPC) as trigger detector, and Multi Drift Tube (MDT) detectors for particle track precise measurement. The 3-D view of the ATLAS experiment and a section view of it are shown in Figure 1 and Figure 2. As shown in the figures, RPC chambers are mounted on top and on bottom of the middle MDT stations, and on only one side of the outer MDT

stations. Hence a system of three RPC concentric layers is used. One RPC detector is composed of two gas gaps, each one having two orthogonal layers of eta and phi readout strips, so that each of the three RPC stations has two eta and two phi strip layers. The trigger system main functionality is to identify the BC corresponding to the event of interest, discriminate the muon transverse momentum p_T and perform a fast and coarse particle tracking for higher level trigger processors.

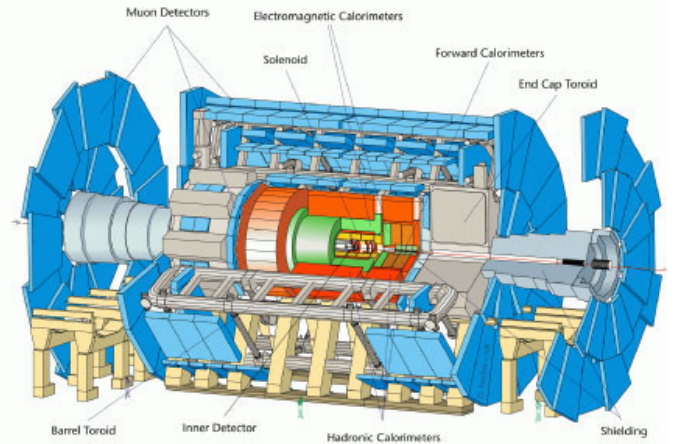


Figure 1: ATLAS 3-D view. Barrel muon detectors are located in the barrel toroid region.

The trigger algorithm makes use of the three RPC stations to perform the trigger functionality, and is divided in a low p_T trigger (5.5 GeV/c) and high p_T trigger (10 GeV/c). If a hit is found on a RPC strip layer in the pivot middle station (see Figure 3), then the same hit is searched in the inner RPC station, within a programmable window whose centre and width define the muon transverse momentum cut (the wider the window, the lower the p_T cut). If the hit passes the low p_T trigger logic, then the high p_T algorithm can be applied, using the outer RPC station for hit detection. Three programmable p_T thresholds can be applied simultaneously, and to cope with background noise, a 1/4, 2/4, 3/4, 4/4 majority logic can be

used. The algorithm is performed in both eta and phi, separately.

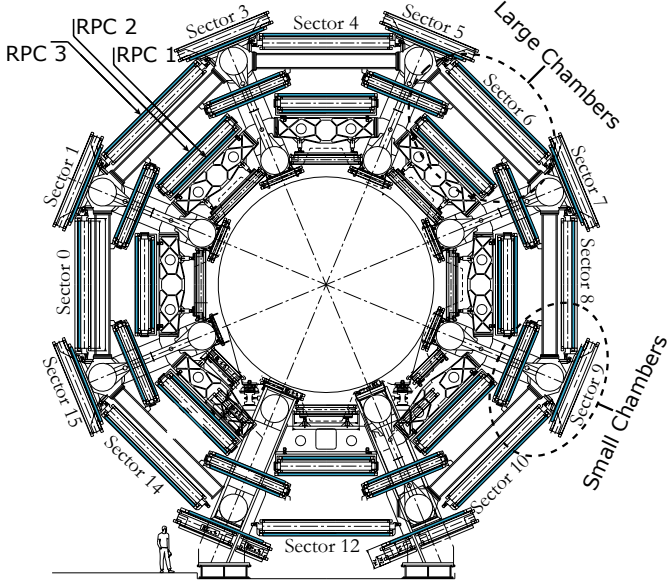


Figure 2: ATLAS barrel muon spectrometer section view. Three concentric RPC stations are located on the middle and outer MDT stations.

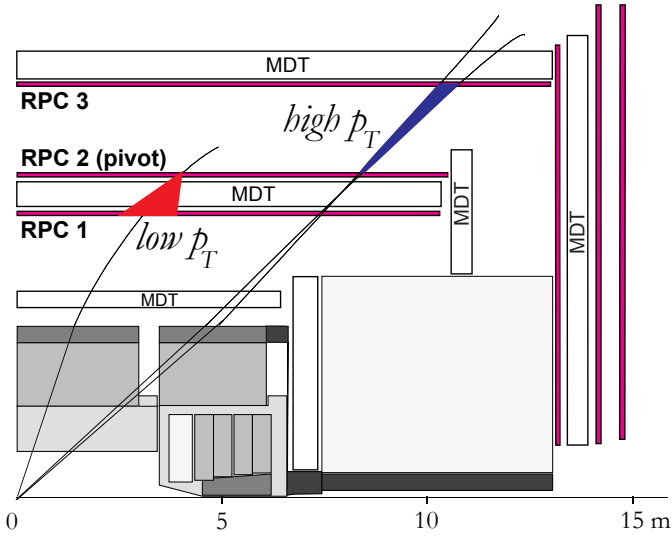


Figure 3: Barrel level-1 muon trigger scheme. Middle RPC station is used as the pivot one, while the inner and outer RPC stations are used as the confirmation planes.

Figure 5 shows the trigger slice implementation. Since trigger windows of two adjacent trigger chambers can partially overlap, inner and outer RPC stations front-end signals have to be consequently fan-out before being sent to the PAD logic. The splitter boxes, which are mounted on top of the RPC chambers, contain the fan-out logic, receive the single-ended RPC front-end signals, and provide LVDS outputs to be sent to the PAD boxes. PAD boxes, again mounted on the trigger chambers, contain the trigger logic electronics. Pivot RPC front-end signals and inner RPC splitter box signals go to the low p_T PAD box, hosting four Coincidence Matrix ASICs

(CMA). Each CMA is capable to receive 32×64 input signals. Two eta and two phi CMAs receive signals from the four detector planes (2 from pivot and two from inner RPC). The ASIC contains the trigger coincidence logic and chambers readout logic. Its internal working frequency is 320 MHz. Data coming from the four CMAs are collected from the low p_T PAD FPGA, and then sent to the high p_T PAD box. This box is mounted on the outer RPC station, and collects LVDS signals coming from the low p_T PAD and from the outer splitter box. The high p_T logic is very similar to the low p_T one. Data from four CMAs are collected together from the PAD FPGA and then sent to the output via one optical link transmitter. Six or seven optical fibres coming from the PADS belonging to one trigger sector go off-detector to one VME receiver board, which elaborates the collected trigger and readout data, and sends readout information to the Read Out Driver (ROD) board and trigger information to the Muon Central Trigger Processor Interface (MUCTPI).

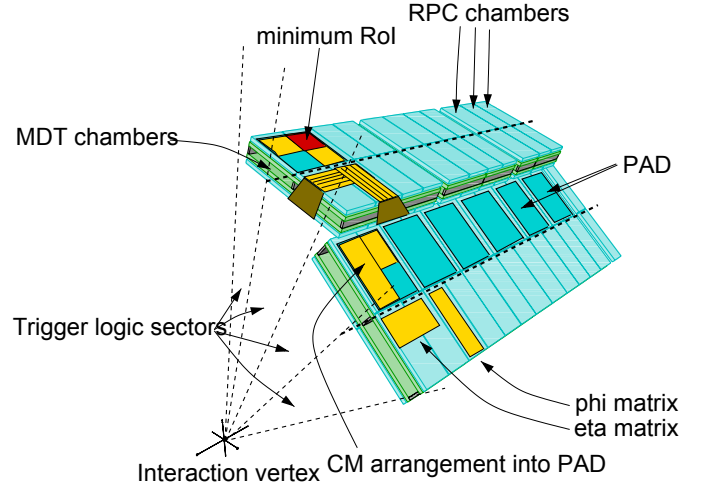


Figure 4: Trigger segmentation. Six or seven RPC chambers form two trigger sectors, each one divided in six or seven PAD regions. Each PAD comprises four ROIs (four CMAs).

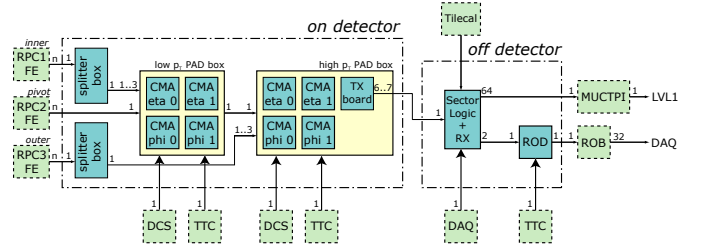


Figure 5: Trigger slice. The slice is composed by two splitter boxes, one low p_T PAD box, one high p_T PAD box, one sector logic/receiver board, one ROD board.

II. LAB TEST

The full slice has been first tested at our lab. Four CMAs were mounted on the low- p_T PAD board, while the high- p_T one did not host any CMA. We developed our own C++ program for controlling via PC the CAN and the VME interfaces. First test was to initialize all components via

CANbus. We were able to initialize the electronics, but a few NACK (not acknowledge) errors from the local I2C interface were observed. This kind of error can be generated if there are noisy conditions on the boards, that can cause spurious transitions on the I2C serial lines. The NACK errors can be easily handled via software, repeating the read/write operation every time an error is found.

A few PRODE (programmable delay ASIC) chip losses of lock were observed at power-up, mainly due to the clock instability on the motherboard during this phase. A power switch chip was so added to both low and high p_T PAD boards, connected to the PRODE power supply lines, and controllable via I2C interface. In this way the PRODE chips can be reset in case of loss of lock.

After being able to initialize our electronics, we started sending L1A signals from TTCvi VME module and reading data from the VME receiver module, in order to check PAD data frame integrity. Time alignment had to be adjusted between signals (CLK, L1A, BCNTR, EVCNTR) going through PRODEs to the CMAs for achieving the right time synchronization between data coming from different CMAs. After having found the proper PRODE initialization settings, CMA data collected from the PAD FPGA were correct, but we still noticed a few bit errors on optical link transmissions. Phase adjustment between optical link clock (DES2 from TTCrx) and PAD FPGA clock (DES1) was so performed to remove the errors. The electronics was finally able to work correctly for days.

The test was then repeated using a hit pattern generator to simulate detector hit signals. More timing adjustments were needed before the system worked correctly. Noise problems were noticed on PAD motherboard, OR and CM mezzanine boards, particularly evident with a high number of input signals switching together.

At the end of the LAB test the slice worked correctly, but noisy signals were observed on the boards, causing a few errors on data frames. Stronger power and ground connections between PAD motherboard and mezzanine boards, as well as special attention on critical signal paths on boards layout were considered for next boards version.

III. BEAM TEST

In April 2003 two BML and two BOL were mounted at CERN H8 test area, on a muon beam. Real ATLAS distance between chambers was respected during installation. The BML had two RPC station (inner and outer), while the BOL had one station, so that the three RPC station trigger system was available to test the trigger slice. Eight splitter boxes were mounted on the chambers, while two PAD boxes, low p_T and high p_T , were mounted respectively on the BML and BOL. Six dummy PAD boxes were using to complete the missing ones in order to have a correct electrical termination for the front-end cables. Front-end cabling was not the corresponding to the final version, in fact the cables used were simple unshielded flat cables, while the final version will have to be plastic shielded, in order to isolate cables and to avoid impedance modification for superimposed cables. The same

electronics used in the LAB test were mounted for this beam test. Splitter boards used in the splitter boxes were pre-production, final version boards. Two CM mezzanine boards, one CM eta and one CM phi, were mounted on the low- p_T PAD box and two on the high- p_T one, so that half RPC chamber was read by each CMA. The optical fiber coming from the high- p_T PAD was connected off-detector to the VME optical receiver board. The same VME crate hosted a ROD board emulator and a few TDC boards used for inner and outer planes readout confirmation. The TDC boards were connected to the RPC front-end via the unused splitter box outputs (inner and outer RPC). The ROD emulator was connected via optical S-Link to the ROS PC.

After power-up, first test was to initialize the electronics. As in the LAB test, a local PC connected to the CANbus was used, in addition with our initialization software. We found that the noise problems coming from cables and from the PAD boards, already seen in the LAB, had now become worse. Still, we were able to initialize the electronics, and after a long work of timing adjustment on the PRODE chips and on the TTCrx board, we were able to initialize correctly the electronics and so to start taking data. Data were taken in stand alone as well as in MDT-RPC combined mode, using the integrated prototype acquisition ROS software. Few errors on the transmitted frame data were observed, due to the noisy conditions. In middle August we received new versions for the CM and OR mezzanines, and for the VME receiver board. The CM and OR board were the final pre-production versions. Moreover the PAD motherboards were manually modified, adding stronger metal connections for power and ground connections, in order to reduce the noise. After developing a new version for the VME receiver board firmware, we were able to test the new boards, which worked properly. Frame data errors significantly reduced.

On September we were so ready to use the slice for the previewed 25 ns run. During this run we were able to test the proper signal synchronization for all boards and between different components, like CMAs and PAD FPGAs. Tests were repeated in stand alone and in MDT-RPC combined mode. Taken data showed that the electronics was working as expected.

Coincidence Matrix ASIC test was an essential goal for this test, since this was the first test in which we were able to feed all CMA inputs from a real detector mounted on a muon beam. For this reason CMA internal logic was tested in all possible configurations, to be convinced that the ASIC was working properly. We tested the input signals masking logic, pipeline depth for front-end signals timing adjustment, input and output signal shaping, de-clustering logic, majority logic (2/4, 3/4 and 4/4), overlap logic, trigger roads, readout window (latency time and window depth), BC capability. During all these tests the ASIC showed a correct functionality.

Using the combined MDT-RPC run data, it was possible to reconstruct particle tracks, using MDT information plus the second coordinate information from the RPC readout data. Hence, detector and trigger efficiency could be calculated,

using information from both MDTs and TDCs. It has to be taken into account that all data were taken using a large hodoscope trigger, which has an intrinsic quite high trigger signal jitter.

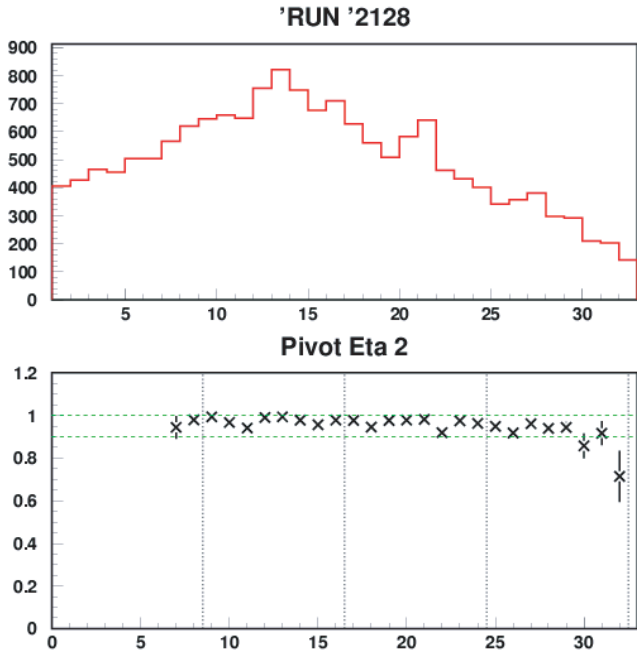


Figure 6: Pivot RPC beam profile and chamber efficiency vs. strip number for 32 RPC strips. The efficiency is calculated using MDT data.

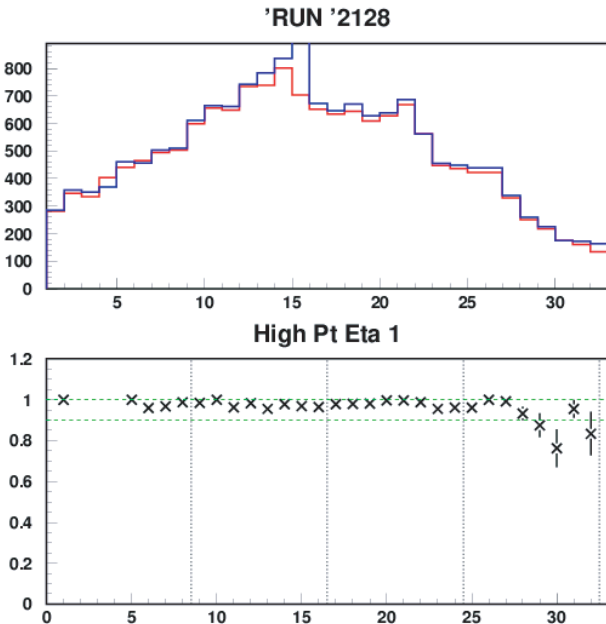


Figure 7: Outer RPC beam profile and chamber efficiency vs. strip number for 32 RPC strips. The blue line represents the beam profile calculated with the TDC data, while the red line represents the beam profile calculated with the CMA readout data.

Figure 6 and Figure 7 show the beam profile plot, calculated with the trigger chambers readout data, and their relative efficiency, calculated with the MDT data. Chamber efficiency is good, and the beam profile calculated with CMA readout data corresponds to the one calculated with TDC data. Trigger efficiency is shown in Figure 8, while the readout system time resolution is shown in Figure 9. It has to be noticed that CM ASIC uses a time interpolator working at 320 MHz (~ 3 ns LSB) to measure time of arrival of RPC hits. The standard deviation for the time resolution is 1.9 ns, corresponding to what was expected.

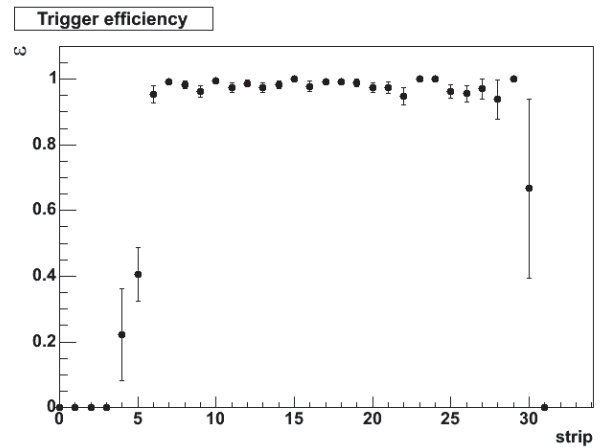


Figure 8: Low p_T trigger eta projection efficiency vs. strip number on pivot plane using MDT reconstructed tracks.

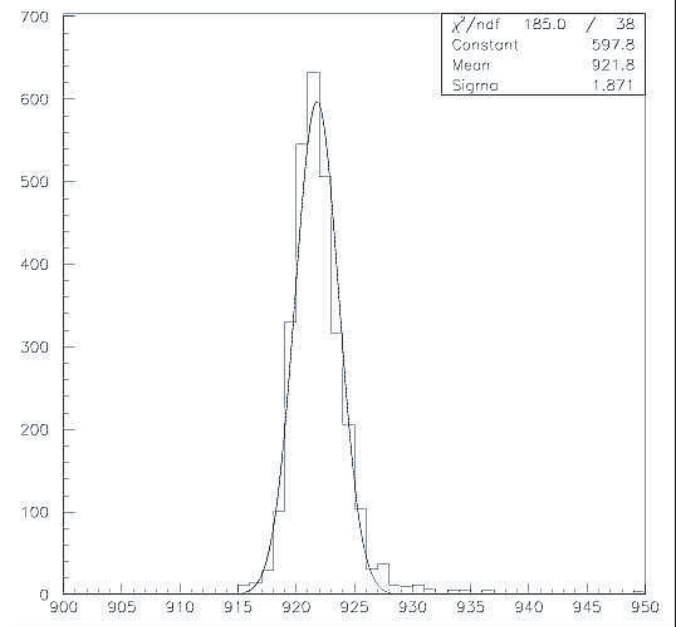


Figure 9: Readout system time resolution. Hit arrival time difference between CM (3 ns LSB) and TDC (1.015 ns LSB). σ is 1.9 ns.

The plot shown in Figure 10 is related to the trigger system Bunch Crossing capability. The CMA has an input programmable pipeline, used to align in time the input signals in steps of 3 ns. All CMA input signals have been moved in steps of 3 ns, in a 50 ns total range. The plot shows the

percentage of right BC association as a function of the programmed input delay. The safe time window is so ~ 12 ns, which corresponds to the expected value.

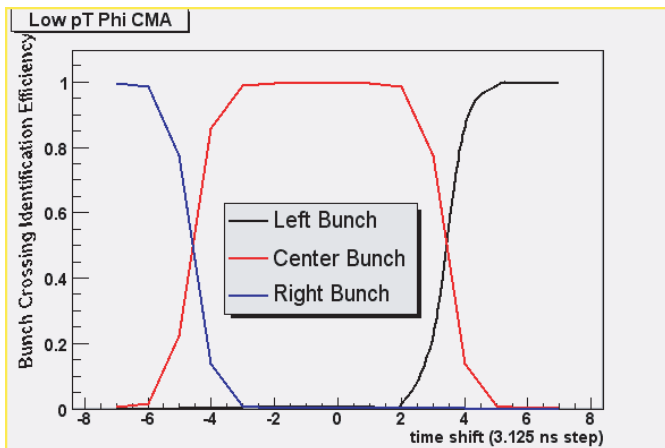


Figure 10: Low p_T trigger bunch counter identification efficiency vs pipeline delay. One time shift corresponds to 3.125 ns.

IV. CONCLUSIONS

Preliminary data analysis shows that the trigger electronics is performing as expected. Beam test data are still under study, and deep data learning is essential to be sure of the correct functionality of the trigger system and electronics. After that, few modifications are under study for the trigger slice. A new CMA version has to be developed, in order to have deeper input pipelines. Those pipelines are needed for aligning in time the CMA input signals. Since the length of the cables connecting the low- p_T PAD box and the high- p_T one is incremented respect to the original request, a deeper input pipeline is required by the high- p_T CMAs in order to be able to align in time the trigger output pattern coming from the low- p_T PAD and the outer RPC front-end hit pattern. Moreover, a new digital filtering will be added for the CMA I2C signals, in order to cope with noisy conditions. A new PAD FPGA firmware has to be developed, adding trigger data formatting and SEU error correction to the actual firmware. A new ELMB firmware has to be developed in order to be able

to initialize the full PAD with one CAN command only, storing in the local memory the initialization values to be written. PAD final version is under development. Stronger power and ground connections between motherboard and mezzanine boards and new layout for critical signal paths have been studied to reduce the noise. The QPLL ASIC will have to be used on the TTCrx mezzanine board, because of the very restrictive clock jitter requests from the GLINK optical transmitter, and for the right CMA timing. The final version of the VME receiver and sector logic board, and the relative FPGA firmware have to be developed.

It is essential that the missing work will be finished before 2004 testbeam, when the full combined ATLAS trigger slice will be tested.

V. REFERENCES

- [1] V. Bocci, G. Chiodi, S. Di Marco, E. Gennari, E. Petrolo, A. Salamon, R. Vari, S. Veneziano, "Prototype Slice of the Level-1 Muon Trigger in the Barrel Region of the ATLAS Experiment", proceedings LECC2001, 2001, pp. 236-239.
- [2] E. Petrolo, A. Salamon, R. Vari, S. Veneziano, "Barrel LVL1 Muon Trigger Coincidence Matrix ASIC User Requirement Document", ATL-COM-DAQ-2000-050.
- [3] E. Petrolo, A. Salamon, R. Vari, S. Veneziano "CMA ASIC Hardware Requirement document", ATL-COM-DAQ-2001-005.
- [4] E. Petrolo, A. Salamon, R. Vari, S. Veneziano, "Readout Requirements in the Level-1 Muon Trigger Coincidence Matrix ASIC", ATL-COM-DAQ-2000-052.
- [5] V. Bocci, A. Di Mattia, E. Petrolo, A. Salamon, R. Vari, S. Veneziano, "The ATLAS LVL1 Muon Barrel Sector Logic demonstrator simulation and implementation", ATL-COM-DAQ-2000-051.
- [6] V. Bocci, E. Petrolo, A. Salamon, R. Vari, S. Veneziano, "The Coincidence Matrix ASIC of the Level-1 Muon Barrel Trigger of the ATLAS Experiment", Transaction on Nuclear Science, Aug 2003.