Local Trigger Electronics for the CMS Drift Tubes Muon detector

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Abstract

In the CMS detector in preparation for the CERN LHC collider, the Drift Tubes Muon Chambers are equipped with mini-crates hosting custom electronics for fast data processing and local trigger generation.

In particular the Trigger Server of a DTC consists of Track Sorter Slave ASICs and a Track Sorter Master system. The trigger electronics boards are in production, to be ready for the muon detector installation in the CMS barrel starting at the end of 2003.

In this work, the performance of the Trigger Server will be discussed, on the basis both of high-statistics tests with predefined patterns and of test beam data collected at CERN, where a DTC was exposed to a muon beam having an LHC-like bunch structure. Finally, some system performance expectations, concerning radiation tolerance and signal transmission issues during LHC running, will be also discussed.

I. System Overview

The Level 1 trigger electronics of a Muon Barrel Drift Tube chamber (DTC) [1] of the CMS detector constitutes a synchronous pipelined system partitioned in several processing stages, organized in a logical tree structure and implemented on custom devices. It can be divided in two well-separated systems: the Local (DTBX) trigger and the Regional trigger.

The DTBX has to single out muon track segment within every DTC, while the Regional system combines information coming from several DTCs, in order to reconstruct tracks in the CMS barrel region, also providing a measurement of the muon momentum in the transverse plane with respect to the beam direction (P_t).

The DTBX electronics is lodged into mini-crates directly mounted on the chambers; its output is sent to the Sector Collector, the first device of the Regional trigger, which is located in a VME crate placed on the balconies surrounding the detector. Then the Sector Collector transmits data to the shielded underground control room, where the Regional trigger devices are.

An overview of the DTBX electronics is presented in Figure 1. The system is partitioned in several Trigger Boards (TRB, from 4 to 6, depending on DTC size) and a Server Board (SB). Each TRB contains 37 ASICs:

- 32 BTI (Bunch and Track Identifier): a BTI finds tracks in a portion of one of the two super-layers (SL) of the DTC in the R-Phi plane, by searching at least three aligned hits out the four layers of drift tubes which compose each SL; it performs bunch crossing (BX) identification and calculates track impact parameters (angle, position);
- 4 TRACO (Track Correlator): a TRACO associates tracks belonging to the two different SL (if they can be correlated); it associates quality information (i.e. number of layers used by BTIs, number of SL used by TRACO);
- 1 TSS (Track Sorter Slave): it selects the best two tracks (smaller incidence angle (higher P_t) and best quality) in a portion of the DTC.

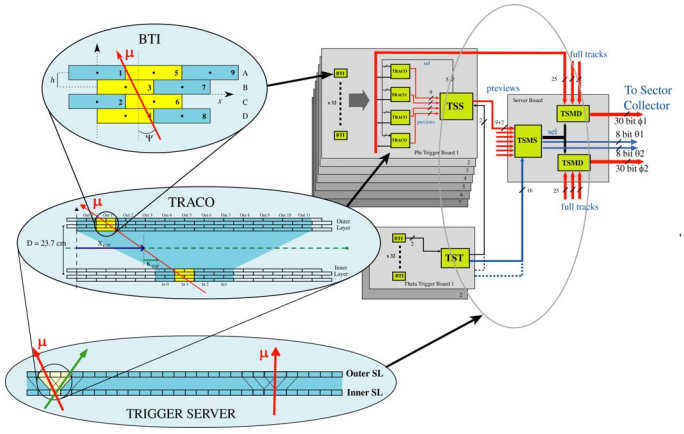

Figure 1: DTC local trigger electronics overview

The SB hosts the Track Sorter Master (TSM) system, which selects the two best tracks in the full DTC and delivers them to the Regional trigger. The TSM was implemented with three FPGAs with antifuse technology. LVDS commercial

devices are used to transmit the TSM output serially at high frequency (480 MHz), through two copper cables.

TSS and TSM form the system called Trigger Server (TS). In sections II and III we will illustrate more in detail the hardware implementation of devices composing the TS, with main focus on the test strategies and production plans. Then, in section VI, some preliminary results of an integrated test of the full DTBX electronics will be shown.

II. TSS – Test and Production

The TSS ASIC chip and the test jig developed for checking prototypes are described in ref. [2].

TSS selects the best two tracks in a portion of the DTC. It receives data from 4 TRACOs, hosted in the same TRB, and sends its output to the SB. The TSS has been implemented in a CMOS 0.5 µm Alcatel technology ASIC. The setup used to test the chips (Figure 2) consists in a board, which hosts a socket for lodging and easily substituting the device under test, which can be inserted, by using appropriate socket strips, on a Pattern Unit [3], a high-throughput VME board, which performs input patterns injection and output signals read-out.

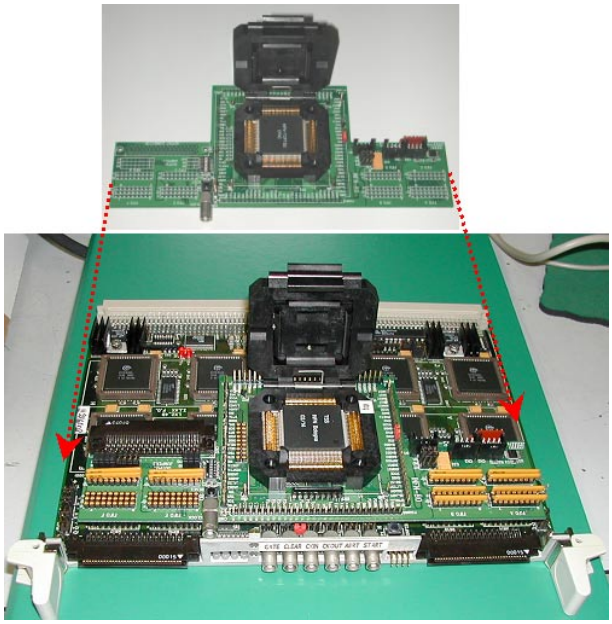

Figure 2: setup for TSS tests: the TSS host board and the connection to the Pattern Unit are shown.

A software application running under Windows 2000 was developed, in a Visual C++ environment. It was able to control the whole test requirements, such as pattern generation, output validation by comparison with a TSS emulator, chip monitoring and configuring. The software also controls external clock generator and power supply (through GPIB protocol), allowing tests in different working conditions.

The full TSS production sample was screened, in order to select for the TRB production only those devices (spares included), working in full accordance with the local trigger electronics requirements.

The system was able to perform a complete test of a TSS, by checking:

- the sorting algorithm on 8 different working configurations (10^5 pattern per configuration @ 60 Kevent / s);
- the performances at different clock frequency and supply voltages;
- internal ASCI bonding connections with JTAG boundary scan;
- monitoring functionalities and control logic;
- the current drawn during the test.

At the end all information concerning each TSS were automatically stored into a mySQL database. A complete test takes about 2 minutes per chip, including time needed by the operator to substitute the chip.

The amount of 1200 successfully tested TSS has been reached with a yield of 93%.

III. TSM – Test and Production

The TSM system [4] located on the SB has been implemented with 3 ACTEL A54SX32 FPGAs with antifuse technology (pASIC) [5], with a partial redundant architecture.

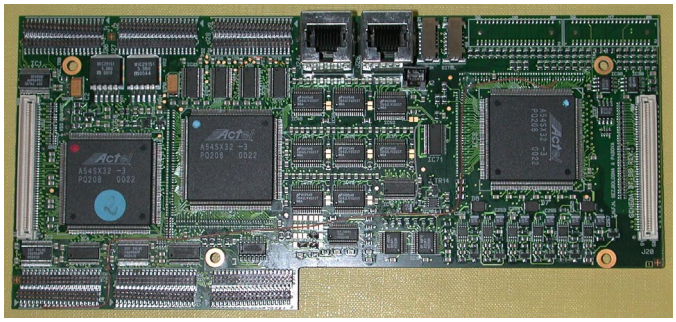

Figure 3: Final version of the SB hosting the TSM system. The larger chips are the Actel pASIC.

The SB (see Figure 3) is a 16 layers PCB, 206 x 98 mm^2, which hosts also LVDS transmitters (National 10-to-1 DS92LV1021 [6]): trigger data are sent to the Regional trigger, through copper cables (see RJ45 connectors at the top in Figure 3). The backside of the SB contains most of the control logic electronics for the mini-crate.

The system to test the SB was designed for checking both the TSM algorithm and the trigger data transmission. The SB receives data from up to 6 TRB, placed along the mini-crate; there could be a sizeable skew between incoming patterns. The SB output is serialized at 480 MHz and transmitted through 2 FTP cables (CAT 6) up to 40 m long. The test system has to detect transmission errors due both to cables and to bad data synchronization.

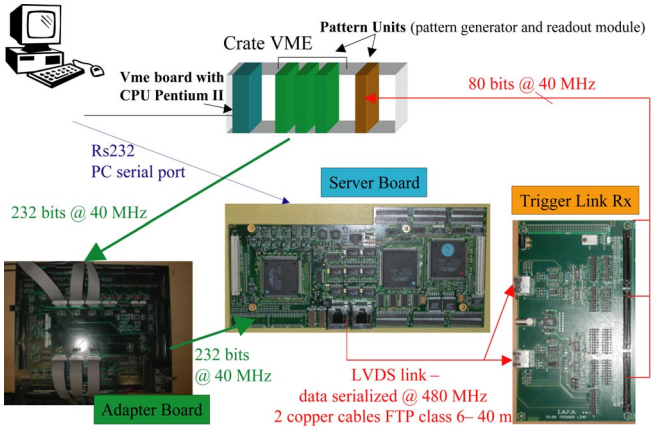

Figure 4: Setup for SB test; paths and types of signals are shown.

In Figure 4 the full setup used for testing the SB is shown.

The core of the test jig is a VME crate, controlled by a VME board with CPU. Three Pattern Units are used for patterns injection and one acts as read-out module. The input patterns were transmitted through flat cables to an Adapter board, which remaps signals, mimicking the TRB output. Then a Trigger Link Receiver board collects the serialized data transmitted by the SB. This module deserializes patterns from 480 to 40 MHz, and sends them to the read-out Pattern Unit. Both TSM functionalities and the trigger chain from the TRB output up to the Sector Collector can be checked.

An RS232 connection, from the CPU module to the microcontroller placed on the SB, allows to monitor and configure TSM chips, and also to check the functionalities of the control logic for the mini-crate.

Two tests have been performed for validating the TSM system, in particular two kind of different patterns have been chosen:

- 1000 "surgical" patterns, developed during the chip design and simulation, thoroughly checking all functionalities in different configurations;
- 10^9 random patterns with different configurations in long tests periods (3-4 days) to check stability and performance.

Successful results of tests made on prototype boards led to approve the pASIC choice.

IV. Summary on Irradiation Tests

In general, electronics to be installed in CMS will have to work in a high-radiation environment. For CMS barrel DTC it was predicted [7] a total integrated neutrons flux of ~3 x 10^{10} neutron/cm^2 for 10 years of LHC running. The flux of neutrons with energy exceeding 20 MeV (relevant for Single Event Upsets (SEU) on electronics) will be of ~10^9 neutron/cm^2. A Total Ionizing Dose (TID) of ~0.01 krad is expected.

Because the local trigger electronics will be inaccessible for most of the time during LHC running, the radiation tolerance of electronic devices has been carefully checked. All electronics devices hosted into the mini-crate have been tested [8]; in the following only measurements concerning the Trigger Server system are reported.

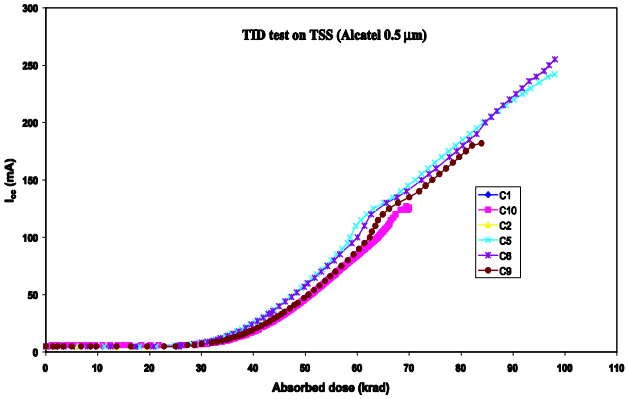

Figure 5: Measured current drawn vs. integrated absorbed dose for 6 TSS chips.

Several tests have been performed at the Cyclotron Research Center of the UCL of Louvain la Neuve (Belgium), with a proton beam of 60 MeV of energy, in order to measure tolerance to the TID and the SEU cross section. In detail, 6 TSS and 4 pASIC of the same batch used for TSM implementation were exposed to the proton beam.

No significant increase in current drawn was observed for TSS (Figure 5) and pASIC (Figure 6) for doses up to about 30 krads (well above the expected one in the DTC).

In conclusion, the measured SEU cross sections leads to calculate the following expected SEU rates when running CMS in LHC:

- TSS: $\sigma_{SEU} = 8.4 \times 10^{-15}$ cm^2/bit
  $R_{SEU} \approx 2$ / 1200 chips
- TSM: $\sigma_{SEU} < 2.9 \times 10^{-12}$ cm^2/chip at 90% c.l.
  $R_{SEU} < 2.2$ / chip

These results confirm that the devices are well tolerant to the radiation level foreseen for the CMS barrel muon chambers.

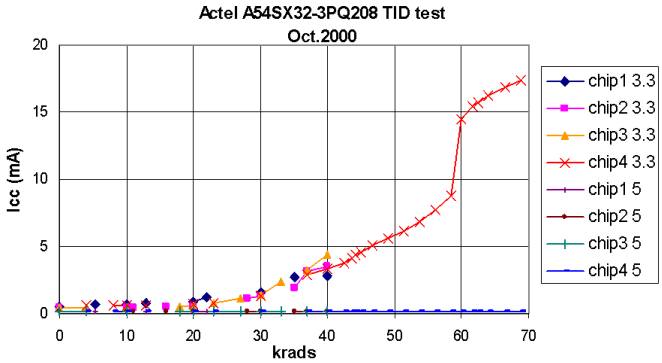

Figure 6: Measured current drawn vs. integrated absorbed dose for 4 ACTEL A54SX32. Two power supply lines were monitored for each chip (3.3 V and 5 V).

V. Trigger Data Transmission

The link between the local trigger and the regional trigger electronics needs must have low power consumption and high throughput. It has been implemented by using LVDS transmission technology, in particular National 10-to-1 DS92LV1021 devices [6] for signal serialization on the SB and National 1-to-10 DS92LV1212A [9] for deserialization, on the Sector Collector side. Dedicated tests were performed with an ad-hoc setup, consisting of a Transmitter board, which receives patterns from a Pattern Unit and send them through 2 FTP cables, to a Receiver board (that one called Trigger Link Rx in Figure 4).

The transmission has been extensively studied with respect to the principal working conditions of the DT system, like temperature, cables length, working frequency and supply voltage. Moreover the link tolerance within the expected amount of jitter of the clock signal in the local trigger electronics environment was verified.

The LVDS link was found to properly work in a range wider than expected in DTC: working frequency from 36 to 44 MHz; supply voltage ± 10% w.r.t the nominal one; cables length from 1 up to 40 m; temperature ranging from 20 °C to 80 °C.

The most stringent test was performed in the worst working conditions, with FTP CAT6 cables, 28m long and a clock jitter of (60 ± 2) ps r.m.s. value. After transmitting a total of 2.034×10^{12} bits, no errors were observed, which corresponds to a Bit Error Rate less than 2×10^{-12}, at 99% confidence level.

The implication of the measured Bit Error Rate on the Trigger system was studied. A bit error implies a possible loss in the trigger efficiency; the generation of fake-triggered events can be in first approximation neglected. With this hypothesis, a very conservative estimate of the fraction of trigger loss can be made, and it has been found to be lower than 5.12×10^{-11}, completely negligible with respect to the total DT intrinsic inefficiency of 2-3% [1].

VI. Test Beam –Preliminary Results

A test of the full electronics in a DTC mini-crate was performed at the end of May '03 at the Cern SPS. A DTC was equipped with the full local electronics and exposed to a muon beam, having LHC-like structure (bunches at 40 MHz frequency).

About 15 million events were collected in 7 angular orientation of the chamber with respect to the beam line (from –30 to 45 degrees) and in 17 different configurations of the trigger devices. The aim was to perform an integrated test of the full DTBX system, for checking all functionalities, trigger performances and the simulation of the detector and the electronics processing. A dedicated sample of events with two muon triggers has been acquired, for analysing more in details the performance of the sorting algorithms in the Trigger Server.

The analysis is in a very preliminary phase, but the quality of data is excellent. In fact the efficiency of BX tagging (a muon track found by the trigger at the expected time) is greater than 95% and limited mainly by the geometrical acceptance. The trigger output timing distribution shows a narrow peak at the correct time; the off-time trigger signals for track of good quality (see section I) are less than 0.1% and they don't affect the track reconstruction in the regional trigger, which receives muon segments from more than one DTC and is able to correctly correlate them.

VII. Conclusions

The local trigger electronics of the DTCs of the CMS barrel has been thoroughly tested in order to verify devices performances and the agreement with the experiment requirements. The Track Sorter Slave and the Track Sorter Master (composing the Trigger Server system) have undergone stand-alone tests and radiation tolerance measurements with successful results.

The link between local and regional trigger electronics of the DTCs has been tested and found to properly work in environment conditions similar to the ones expected in LHC.

An integrated test of the DTC local trigger was performed with the CERN 40 MHz bunched beam and a preliminary analysis of the muon data collected confirms that the system works according to the expectations.

VIII. References

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[9] Data Sheet 100056, National Semiconductor, “DSLV1212A 16-40 MHz 10 Bit Bus LVDS Random Lock Deserializer with Embedded Clock Recovery”, 2000