Full Crate Test of the CMS Regional Calorimeter Trigger.

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Abstract

The CMS regional calorimeter trigger system detects signatures of electrons/photons, τ-leptons, jets, and missing and total transverse energy in a deadtimeless pipelined architecture. It consists of 18 crates containing Receiver Cards with four-gigabit copper cable receiver/deserializers on mezzanine cards. The Receiver Cards deskew, linearize, sum and transmit data on a 160 MHz backplane to Electron Isolation cards that identify electrons and a Jet/Summary card that sums energies. Most processing is done on five high-speed custom ASICs. A clock and control card choreographs the system timing. We present results from testing a completely instrumented and fully functional pre-production crate.

I. Introduction

The Compact Muon Solenoid level-1 electron/photon, τ-lepton, jet, and missing transverse energy trigger decisions are based on input from the level-1 Regional Calorimeter Trigger (RCT) [1]. The RCT plays an integral role in the reduction of the proton-proton interaction rate (10^9 Hz) to the High Level Trigger input rate (10^5 Hz) while separating physics signals from background with high efficiency. The RCT receives input from the brass and scintillator CMS hadron calorimeter (HCAL) and $PbWO_4$ crystal electromagnetic calorimeter (ECAL), that extend to $|\eta|=3$. An additional hadron calorimeter in the very forward region (HF) extends coverage to $|\eta|=5$. A calorimeter trigger tower is defined as 5x5 crystals in the ECAL of dimensions 0.087x0.087 ($\Delta\eta$x$\Delta\phi$), which corresponds 1:1 to the physical tower size of the HCAL. Since the HF is not used in any electron or photon algorithm, it has a coarser segmentation in η and ϕ.

The algorithm to find electron and photon candidates uses a 3x3 calorimeter trigger tower sliding window centered on all ECAL/HCAL trigger towers out to $|\eta|=2.5$. Two types of electromagnetic objects are defined, a non-isolated and an isolated electron/photon. Four of each type of electron per regional crate are forwarded to the Global Calorimeter Trigger (GCT) [2] for further sorting. The top four candidates of each type are received by the level-1 Global Trigger (GT) [3].

The jet trigger uses the transverse energy sums ($E_{T,ECAL}+E_{T,HCAL}$) for each 4x4 trigger tower calorimeter region in the barrel and endcap [4]. In the very forward region ($3<|\eta|<5$) of the CMS spectrometer, each HF tower is treated as a single region and their $\eta\phi$ division matches that of the 4x4 regions of the barrel and endcap. The jet or τ-tagged jet is defined by a 3x3 region E_T sum. In the case of τ-tagged jets (only $|\eta|<2.5$), none of the nine regions are allowed to have more than 2 active ECAL or HCAL towers (i.e. above a programmable threshold). Jets in the HF are defined as forward jets. Four of the highest energy central, forward, and τ-tagged jets are selected, allowing independent sorting of these 3 jet types until the final stage of jet sorting and trigger decision. This sorting is started on the RCT and continued through the GCT, which sends a total of twelve jets to the GT.

II. Calorimeter Trigger Hardware

The regional calorimeter trigger electronics comprises 18 crates for the barrel, endcap, and forward calorimeters. These will be housed in the CMS underground counting room adjacent to and shielded from the underground experimental area.

Twenty-four bits comprising two 8-bit calorimeter energies, two energy characterization bits, a LHC bunch crossing bit, and 5 bits of error detection code will be sent from the ECAL, HCAL, and HF calorimeter electronics racks to the nearby RCT racks on 1.2 Gbaud copper links. This is done using one of the four 24-bit channels of the Vitesse 7216-1 serial transceiver chip on calorimeter output and RCT input, for 8 channels of calorimeter data per chip. The RCT V7216-1 chips are mounted on mezzanine cards, located on each of 7 Receiver Cards and one Jet/Summary Card for all 18 RCT crates. The eight mezzanine cards on the Receiver Cards are for the HCAL and ECAL data and the one mezzanine card located on the Jet/Summary Card is for receiving the HF data. The V7216-1 converts serial data to 120 MHz TTL parallel data, which is then deskewed, linearized, and summed before transmission on a 160 MHz ECL custom backplane to 7 Electron Isolation Cards and one Jet/Summary Card. The Jet/Summary Card receives the HF data and sends the regional E_T sums and the electron candidates to the GCT.

The Receiver Card, in addition to receiving calorimeter data on copper cables using the V7216-1, shares data on cables between RCT crates. Synchronization of all data is done with the local clock and the Phase ASIC (Application-Specific Integrated Circuit--described below). The Phase ASIC also checks for data transmission errors. Lookup tables are used to translate the incoming E_T values onto several scales and set bits for electron identification. Adder blocks begin the energy summation tree, reducing the data sent to the 160 MHz backplane.

The Electron Isolation Card receives data for 32 central towers and 28 neighboring towers via the backplane. The electron isolation algorithm is implemented in the Electron Isolation ASIC described below. Four electron candidates are transmitted via the backplane to the Jet/Summary (J/S) Card. The electrons are sorted in a Sort ASIC on the J/S Card and the top 4 of each type are transmitted to the GCT for further processing. The J/S Card also receives E_T sums via the backplane, and forwards them and two types of muon identification bits (minimum ionizing and quiet bits –

described later) to the GCT. A block diagram of this dataflow is shown in Figure 1.

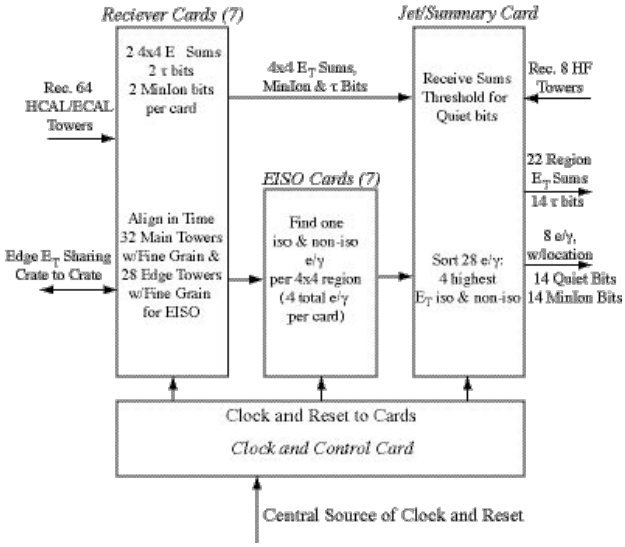


Figure 1: Dataflow diagram for the crate, showing data received and transferred between cards on the 160 MHz differential ECL backplane. Brief explanations of the card functionality are shown. For more details see the text or reference [1].

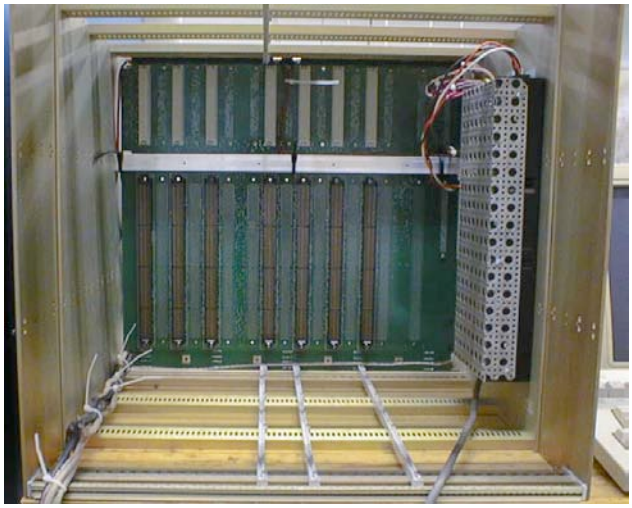
To implement the algorithms described above, five high-speed custom Vitesse ASICs are used: a Phase ASIC, an Adder ASIC, a Boundary Scan ASIC, a Sort ASIC, and an Electron Isolation ASIC [5]. They were produced in Vitesse FX™ and GLX™ gate arrays utilizing their sub-micron high integration Gallium Arsenide MESFET technology. Except for the 120 MHz TTL input of the Phase ASIC, all ASIC I/O is 160 MHz ECL.

The Phase ASICs on the Receiver Card align and synchronize the data received on four channels of parallel data from the Vitesse 7216. The Adder ASICs sum up eight 11-bit energies (including the sign) in 25□s, while providing bits for overflows. The Boundary Scan ASIC handles board level boundary scan functions and drivers for data sharing. Four 7-bit electromagnetic energies, a veto bit, and nearest-neighbor energies are handled every 6.25 ns by the Electron Isolation ASICs, which are located on the Electron Isolation Card. Sort ASICs are located on the Electron Isolation Card, where they are used as receivers, and are located on the J/S Cards for sorting the e/□. All ASICs have been successfully tested and procured in the full quantities needed for the system.

III. PRE-PRODUCTION PROTOTYPES

The successful conclusion of the first generation prototype program proved the design as described in Chapter 5 of the CMS Trigger Technical Design Report (TDR), which was approved in March 2001 [1], marked the start of the construction of full-function pre-production modules[6] based on the TDR. A custom pre-production prototype 9U VME crate, Clock and Control Card, Receiver Card, Electron Isolation Card, and Jet/Summary Card were produced with the above ASICs. Mezzanine cards with the Vitesse 7216-1 serial link for the Receiver Card and dedicated test cards were also constructed.

We have built a pre-production crate, shown in Figure 2 with a new backplane that implements all of the level-1 trigger algorithms approved by CMS and the LHCC, and documented in the Trigger TDR [1]. The backplane is located in the middle of the crate between a card cage 400 mm deep in the rear and a card cage 280□mm deep in the front. As shown in Figure 2, the backplane is a monolithic, custom, 9U high printed circuit board with front and back card connectors. The top 3U of the backplane utilizes 4 row (128 pin) DIN connectors, capable of full 32-bit VME. The two leftmost front slots of the backplane use three row (96 pin) DIN connectors in the P1 and P2 positions with the standard VME pin assignments. Thus, a standard VME system module can be inserted in the two front stations with a form factor conversion between the first slot and remaining slots performed on the custom backplane.



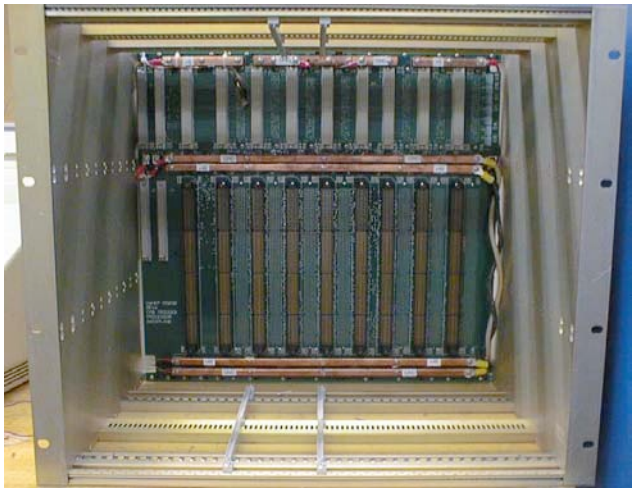


Figure 2. Pre-production crate: rear (top picture) and front (bottom picture) view.

The rear of the crate behind the two standard VME stations is occupied by the VME power supply. Power to the DC-to-DC converters on the boards is provided by an external 48 V power supply connected to the bus-bars visible in the front view of the crate shown in Figure 2. In the data processing section of the crate (the bottom 6U of the backplane) a single high speed, controlled impedance, AMP 340-pin stripline connector is used for both front and rear card insertion. The

stripline connectors have a power plane between every four signal pins, producing an impedance of 50 . Separate high current contacts, provided for the power plane connections, are used to transmit power to the boards. The connectors are housed in a cast aluminum shell that doubles as a board stiffener. The electrical characteristics of the connectors are excellent, allowing sub-nanosecond rise times with very low crosstalk. Data is transmitted across the backplane in 160 MHz differential ECL

We have built a new Clock and Control Card, (front side shown in Figure 3), that matches the timing in the new backplane and cards. The Clock and Control Card distributes 160 MHz clocks and resets across the backplane to all cards, with delay adjusts on the back of the card to allow for differences in travel times across the backplane. The 120 MHz clocks for the Vitesse 7216-1 serial links and the Phase ASICS are also sent out to the Receiver Cards and Jet/Summary Card via the backplane. Power distribution on all the cards is handled with DC-to-DC converters fed with 48 V from the backplane power pins.

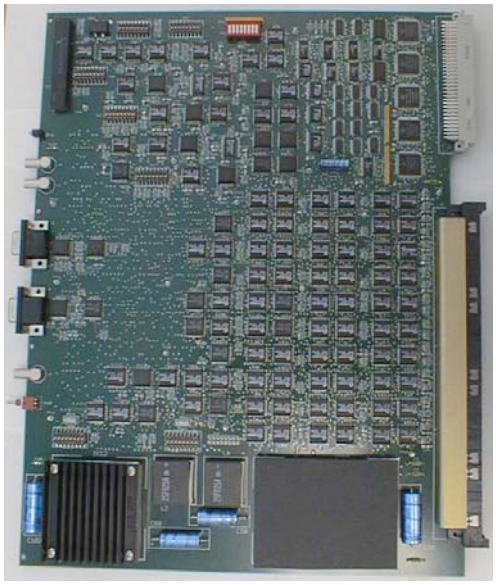


Figure 3. Pre-production Clock & Control Card.

We constructed eight full function Receiver Cards, shown in Figure 4 and Figure 5, on which we installed the Adder, Phase and Boundary Scan ASICs, as well the new version of the 4 x 1.2 Gbit/s serial receiver mezzanine card, shown in Figure 6. The new Receiver Card features mezzanine cards with an improved version of the Vitesse serial receiver chip that is more tolerant of clock jitter. Two channels of tower data for each of four channels of serial link are received per mezzanine card for a total of 64 channels of data from the HCAL and ECAL per Receiver Card. Parallel data out of the Vitesse serial link are aligned via the Phase ASIC and then sent to the memory lookup (LUT) to linearize the data and set the electron identification bit for the electron algorithms. From the memory lookup, seven bits of ECAL E_T and one electron identification bit are sent to the Electron Isolation Card via the Boundary Scan ASICs. The Boundary Scan ASICs also handle the shared data coming in from other crates via the SCSI type cables at the front of the card. In addition, a sum of $E_{T,HCAL} + E_{T,ECAL}$, is sent from the memory lookup to two stages of Adder ASICs to form the 4x4 region sums that then travel via the backplane to the Jet/Summary Card.

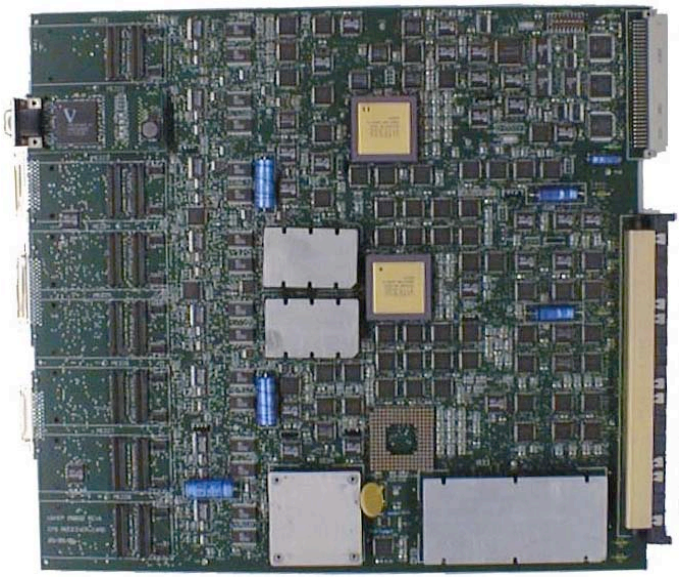


Figure 4. Pre-production Receiver Card (front) showing Adder ASICs and a Mezzanine Receiver Card installed.

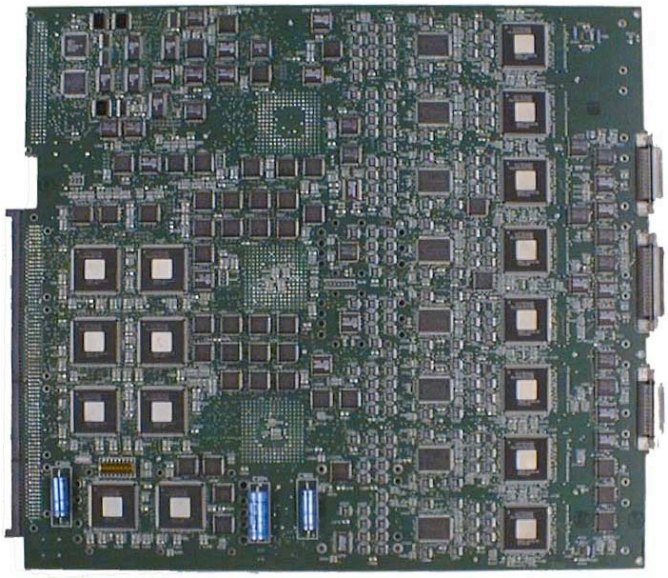


Figure 5. Pre-production Receiver Card (rear) showing Phase and Boundary Scan ASICs and lookup tables.

Figure 6. Close up of a pre-production 4 x 1.2 Gbit/s Copper receiver mezzanine card.

We have also built a dedicated new Serial Test Card, shown in Figure 7, for testing the receiver mezzanine cards

and performing detailed bit error checking. Additional copies of this card are being used for production testing of the mezzanine cards and integration tests with ECAL and HCAL electronics.

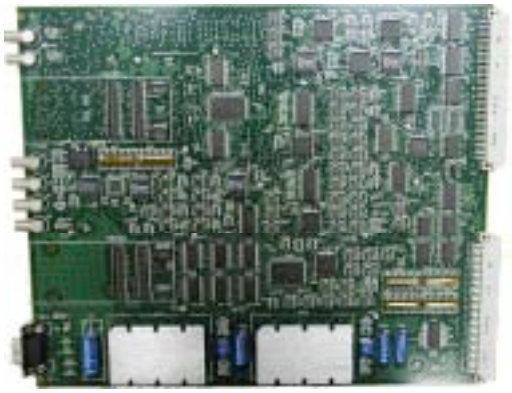


Figure 7. Pre-production Serial Link Test Card.

A set of 8 full function Electron Isolation Cards has been built (Figure 8) on which we have installed the Electron Isolation and Sort ASICs. Data are received over the backplane from the Receiver Card via the Sort ASICs' differential input. The Sort ASIC's sorting feature can be set on or off and is off for receiving data on the Electron Isolation Card. This data includes 16 towers for each Region and 28 towers of neighbor data coming from adjoining Receiver Cards or neighboring crates via the data sharing cables at the front of the Receiver Card. Alignment in time is done at the Boundary Scan ASIC on the Receiver Card. The total of 44 towers are sent to two Electron Isolation ASICs which choose the two highest energy electrons of each type, isolated and non-isolated. A memory lookup compresses the seven bit energies to six bits and sets a location bit for each region served by the card.

We have built a pre-production J/S card. It received the E_T and position information for the four electrons from the electron Isolation card via the backplane. The HF data is received via one receiver mezzanine card located at the top of the J/S card (seen in Figure 9). Since each HF tower also represents one HF Region, the Phase ASIC handles the data, and then two Memory lookups handle the energy assignment of the four different □ slices of the HF. This information is delayed using Boundary Scan ASICs to align it with the Region E_T sums from the Receiver Cards and then forwarded with a quality bit to the GCT.

IV. Test Results

We have completed a detailed testing and validation program of these pre-production trigger boards. We have tested a fully functional crate with its full complement of pre-production Backplane, 7 Receiver Cards, Clock Card, 7 Electron Isolation Cards, and the Jet/Summary Card as shown in Figure 10 and Figure 11. These tests have fully verified all 5 Vitesse custom ASICs and we have completed their production. The Receiver Card, Clock Card and Electron Isolation Card have been validated and are in production. The Jet/Summary Card, Crate, and Backplane have also been verified and are being readied for production. Verification of data pathways and logic function is checked using Boundary Scan, which is fully implemented on all boards and ASICs. The output of the J/S Card has also been validated through integration tests with the GCT.

Figure 8. Pre-production Electron Isolation Card with Electron Isolation and Sort ASICs installed.

Figure 9. Pre-production Jet/Summary Card.

Additionally, we have completed tests of the pre-production 4 x 1.2 Gbit/s copper serial link system. The cable used in the tests was composed of two 20 m lengths of 22 AWG Spectra Strip Skew-Clear® shielded 2-pair cable with VGA-type 15-pin DIN connectors. We built a special "test" transmitter mezzanine card to drive the signals over the cables and used two Serial Link Test Cards to continuously transmit and receive pseudo-random data over many days with a trap on error, yielding a bit error rate of less than 10^{-15}. The full Receiver Mezzanine Card production run is complete and the Serial Test Cards are being used to test this production run in-house and have been sent out to other laboratories to assure compatibility of the RCT with the ECAL and HCAL electronics [5].

Figure 10. RCT Full Crate Test front side.

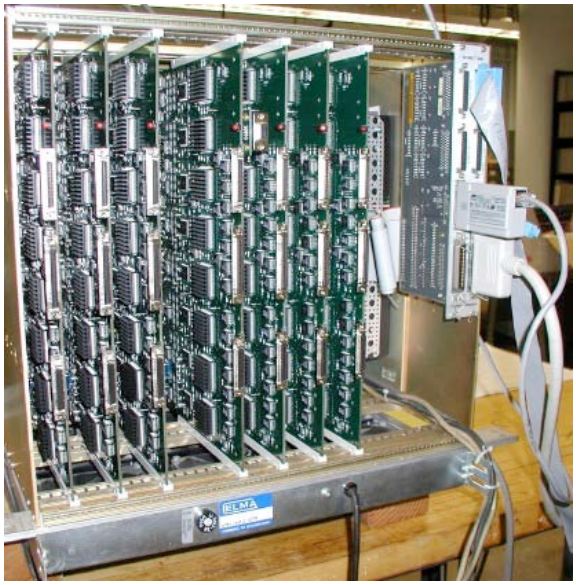


Figure 11. RCT Full Crate Test rear side

The detailed testing of the boards in the full crate test has led to the development of production testing sequences for the boards. After visual inspection, the Receiver, Electron Isolation and Jet/Summary Cards have their VME programming checked by reading and writing command registers. Then the memory look-up tables are loaded with random data and read back. The next step is to run the JTAG program on the full crate. This verifies the ASIC to ASIC paths, including those through the backplane. Then we load the memories with specific data and cycle the Phase ASIC test vectors to send known patterns through the regional sum and electron data paths. Finally, we verify the links through reception of data from a Serial Test Card through the Receiver Mezzanine Cards as shown in Figure 12. Clock and Control Cards are tested against a known working board and then are placed in a fully working crate to verify timing in detail. After initial checkout, backplanes are fully populated with a known working set of cards for final checkout.

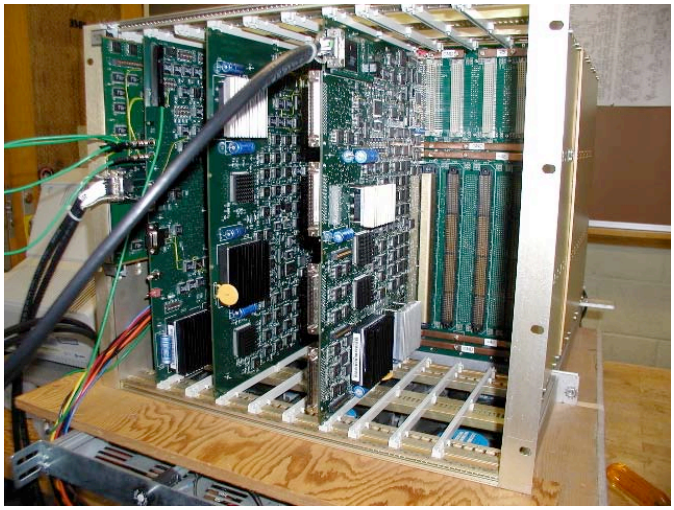


Figure 12. Testing Jet Summary Card with input data from Serial Test Card.

V. Summary

Testing of the CMS level-1 Regional Calorimeter Trigger Pre-production Prototype Receiver Card, Isolation Card, Jet/Summary Card, Clock and Control Card, Serial Link Mezzanine Card, Backplane, Crate and five custom ASICs that implement the CMS level-1 calorimeter trigger algorithms is complete. These tests conducted have validated the design of the production boards and production of the system has started.

VI. Acknowledgments

This work was supported by the United States Department of Energy and the University of Wisconsin.

VII. References

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