The Level-1 Global Muon Trigger for the CMS Experiment

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Abstract

The three independent Level-1 muon trigger systems in CMS deliver up to 16 muon candidates per bunch crossing, each described by transverse momentum, direction, charge and quality. The Global Muon Trigger combines these measurements in order to find the best four muon candidates in the entire detector and attaches bits from the calorimeter trigger to denote calorimetric isolation and confirmation. A single-board logic design is presented: via a special front panel and a custom back plane more than 1100 bits are received in every bunch crossing and processed without dead-time by pipelined logic implemented in five large and several small Xilinx FPGAs.

I. Introduction

CERN's new Large Hadron Collider (LHC) will provide proton-proton collisions at a bunch crossing frequency of 40 MHz. With a typical event size of around 1 MB in the general purpose experiments CMS and ATLAS, data handling and storage capabilities will limit the rate of events to be stored for offline analysis to of the order of 100 Hz. The enormous reduction from 40 MHz to ~100 Hz has to be performed on-line by the trigger system of the experiment. In the Compact Muon Solenoid (CMS) experiment, two trigger levels will be employed. The fully pipelined custom-built Level-1 Trigger [1] electronics will analyse every bunch crossing without dead-time and reduce the rate below 100 kHz based on coarsely segmented data from the muon system and calorimeters. The remaining rate reduction will be performed by the High Level Trigger [2] algorithms running on a large farm of commercial processors.

The present paper deals with the Global Muon Trigger, a central part of the Level-1 Trigger electronics, which is responsible for combining the information delivered by three independent muon trigger systems in CMS. Relying on sophisticated algorithms it significantly improves background rejection in the muon trigger while maintaining high efficiency. The Global Muon Trigger algorithms will be implemented in several large Xilinx Field Programmable Gate Arrays (FPGAs) that are currently being designed.

II. The CMS L1 Trigger

The CMS Level-1 Trigger (Figure 1) consists of three main systems: the Calorimeter Trigger, the Muon Trigger and the Global Trigger. The Muon Trigger and the Calorimeter Trigger identify trigger objects such as muons, electrons/photons, jets and the total and missing transverse

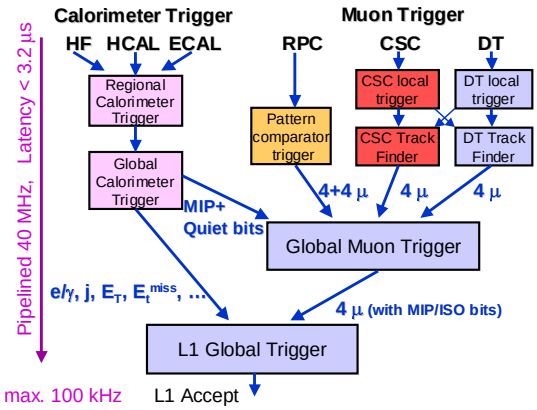

Figure 1: The CMS Level-1 Trigger.

energies. Trigger objects include the transverse momentum or energy as well as the directions in ϕ and η of the object. The Level-1 trigger decision is determined by trigger algorithms computed in the Global Trigger [3]: algorithms check for trigger objects passing certain programmable thresholds or combinations of trigger objects which may include topological conditions such as a check for back-to-back objects. Up to 128 algorithms can be processed in parallel, the final L1 decision being the logical OR of all algorithms after taking into account possible pre-scaling factors.

Three muon systems are employed in CMS and all of them are used in the L1 Trigger: four stations of Drift Tube (DT) Chambers with bunch-crossing identifying capabilities cover the barrel region, each station consisting of twelve (or eight) staggered layers of drift tubes. Four disks of Cathode Strip Chambers (CSCs) cover each of the two endcaps, each disk consisting of 6 layers of chambers. Local triggers identify track segments at the muon stations, which are then connected to muon candidate tracks by track finders, separately for the barrel and the endcaps. As a third complementary system, layers of Resistive Plate Chambers (RPCs) are mounted on the DT and CSC stations in the barrel and endcaps. RPC hits are processed by an independent Pattern Comparator Trigger, which identifies muon candidates based on hits.

III. Global Muon Trigger Algorithm

It is the task of the L1 Global Muon Trigger (GMT) to combine the muon candidates from the three muon systems in an optimal way and to find the best four over-all muon candidates in the detector. Additionally the Global Muon Trigger checks for calorimetric isolation of the muon candidates and for confirmation of the candidates by checking the energy deposit in the calorimeter.

A. Input

The Global Muon Trigger receives in every bunch crossing up to four muon candidates each from the DT and RPC Triggers in the barrel region and up to four muon candidates each from the CSC and RPC Triggers in the forward region. Candidates consist of measurements of transverse momentum (5 bits), sign of charge (2 bits), azimuthal angle ϕ (8 bits) and pseudorapidity η (6 bits) at the muon system as well as a quality code (3 bits).

From the Global Calorimeter Trigger the GMT receives MIP and Quiet bits for each of 252 calorimeter regions measuring $\Delta\eta$ x $\Delta\phi$ = 0.35 x 0.35 rad. MIP bits denote compatibility of the energy deposit in the calorimeters with the passage of a minimum ionising particle while Quiet bits indicate that the energy deposit in the region was below a certain threshold.

B. Functionality

By combining candidates from the regional triggers the GMT naturally increases trigger efficiency, especially in detector regions of slightly different geometric acceptance of the regional triggers. The GMT matches candidates of complementary regional triggers based on their coordinates η and ϕ in order to confirm them. By applying selection criteria based on quality and pseudorapidity to the remaining unconfirmed candidates, the GMT can significantly lower the trigger rate caused by fake or improperly measured muons while keeping the efficiency close to the maximum possible [4].

A further significant reduction of trigger rates can be achieved by careful merging of the parameters of matched candidates based on their detector region and qualities: proper combination of transverse momentum measurements can to a great extent reduce the effect of feed-through (assigning high transverse momenta to low-momentum muons) [5].

The suppression of certain types of low-quality unconfirmed muons in the di-muon trigger considerably reduces the rate contribution due to ghosts in some regions of pseudorapidity. A special case is the barrel/endcap overlap region, where ghosts can arise because the DT and CSC Triggers share several chambers. Special cancel-out units in the GMT can eliminate almost completely these ghosts [5].

An additional function of the GMT is the correlation of muon candidates with calorimeter regions in order to check the candidates for confirmation and isolation. Starting from their positions (η and ϕ) in the muons system, the candidates are propagated to the calorimeter/vertex, based on their charge and transverse momentum measurements using tabulated parameterisations of muon trajectories. For confirmation, the calorimeter MIP bit at the propagated position of the muon in the calorimeter is attached to the muon candidate. In order to check a muon candidate for isolation, calorimeter Quiet bits are checked in calorimeter regions corresponding to the direction of the muon at the vertex (axis of a potential jet). An Isolation bit is attached to a muon candidate when the calorimeter region or multiple regions around the potential jet

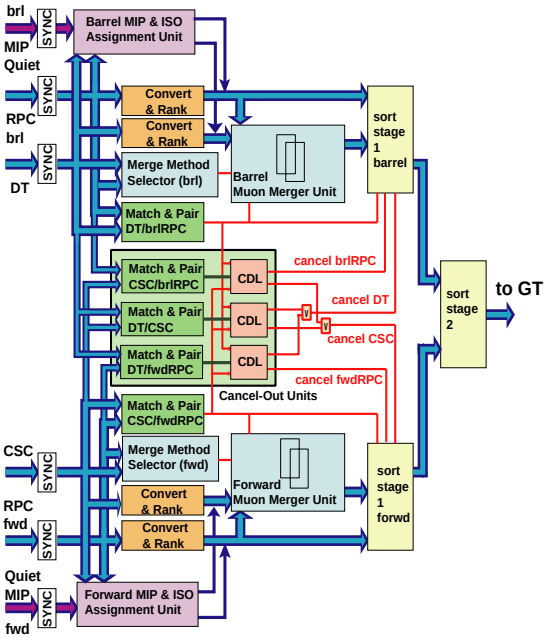

Figure 2: Block Diagram of the Global Muon Trigger.

axis have their Quiet bit(s) set. Isolation and MIP confirmation can be used as additional criteria for trigger conditions in the Global Trigger.

A complete list of the functions performed by the GMT is given, below:

- **Synchronizing** the muon candidates and calorimeter bits to each other and to the LHC orbit.
- **Matching and Pairing** DT with barrel-RPC muons in the barrel and CSC with forward-RPC muons in the endcaps based on their proximity in η and ϕ.
- **Merging** the parameters of corresponding pairs of candidates from complementary systems.
- **Converting** pseudorapidity measurements to a common scale.
- **Detecting possible ghosts or fake triggers** by tagging unconfirmed low-quality candidates in certain regions of pseudorapidity in order to exclude them from certain trigger algorithms.
- **Cancelling-Out** duplicate candidates in the barrel/endcap overlap region., especially candidates detected by both the DT and CSC Triggers.
- **Propagating** muon candidates from the muon system to the calorimeter and vertex in order to check for calorimetric isolation or confirmation.
- **Ranking and Sorting** the candidates in order to determine the four most important ones.

The algorithm of the GMT (Figure 2) has been designed based on the above requirements. In order to process muon candidate data within a maximum latency of 10 slots of 25 ns, functions are performed in parallel wherever possible. Most of the GMT functions such as matching, merging, detection of

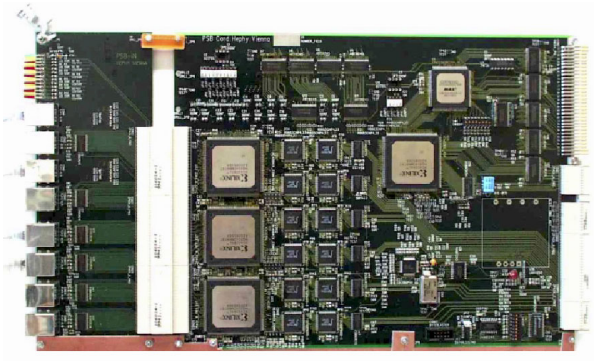

Figure 3: Prototype of the PSB card.

low quality candidates, ranking and propagation depend on the detailed characteristics of the regional trigger systems or on the alignment of the trigger systems and calorimeters. In order to keep the GMT as flexible as possible, all the main functions are configurable via memory-based Look-Up Tables (LUTs). LUT contents have been optimised according to the simulated performance of the regional trigger systems based on the default detector geometry. In future the actual measured characteristics of the regional trigger systems and the alignment can easily be taken into account by updating the LUT contents.

The algorithm has been modelled in C++ and simulated in the framework of the ORCA [6] detector simulation software. Its performance has been demonstrated in many detailed simulation studies [1, 2, 4, 5].

C. Output

The GMT sends up to four muon candidates to the Global Trigger, each candidate consisting of measurements of transverse momentum (5 bits), sign of charge (2 bits), azimuthal angle ϕ (8 bits) and pseudorapidity η (6 bits), quality code (3 bits) as well as a MIP bit and an ISO bit denoting calorimetric confirmation and isolation.

IV. Global Muon Trigger Implementation

In order to reduce processing time and to enable cancel-out links between barrel and forward processing chains, the main functions of the GMT will be performed on one single 9U VME board, the GMT Logic Board. Three additional Pipeline Synchronizing Boards (prototype shown in Figure 3) receive, synchronize and optionally delay the calorimeter MIP and Quiet bits. All four boards are housed in the Global Trigger crate next to the Global Trigger boards.

A. The GMT Logic Board

The GMT Logic Board (Figure 4) receives signals of the 16 input muons on 16 SCSI-2 cables connected to a special wide input board mounted in parallel to the front panel and connected to the GMT Logic Board by edge connectors. Parallel LVDS transfers (32 bits per muon including status bits) are used in order to keep latency low. The synchronized calorimeter bits are received via the custom-built backplane at 80 MHz in order to halve the number of connections. The output muon candidates (26 bits per muon) are sent to the Global Trigger directly via the backplane using 80 MHz GTL+ signals. VME, JTAG and control signals as well as a Channel Link for readout by Data Acquisition are also connected via the backplane.

The GMT logic is implemented in several Xilinx FPGAs as illustrated in Table 1. In order to simplify routing of the board, the possibility of placing the large FPGAs on mezzanine boards is currently being investigated. The FPGA design currently targets the Virtex II series but a move to the new and more economic Spartan 3 series will be considered if the new devices are available by the time of board production.

Table 1: FPGAs on the GMT Logic Board

FPGA	# chips	Chip Model	I/O pins
Input (RPC/DT,CSC)	4	XC2V2000	388/444
MIP & ISO Assignment	2	XC2V3000	432
Logic	2	XC2V3000	464
Sorter	1	XC2V3000	408

B. Input FPGAs

Muon candidate signals are received by LVDS receivers and then synchronized and - if necessary - delayed by a programmable delay in the *Input FPGAs*. Synchronization circuits [7] sample the incoming signals with 160 MHz and select the sample furthest away from the switching time.

C. MIP and ISO Assignment FPGAs

MIP and Isolation bits are assigned to the synchronized muons in the *MIP and ISO Assignment FPGAs*. The coordinates of the muons in the muon systems are propagated to both the calorimeters and the vertex using look-up tables separately in ϕ and η. By cascading up to three stages of smaller look-up-tables it is possible to implement the propagation in the available internal Block RAMs of the Xilinx FPGAs.

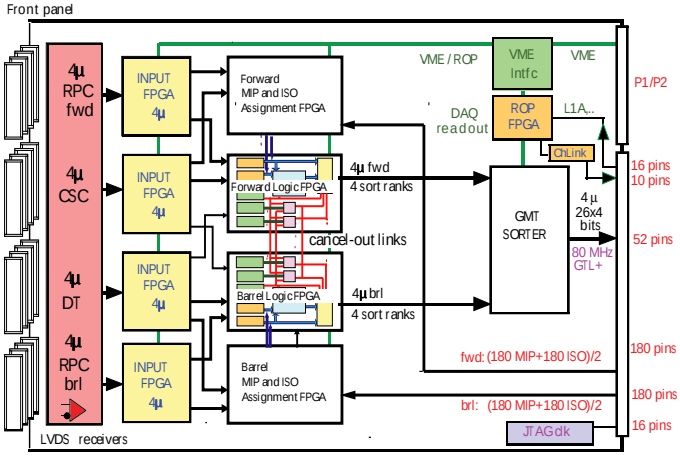

Figure 4: Global Muon Trigger Logic Board.

D. GMT Logic FPGAs

The bulk of the GMT functions are performed by the two *GMT Logic FPGAs* separately for the barrel and for the endcaps. Figure 5 shows a block diagram of the Forward Logic FPGA including timing details. Complementary candidates are matched in the Matching Unit. Pairs of corresponding measurements are determined. In parallel a sort rank is calculated for each muon based on its transverse momentum, quality and position using two stages of look-up tables implemented in Block RAMs.

Also in parallel, the Merge Method Selection unit determines for each possible pairing of muons and for each parameter if the parameter is to be taken from the RPC or from the DT(CSC) candidate or if a special combination of the two parameters is to be performed. The selection of a parameter can be fixed to one system or depend on merge ranks which are calculated mainly from pseudorapidity and quality in two stages of LUTs. Alternatively, the parameter can be taken form the system that delivered the lower transverse momentum. The latter option can be combined with the merging based on merge ranks.

The subsequent Muon Merger Unit merges RPC and DT(CSC) candidates and their sort ranks based on the results of the Pair Logic and the Merge Method Selection Unit.

In order to detect duplicate candidates in the overlap region, cancel-out units compare CSC candidates with DT and barrel-RPC candidates (barrel chip) and DT candidates with CSC and forward-RPC candidates (forward chip). If duplication is detected, one of the concerned candidates may be cancelled based on whether the candidates are confirmed by the complementary system. Several cancel-out links between the Barrel and Forward Logic FPGAs are required for this to work. Cancel-out signals are transferred between the Logic FPGAs at 80-MHz in order to reduce latency.

Unconfirmed RPC candidates and DT(CSC) or merged candidates are sorted by the Barrel (Forward) Sorter Unit which determines the best four muons of the barrel (endcaps) based on the sort ranks.

E. Sort FPGA

The best four barrel candidates and the best four endcap candidates are transferred from the Barrel and Forward Logic FPGAs to the *Sort FPGA* along with their sort ranks. The candidates are again sorted by rank and the four best are forwarded to the Global Trigger.

F. Other Logic

The Input FPGAs and Sort FPGA additionally contain readout circuits that store incoming and outgoing muon data in ring buffers in order to be read out by Data Acquisition for triggered bunch crossings.

A *Read-Out Processor* controls the read-out and transfers the data to a Read-Out Board located in the same crate via a Channel Link. A *VME Interface* chip handles VME transfers to access the registers and memories in all FPGAs.

V. FPGA Development

The main focus of work in 2003 has been on FPGA development. The employed design flow starts from a hardware model written in the VHDL hardware description language. For functional verification the model is simulated with the VHDL simulator NCSIM by Cadence [8]. The model is synthesised with the synthesis software Synplify by Synplicity [9] and implemented with the Xilinx [10] ISE tools. To verify timing, a gate-level model of the implemented design is again simulated with the Cadence NCSIM VHDL simulator.

While most VHDL code has been written manually, for the look-up tables a special solution has been developed. The function to be represented by the look-up table is first implemented in a C++ class that can be directly used in the C++ simulation of the trigger. Tools have been developed to convert the C++ class to a VHDL wrapper and all the files needed to create Block RAM or Distributed RAM cores with the correct initialisation values using the Xilinx Core Generator. The solution ensures that exactly the same operations are performed in the C++ simulation and in the final hardware.

Scripts and Makefiles have been written to automate most of the design flow and the testing procedures. Test benches have been developed for each FPGA in order to test both the behavioural VHDL model and the gate level model produced by the implementation tool. In the C++ simulation the inputs, outputs and intermediate signals of the GMT simulation are saved to an ASCII file that is read in by the test bench in order to generate test vectors and to verify chip outputs and intermediate results. Simulation runs can easily be started from the command line in order to be able to verify the design after every change.

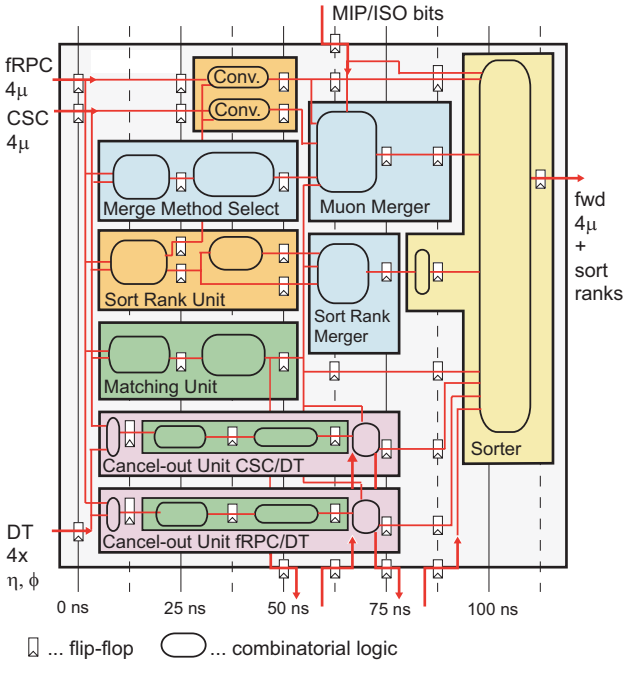

Figure 5: GMT Forward Logic FPGA, simplified.

VHDL sources and related scripts/Makefiles are stored in a code repository using the Concurrent Versions System [11], which is commonly used for software projects. The system facilitates distributed code development and allows keeping track of the history of the sources.

VI. CONCLUSION

The L1 Global Muon Trigger is a central component of the CMS First-Level Trigger. It combines the muon candidates found by the three muon trigger systems in CMS and identifies the best four candidates in every bunch crossing. Its elaborate algorithms significantly improve background rejection, efficiency and ghosting as proven by detailed simulation studies. The GMT furthermore checks for calorimetric isolation and confirmation of the muon candidates. A compact design consisting of four VME boards - one main Logic Board and three Pipeline Synchronizing Input Boards - has been developed in order to minimize processing time. The main functions of the GMT are implemented in five large Xilinx FPGAs on the 9U GMT Logic Board. Development of the FPGA firmware using modern methods and tools is close to completion. Board production and tests are planned for 2004.

VII. REFERENCES

[1] CERN/LHCC 2000-38, *"CMS, The TriDAS Project, Technical Design Report, Volume 1: The Trigger Systems"*.

[2] CERN/LHCC 2003-26, *"CMS, The TriDAS Project, Technical Design Report, Volume 2: Data Acquisition and High-Level Trigger"*.

[3] Nucl. Instr. Meth. A473 (2001), 231, C.-E. Wulz, *Concept of the First Level Global Trigger for the CMS Experiment at LHC"*.

[4] CMS NOTE-2001/003, H. Sakulin and M. Fierro, *"Studies of the Global Muon Trigger Performance"*.

[5] PhD Thesis, TU Vienna, 2002, H. Sakulin: *"Design and Simulation of the First Level Global Muon Trigger for the CMS Experiment at CERN"* http://cmsdoc.cern.ch/documents/03/doc2003_005.pdf

[6] Object Oriented Reconstruction for CMS Analysis http://cmsdoc.cern.ch/orca

[7] Nucl. Instr. Meth. A473 (2001), 243, A. Taurok, H. Bergauer, M. Padrta, *"Implementation and Synchronisation of the First Level Global Trigger for the CMS Experiment at LHC"*.

[8] CADENCE: www.cadence.com

[9] SYNPLICITY: www.synplicity.com

[10] XILINX: www.xilinx.com

[11] Concurrent Versions System: www.cvshome.org