Control slice prototypes for the ALICE TPC detector

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Abstract

ALICE TPC (Time Projection Chamber), worldwide the largest TPC under construction, imposes the development of a high-performance control system to ensure the stability and uniformity of gas and temperature over the sensitive volume. The present paper describes control slice prototypes of the DCS system, including high and low voltage controls as well as temperature monitoring of the Front-End Electronics (FEE) cooling system. Currently available industrial and "in-house" hardware solutions have been tested in the present control slice prototype, like *Iseg Power Supply* for High Voltage, *Wiener Power Supply* for Low Voltage and the CERN "in-house" Embedded Local Monitor Box (ELMB) for the temperature monitoring. For all this hardware, control software has been written in PVSSII, the CERN selected SCADA software package. JCOP software tools have been used whenever needed. The current status of the TPC vertical control slice prototype is reviewed.

I. OVERVIEW

The ALICE TPC [1] is the main tracking detector of the central barrel and together with the ITS (Inner Tracking System) and TRD (Transition Radiation Detector), it must provide good particle identification and two-track separation in the region of $p_T < 10$ GeV/c and pseudorapidities $|\eta| < 0.9$, in addition to momentum measurements of charged particles. The TPC requires a high stability and uniformity within the sensitive volume of the TPC over the long drift distances and precise control of High and Low Voltage for the operation of the ReadOut Chambers (ROC). This represents a technical challenge for the control system.

In the present paper we report on three common solutions; High and Low Voltage and Temperature monitoring. Their architecture is described and results of tests done with these prototypes are presented. These prototypes were developed first as local control. They were tested for different applications, and the behaviour of the hardware was understood. After this step accomplished, the systems were modelled to be included in the FSM architecture prototype.

All FSM subsystems have been simulated, but only the High Voltage prototype was connected to real hardware. In the near future all the subsystems will be controlled and monitored from a FSM.

II. CONTROL CONCEPT

The development of the ALICE control system is a "bottom-up" approach. The control concept starts from the hardware processes up to the higher field layers with the aim of producing building blocks that can be standardized. These building blocks are later included in the Detector Control System (DCS) hierarchy of Finite State Machine (FSM). The topmost layer is the Experimental Control System (ECS) that synchronises and coordinates the DCS, Data Acquisition (DAQ) and Trigger systems. During normal operation the shift crew (that has not necessarily knowledge about the sub-detectors) operates the detector from the ECS level. The ALICE Control System will have to control and monitor 19 sub-detectors, with up to 300 physical devices. To come to a homogenous control system, common solutions that can be used by several sub-detectors are necessary.

So far, ten common solutions and fifteen detector specific solutions have been identified. Some of these common solutions are applicable to the TPC:

- High and Low Voltage
- Temperature Monitoring
- Gas System and Cooling

For all of these common solutions, prototypes have been built as vertical control slice. The concept of a vertical control slice is described (see Fig.1).

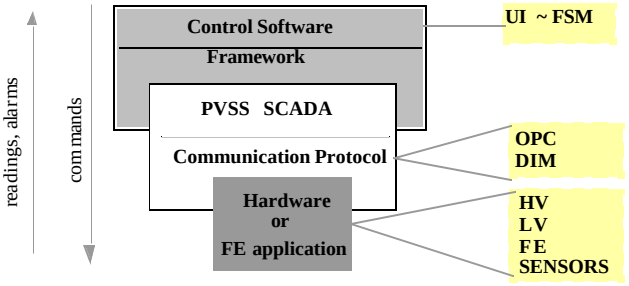

Figure 1: *Vertical Control Slice*

The hardware level can represent temperature sensors, as well as Front-End Electronics, a power supply (Low Voltage or High Voltage) or a cooling plant. The hardware is communicating with the supervisory level, PVSSII [2] (the SCADA tool, selected by CERN and used by all LHC experiments), through the communication protocols, OPC (OLE for Process Control) or DIM (Distributed Information Management). OPC is based on COM/DCOM (Distributed Component Object Model) technology, and represents the standard PVSSII communication (API/Driver) mechanism. DIM has been developed at CERN and used in the LEP experiments. Most of the hardware is integrated in the Framework, which is a JCOP (Joint COntrols Project) development tool. At the highest layer of the vertical slice

control is available through either a User Interface (UI) control software or a FSM [3] application.

III. CONTROL SLICE PROTOTYPES

A. High Voltage (HV)-prototype

Iseg [4] HV Power Supplies are planned to use for the TPC Readout Chambers operation. HV must be delivered to anode and edge wires and skirt channels (in total 288 channels) with 4 different voltages 1280, 1450, 600 and 400V and different polarities.

For the HV prototype, the *Iseg* module EHQ F025p (16 channels, 2.5kV and 200μA) has been used. The module was housed in an *Iseg* ECH238 crate and controlled via a CanBus interface installed in a PC. The following types of CanBus interfaces can be used: ISA, Dongle, USB or PCI.

For this prototype the *Peak* [5] PCI Can card (2 ports, 125 kb/s), and the *Kvaser* [6] PCI Can card (2 ports 125 kb/s) were used. A PVSSII control application was written [7]. The HV module was connected to a test box that emulates 16 Readout Chambers of the TPC, each of them under a permanent load of 1μA at 1000V (see Fig. 2).

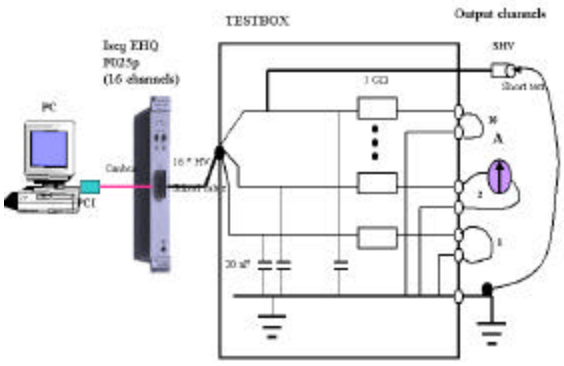

Figure 2: *Schematics of the test box used for Iseg EHQ F025p tests.*

As communication protocol, two solutions were used: the custom IT-CO developed OPC server [8], and the *Iseg* OPC server v2.02, which is an intermediate version of the final *Iseg* OPC server. The main scope of the test was to understand the HV module behaviour during normal and exceptional operating modes of the TPC ROC. Communication failure with the Power Supply have been simulated, i.e. CanBus corruption and computer crash. The voltage output was stable during all these situations. A correct reaction in case of over-voltage or over-current, by tripping off the HV bad channels was observed. Detailed results of the test are reported elsewhere [9].

Although the *Iseg* OPC server v2.02 is not yet the final version, it is working very well with PVSSII OPC clients. Tests with a fully loaded crate and long term stability are planned for the near future.

The High Voltage prototype was included in the FSM prototype. Three state diagrams were implemented in the FSM, describing the operating mode of the crate, of the module and of the channel itself. The connection with the PVSSII control software prototype was done. Test of operating the system from the FSM was done with a real hardware connection for 16 channels and simulated for 100 channels. Although the final scheme of operating the ROC was not performed, the main operations, like ramping up/down, error recovering, On/Off state etc. behaved very well. Further test of FSM scalability and distributing the system over several computers will be done in the near future.

B. Low Voltage (LV)-prototype

The Low Voltage system must deliver voltages between 3.3 and 4V and high currents up to approximately 200A to the Front-End Cards (FEC) installed in the TPC ROC.

The Power Supply selected for tests and prototype is a *Wiener* PL 500 crate with modules, which have as output 2-7V, and 115A or 230A. *Wiener* PL500 is controlled via a CanBus. For the prototype, the *Kvaser* PCI Can card (2 ports 125 kb/s) was used and was installed in the same computer as the Can interface for the *Iseg* HV module.

The *Wiener* OPC server is still under development and not yet available, so the custom IT-CO solution was used instead. A PVSSII control application was developed. A detailed description of the control programs is described elsewhere [10].

The prototype was used for bus bar measurements with voltages and currents listed in Table 1.

Table 1

Bus Bar description	Voltage on load (V)	I stby (A)	I max (A)	Bus bar Sect (mm^2)
Analogue	4.0	60	60	100
Digital	3.3	133	194	200

During the test the power supply responded well to all control operation and measurement (see Fig.3).

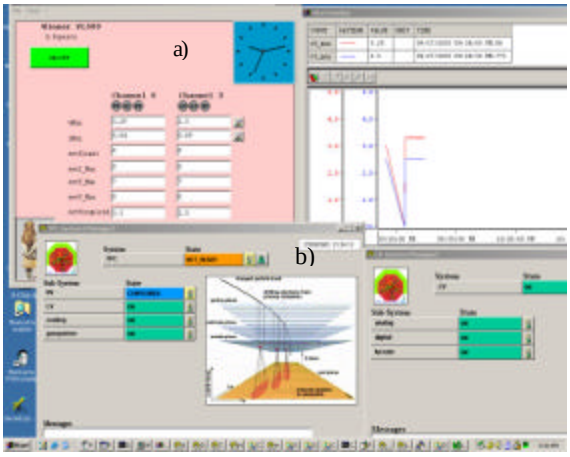

Figure 3: *LV control panels: a) local control, b) FSM control panel*

C. *Temperature monitoring prototype:*

An important requirement for the ALICE TPC detector is the temperature stability over the whole TPC volume; the aim is to achieve a stability of 0.1 ºC over the sensitive volume [1]. The main heat sources in the drift volume are the TPC Read-Out Chamber electronics and the Resistor Rods for the drift field. A cooling strategy has been defined and a cooling system for the ROC is being designed. A small test system has been build to validate the strategy. In order to have a very fine temperature monitoring, the aim was to achieve a resolution of approximately 0.01 ^{0}C in the temperature readings. Two solutions, (an industrial and an "in-house") have been tested and compared: the *WAGO* µPLC [11] and the ELMB (Embedded Local Monitor Box) [12]. The *WAGO* µPLC is an industrial solution for which two modules have been tested and compared. The ELMB is a plug-on board developed by the ATLAS collaboration, for different front-end control and monitoring tasks. It is implemented as a CanBus node and has the advantage of being radiation resistant (~ 5Gy and 3*10^{10} n/cm^2 for 10 years) and magnetic field tolerant (up to 1.5T). After comparative tests, ELMB was chosen as preferred solution for temperature reading due to a higher resolution (0.003 ^{0}C, compared to 0.1 ^{0}C of *WAGO*), and a significant lower price per channel (more than a factor of ten compared to *WAGO*).

One of the most important tests was to measure the heat transfer from the FEC to the pad plane, situated at the edge of the gas volume, with electronics operating at the nominal value of the power consumption.

A test set-up was built in order to do this precise measurement. For the tests one IROC (Inner ROC) was installed in a thermal box, which had a very constant (controlled) temperature of approximately 15 ^{0}C (see Fig.4).

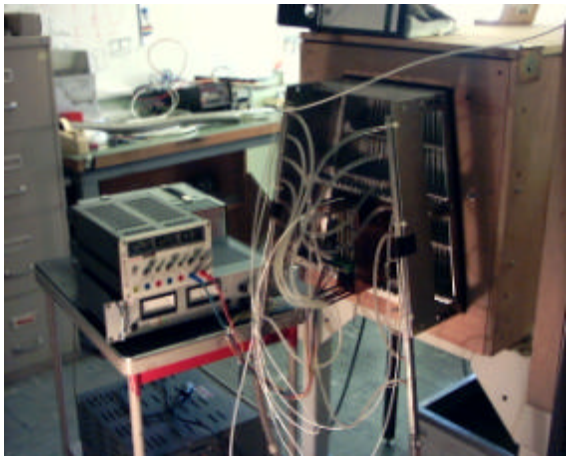

Figure 4: *IROC test set-up in the thermal lab.*

Two cooling circuits were used in this set-up: a cooling circuit for the FEC and a cooling circuit for the IROC. The temperature set point for the cooling circuits was 15 ^{0}C. Temperature sensors were glued on the pad plane, behind the FEC connected to the pads with flat cables and others were glued at 10 cm distance from the FEC connections. More sensors were installed on the aluminium body of the TPC chamber and on the input and output cooling pipes. All sensors used were PT1000 2wires, and were connected to ELMB AI (Analog Input) ports. The OPC20CanOpen ELMB server was used to connect to the PVSSII control application. The sampling frequency in data taking was 2 seconds, and the conversion from ADC voltage measurements to temperatures was done in PVSSII.

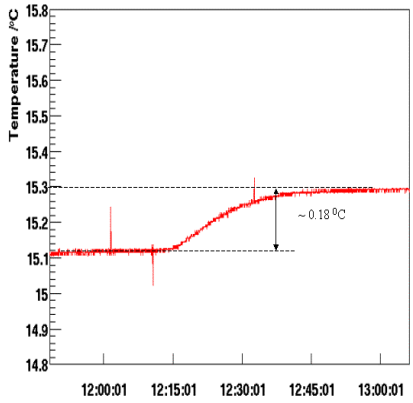

Figure 5: *Heat transfer from FEC during powering up.*

The measurements (Fig.5) showed that during the powering up of the FEC, the temperature on the pad plane, behind the FEC's connection, increased with approximately 0.18 ^{0}C. A relaxation time of approximately 30 minutes was measured, independent of cooling flow, while all cooling circuits are working. These numbers are important input parameters for the PID regulation loops which will be implemented for the cooling circuits.

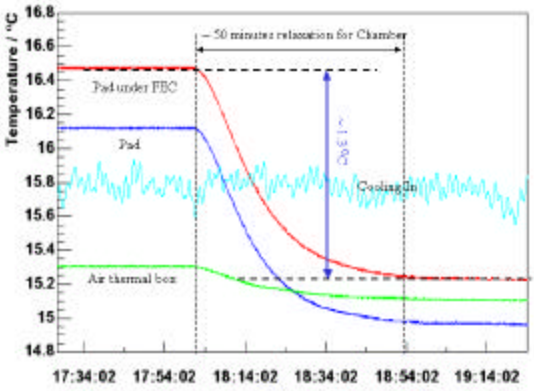

Figure 6: *Temperature variation while switching off the IROC cooling (see "Pad under FEC" curve)*

The influence of the chamber cooling on the pad plane is measured to be approximately 1.3 ^{0}C and the relaxation time for the chamber if the cooling is stopped is of approximately

50 minutes. This is an important parameter to know for the operation of the ROC during the shutdown and start-up periods. It was seen that the pad plane is sensitive to the change in the environmental temperature.

D. Finite State Machine prototype

The DCS models the operation of its subsystems and devices as a hierarchy of FSM [3]. The FSM prototype developed for the TPC was designed to control and monitor the High Voltage, Low Voltage, and Temperature. It will be used during the TPC sector test that will take place in April 2004.

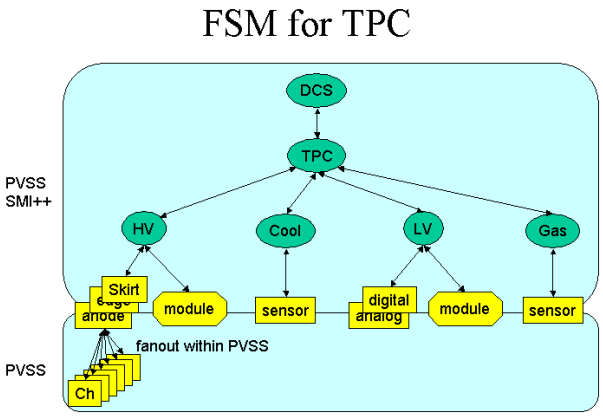

Figure 7: *FSM design for the TPC*

The prototype was designed to be very flexible to accommodate future changes (i.e. include Gas system, Cooling plant etc.). It was developed using the PVSSII scripting tool. The partitioning was done, having in mind the operation of the TPC, so HV and LV channels were grouped according to their functionalities, in so called Control Units. So for example, HV channels that are powering the Anode wires of the TPC ROC were grouped in a control unit: Anode. The same for Skirt wires, Edge, Analog and Digital chamber LV, as you can see in the figure 8.

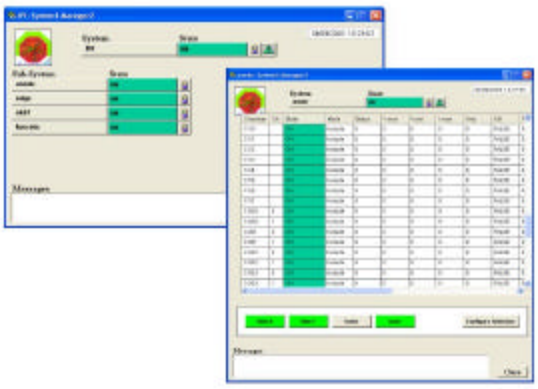

Figure 8: *FSM operational panels for TPC High Voltage*

The TPC FSM prototype allows to exclude/include channels or group of channels. It is possible to configure a channel or a group of channels, manually or through a database. "Writing to" and "Importing from" a database using simple ASCII files was simulated. Three state diagrams were designed, one for a HV channel, one for a group of HV channels and the last one for a group of different groups of HV channels. The Command/State interface between different hierarchical layers, based on these three state diagrams was implemented and operated. The prototype was operated with 16 channels connected to hardware and 100 channels simulated.

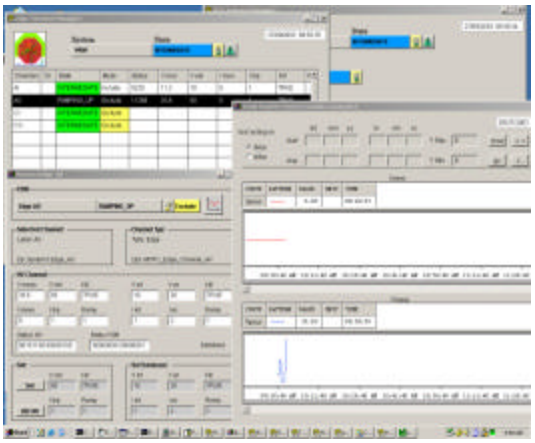

Figure 9: *FSM operation of HV edge channels during ramping –up.*

The prototype performed well (see Fig.9) during the operation of these 16 channels connected to the real hardware (*Iseg* HV module EHQ F025p) and also for the simulated channels. Connection with a fully loaded crate will be done in the near future.

IV. CONCLUSIONS

Control slices for HV, LV and Temperature Monitoring were prototyped and validated for the ALICE TPC Read-Out Chambers. The temperature-monitoring set-up allowed comparative tests to select a preferred solution from several options (industrial and "in-house" hardware).

The High Voltage prototype was included and operated successfully in the TPC Finite State Machine for 16 channels connected to hardware and for 100 channels simulated.

The other FSM prototypes will be connected to hardware in a near future. An important step is to use the final operational prototype in the TPC sector test beam, which will take place in April 2004.

All control slices were tested with detector equipment. The control principle and hardware choices were verified and we are confident that these choices will cover the needs of the full TPC control system. As these solutions are applicable to other sub-detectors it represents an important step towards a homogenous control system for the ALICE experiment.

V. REFERENCES

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