A 20 ps TDC readout module for the ALICE Time of Flight system: design and test results.

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Abstract

The ALICE Time-of-Flight (TOF) system will be a large area (140 m^2) detector made by Multigap RPC (MRPC). A VME TDC Readout Module (TRM) hosting each 30 High Performance TDC chips (HPTDC) will perform the time digitisation. Tests carried out on various board prototypes towards final TRM design are discussed, emphasizing the optimization of the effective time resolution of the chip when working in its Very High Resolution Mode. Lab bench tests and tests beam results are presented, showing that a 20 ps resolution has been achieved.

I. INTRODUCTION

The Time-Of-Flight (TOF) detector of the ALICE experiment [1,2] has to provide particle identification information in the momentum range between 0.5 GeV/c and 2.5 GeV/c in the central region ($|\eta|\leq 1$) through precise time measurements of pulses induced by particles crossing the MRPCs. Physics goals of such detector dictate demanding requirements (<100 ps time resolution). In this context the choice and optimisation of the time digital converter are critical to maintain, starting from an excellent intrinsic time resolution of the MRPC itself (≈50 ps) [3], the required detector performances and global time resolution.

This paper describes the design of the TDC Readout Module (TRM) of the experiment and the R&D work carried out during last two years with various board prototypes to fix its main parameters. After a description of the TRM conceptual design and of the ASIC chip used as time digital converter (section II), in section III we describe the main tests carried out, underlying the consequences for the final card and its deployment in the experiment.

II. THE TDC READOUT MODULE

A. The time to digital converter

The TRM is based on a High Performance TDC (HPTDC) ASIC [4], developed by CERN/EP Microelectronic group for LHC applications, with multi-hit and multi-event capabilities. The ASIC provides relative time measurement of each hit at external trigger arrival. With a dynamic range up to 102 μs, it can work in four different resolution modes. When used in its Very High Resolution Mode (VHRM, 24.4 ps LSB), as in the TOF case, the ASIC integrates 8 channels per chip. In the lower resolution modes (from 800 to 100 ps LSB) 32 channels per chip are available. The time digitization is based on a clock synchronous counter and a DLL interpolator. The external 40 MHz clock is internally multiplied by a PLL to feed properly the DLL to reach the required resolution. To achieve the 24.4 ps bin size, an adjustable RC delay line is used, interpolating the measurement of the same hit made by four different channels. It is relevant to remember, for TOF use, leading and trailing edge detection capability of the HPTDC, as well the use of LVDS inputs.

B. The ALICE TOF readout system

The TOF detector consists of an array of detector elements that are long strips with an active area of 7x120 cm^2. Each strip is read-out by 96 pads each. It surrounds the central interaction region of ALICE with a total of 18 azimuthal sectors, filled by MRPC strips, at 3.7 m from the beam pipe. Each sector will have 8736 readout channels, for a total of 157248 channels. Front-end cards are based on a custom ASIC, which implement a fast amplifier and discriminator. Output signals are shaped to provide a time over threshold (TOT) information. The signals are then transmitted via 5 to 8 m long cable to the TDC readout modules placed in two custom VME64x crates – 12 slots each - positioned at the end of both sides of each sector. A VME master card in each crate will provide readout and the needed interface with the experiment (TTC and DDL as well DCS).

C. The TDC card

A conceptual design of the TRM is shown in Fig. 1. The card, a VME slave card, will host 30 HPTDC, organised in two separate 32-bit parallel readout chains. An FPGA (typical dimension ≈ 100,000 gates) will act as readout controller and implement also the VME interface (these two functions are separately shown in Fig. 1).

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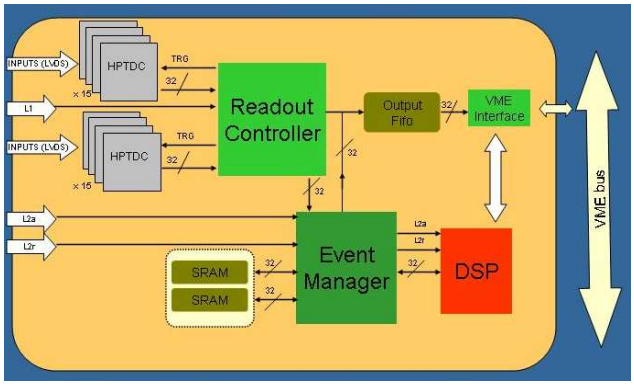

Figure 1: Conceptual design of the TRM

At L1 arrival, distributed to each HPTDC as trigger tag, the controller will move matched hits from HPTDC readout FIFO to two coupled SRAM, handled by an event manager (implemented by a separate FPGA). This will mimic a dual port RAM. In this way, the readout doesn't need to stop when data are transferred to internal memory of the DSP for further processing. Finally an L2a signal will start transfer from DSP to output FIFO. An L2r assertion will allow the DSP to discard the relevant event.

The DSP will provide online data correction for Integral Non Linearity (see III.A), data packing (leading and trailing edge information, which are stored in two separate 32-bit words by the HPTDC, when working in VHRM, will be packed just in a 32-bit word), and data monitor at first level trigger. Actually the DSP will be the unique component of the detector able to access and monitor MPRC data at first level trigger, providing useful online information for detector debug and data quality monitor. Collected data statistics will be periodically inserted inside data stream through the output FIFO. Finally the DSP is expected to trace error conditions signalled by the HPTDC (notably SEU auto-detections inside internal buffers) and to proper react through the JTAG interface of the chips.

A conservative expected bandwidth required on the bus, according to simulation with 8000 charged particles per unit of rapidity, taking into account central DAQ requirements and pessimistic assumptions on MRPC occupancy, is 16 MB/s, which doesn't pose problems on a standard VME bus.

The proposed architecture is highly flexible and it will allow during the life cycle of the experiment firmware refinements if needed, depending on changing conditions inside the experiment as well during detector commissioning. Some of the functions of the DSP could be transferred to the FPGA; the VME interface could be improved to implement 2eVME protocol, etc. Firmware upgrade will be made possible through the VME bus.

III. PROTOTYPE CARDS AND TEST RESULTS

A. *The test cards*

To test and qualify the HPTDC chips, tailor properly the proposed TRM design and develop needed firmware, a set of prototype cards was built, trying to separate HPTDC issues (e.g. achievable time resolution) from development of readout, data processing and trigger interface.

We designed a slave prototype card, shown in Fig. 2, hosting 4 HPTDC. The card, in 6U format, is read through a private 32 bit LVDS bus implemented on P2 connector and controlled through a front-panel 20 pins control bus. We use parallel readout of the chain of the four HPTDCs (a master-slave scheme was selected). The on board Altera MAX PLD is mainly responsible to handshake JTAG commands with the HPTDC chips for programming. Through different iterations and improvements, we prepared three versions of this card.

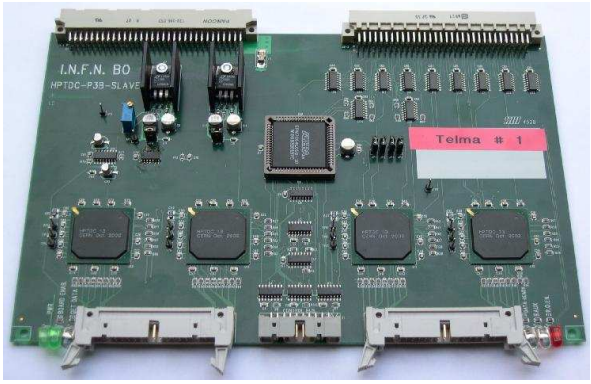

Figure 2: The HPTDC slave card.

The master card is a 6U VME slave card, which can control up to four HPTDC slave cards. It has on board clock (as well the possibility to receive it as an external input), an Altera APEX FPGA EP20K100, a 32 bit Sharc Analog Device DSP (ADSP 21160M), two FIFOs (one to store data collected from slave cards, the other as output FIFO visible from VME) and Flash memory resources (to store DSP boot code, as well needed look-up tables). In practice, almost all the functionalities that will be implemented in the final TRM card can be tested using these couple of cards. A previous version of the master card was initially built, without the DSP.

B. *Integral Non-Linearity and Time Resolution*

In its high resolution modes (98.6 and 24.4 ps LSB) the HPTDC showed, as firstly reported in [5], a typical integral non-linearity pattern, spanning over the 25 ns cycle of the 40 MHz clock. Non-linearity performances can be easily achieved through a Core Density Test. To characterize the VHRM response, we normally use a 1,024,000 random hits sample, allowing in the collected DNL distribution, from which INL information are then obtained, a statistical error of the order of 3% in each bin. A devoted DAQ chain to monitor the INL was set-up, making use of a 32-bit LVDS I/O (Struck SIS3601). Despite various attempts done to improve the situation at hardware level by the CERN EP/MIC group (use of a lower inductance package, improved distribution of the power supply) or at programming level (DLL tap adjusts can be applied), even in the last release of the chip the INL pattern is still clearly present. Actually the main source of the INL was identified coming from on-chip crosstalk from logic part of the chip through the power supply.

The INL pattern resulted very stable and moderately chip dependent. We found there are also external parameters affecting it, in particular the applied core voltage (we tested it from 2.3 to 2.7 V), as well as, obviously, the quality of the input clock feeding the DLL. Periodic measurements checked that in stable external conditions the pattern results essentially unchanged. To overcome the problem, the application of an INL compensation scheme through look-up tables (LUT) was a straightforward choice. Even if a sort of "common" pattern can be identified, extensive checks showed that the best correction is always achieved with a per channel LUT. Given the extent of the correction (typically +/- 4 bits in the worst cases) 1 kB is needed to store the LUT for one channel.

The time resolution of the device was tested through cable length measurements, using different delay lines over the 25 ns cycle. The RMS of the measured distribution, divided by the square root of 2, is a measurement of the achievable single channel resolution. Fig. 3 shows measurements for 8 couples of channels for various delays. The theoretical statistical limit of the converter (LSB/√12) and the requirement for the TOF are also shown. A resolution better than 25 ps is reached after applying INL compensation. In this case the two HPTDC under test were located in two different slave boards. Therefore, a contribution to the resolution coming from the distribution of the clock to different boards is also present.

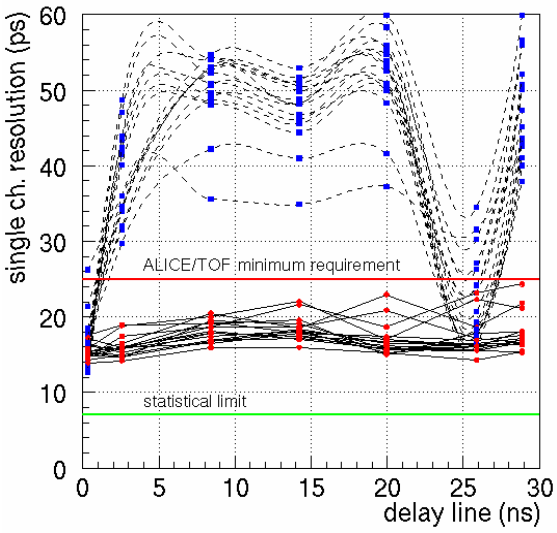

Figure 3: HPTDC single channel resolution estimated through delay line measurements (squares, blue, dashed: without INL compensation; bullets, red, continuous: with INL compensation).

To further improve the effect of the INL compensation a more refined approach was also tested. The basic idea is that, despite the converter has a bin width of 24.4 ps, we know the INL pattern with a better granularity. With a small overhead it is possible for example to add two bits of information (that is use bins of 6.1 ps) to correct INL pattern. The effect on time resolution is shown in Fig. 4 (in this case the two HPTDCs under test were located on the same board). Paying a small penalty of larger LUT tables and lower TDC dynamic, it is worthwhile to note that a resolution around 15 ps for all channels was reached.

Taking into account other assumed contributions to the global time resolution of the detector from the MRPC itself plus the front-end card (50 ps), from the t_o determination (50 ps) and the clock distribution (15 ps to the crate and 10 ps inside the crate) [2], the HPTDC contribution between 15 and 20 ps, as measured from test cards, sets the total detector resolution below 80 ps.

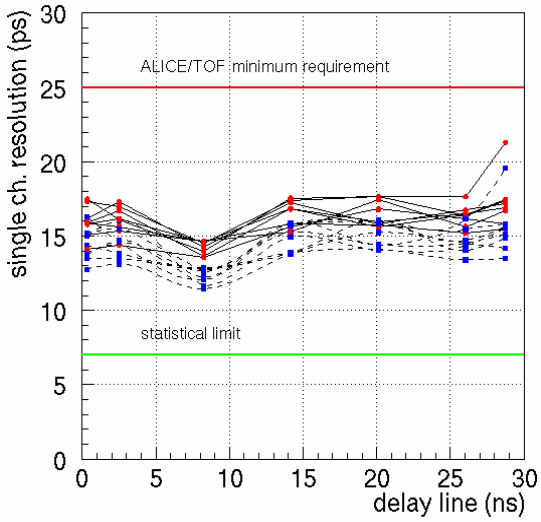

Figure 4: HPTDC single channel resolution applying standard INL compensation (bullets, red, continuous) and refined INL compensation (squares, blue, dashed).

C. *Time Over Threshold Capability Check*

The TOT signal from front-end cards gives, with the leading edge, the time of the hit and, with the width, an equivalent measurement of the amplitude. Slewing corrections are then applied according the measured width. In this context it was important to assess the minimum time between two consecutive measurements. Fig. 5 shows the fraction of "complete" pulses (both leading and trailing edges detected) for different pulse widths.

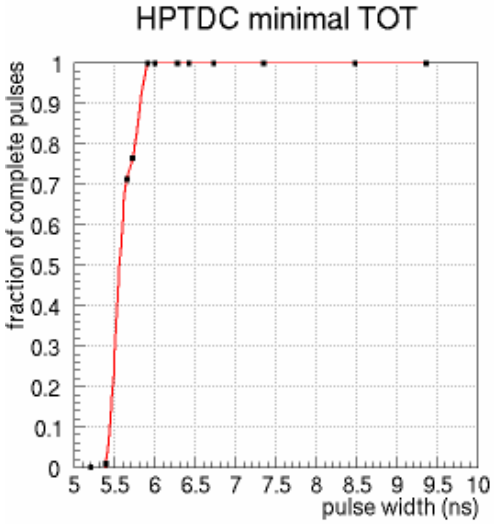

Figure 5: Fraction of complete pulses (leading and trailing) detected by the HPTDC as a function of the pulse width.

The inefficiency (that is missing trailing edge detection) was found to appear very sharply just below 6 ns as expected. The final front-end ASIC will stretch TOT pulses according these measurements, to ensure trailing edge detection, but minimizing dead time of the single TDC channel.

D. Test Beam Results

Since May 2002 the HPTDC prototype cards were tested also during tests beam at CERN PS, to check their performance when connected to real MRPC signals and to monitor performance stability. Signals were splitted in such a way to allow comparison between measurements performed with standard electronics (CAMAC LeCroy TDCs) and with the HPTDC. Delay lines measurements were also simultaneously done to monitor independently stability of the resolution during the runs. The measured time resolution of the MRPCs under test was found fully compatible (as seen in Fig. 6), confirming time resolution of the converter estimated with the described lab benchmarks.

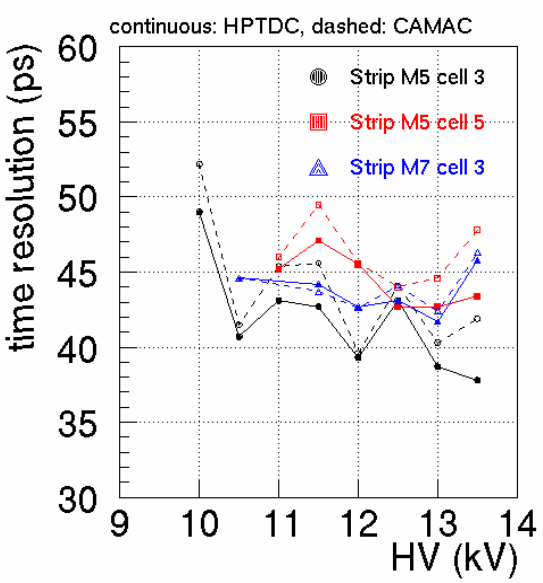

Figure 6: MRPC time resolution measured in different pads with standard electronics and with the HPTDC.

E. Crosstalk measurements

Having in mind the final detector and its huge amount of channels, a major investigated concern was the shift on a measured difference of time between two signals, generated at ASIC level by crosstalk from another firing channel. To mimic as much as possible the final set-up, we measured the fixed time difference (obtained by means of a delay line) between two signals, digitising them in two separate chips. A noise signal was then injected in the other channels of the chip measuring the start signal, at various time distances from it. All the signals used had 10 ns width, with leading and trailing edge detection enabled. At 20 ps level it is really difficult to build a "noise free" set-up for this kind of measurement. To isolate the contribution of the chip, two sets of measurement (shown in Fig. 7) enabling and disabling by software the noisy channel were done. Even if a small perturbation when the HPTDC channel receiving the noise signal is enabled is present (when the time from noise to signal is between –10 ns and 0 ns), the effect has been satisfactory checked to be within 1 LSB over all channels tested.

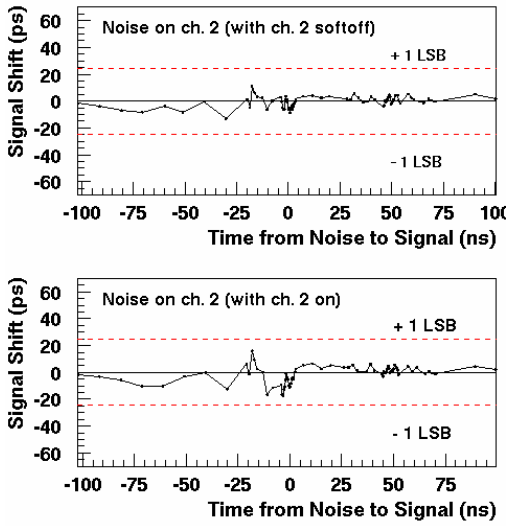

Figure 7: Signal time shifts measured as a function of the distance of the signal in another HPTDC channel.

In MRPCs there is a distinct probability to observe signals in two neighbouring pads when particle hits the pad boundary, due to a charge sharing effect. At the same time near the boundary, due to a smaller collected charge, the resolution is normally worse [2]. We checked if the HPTDC is introducing additional contribution to this effect due to crosstalk during test beam by means of a beam scan. As can be seen in Fig. 8, even with 20% efficiency and the neighbouring pad having more than 90% efficiency (that is a "noise" signal is always present) the resolution is still below 80 ps, as measured with standard electronics.

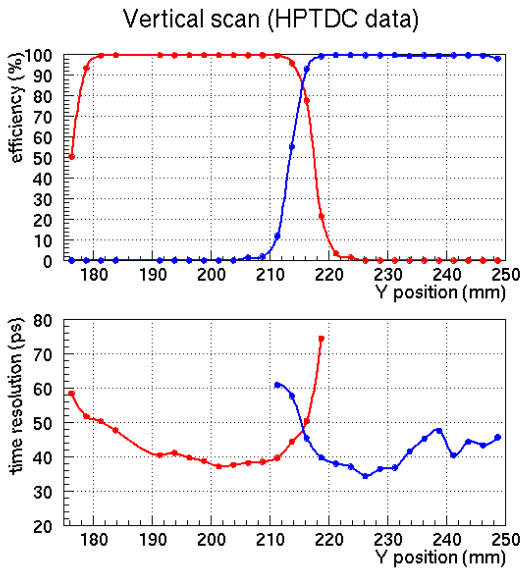

Figure 8: Efficiency and time resolution in two neighbouring pads as a function of beam position.

F. Environmental Conditions Testing

1) Magnetic field

The readout crates will be placed inside the ALICE magnet and will operate in a magnetic field up to 0.5 T. Even if an influence of the magnetic field is not reasonably expected, we tested an HPTDC slave card in magnetic field up to 0.5 T at INFN Legnaro laboratories. During a three hours intensive test no error was detected. We checked also that the INL pattern is not modified at different magnetic field values.

2) Radiation tolerance

The ALICE TOF readout system will operate in a moderate hostile environment for what concerns levels of radiation. A total dose of 0.3 Gy is expected in 10 years, with a total neutron fluence of $2 \cdot 10^9$ cm^{-2} with energy above 20 MeV [6]. The HPTDC was not implemented in a technology guaranteed to be radiation hard and SEU insensitive, nevertheless it has self-checking built-in mechanisms enabling it to auto-detect SEU occurrences. The CMS group, which is using the HPTDC for readout of muon barrel drift chambers, tested at CRC facility at Louvain the HPTDC for SEU, irradiating it with 60 MeV protons. Extrapolating their measurement [7], taking into account the different radiation levels and the number of HPTDC used, we expect just a total rate of 1-2 SEU per day in the whole detector. By the end of 2003, we will moreover characterize the SEU threshold of the device irradiating it with heavy ions at SIRAD facility [8] at Legnaro, complementing the existing measurement.

A final irradiation campaign is foreseen in 2004 to test other components used in the TRM not yet tested. However, using 0.25 and 0.18 μm CMOS technology for FPGA and DSP and taking into account the "low" level of radiation, we expect an acceptable rate of SEU to be handled by the card.

IV. The Final Layout

Having tested functionalities and performances of the HPTDC, we are now planning the final layout of the 240 channels card. On the basis of the experience gained during last years, taking into account our front-end modularity and the need to reduce card complexity and to simplify its maintenance, 10 piggy back cards, plugged on both sides, hosting 3 HPTDC and local voltage regulator each will be used. In the central main board, the use of ACEX EP1K100 as FPGA and ADSP 21160N as DSP is now foreseen. The card will be equipped with 4 Mbits flash RAM for LUT tables and DSP code, latch-up protection systems as well redundancy and watchdog mechanisms to react properly to SEU events.

V. Conclusions

The HPTDC has been thoroughly tested and qualified for ALICE TOF use in its Very High Resolution Mode. It was shown that, after applying INL correction, a 20 ps resolution is achieved.

Building "bricks" of the final TRM card have been tested, as well its key functionalities. The definition of the layout of the card and the choice of its components is now in an advanced stage.

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VI. References

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