High speed parallel optical links for the LHCb muon trigger

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Abstract

The principles retained to transport binary data between the muon detector and the muon trigger for the LHCb experiment is based on the serialization of the binary detector data ; the use of optical links ; and the use of high integration optical devices.

In this paper, we describe the designed optical link. In section 2, we demonstrate that the chosen devices allow high speed data transfers with a very low bit error rate. In section 3, we present the clock jitter filtering system designed to make the TTC clock compatible with high speed link requirements. In section 4, we describe the experimental set-up designed to characterize this high speed parallel optical link and we give the results obtained with this test bench.

I. DESCRIPTION OF THE HIGH SPEED PARALLEL OPTICAL LINK

The basic element to transfer data between the muon detector electronics and the muon trigger is the parallel optical link shown in Figure 1. It contains 12 channels running at 1.6 Gbit/s.

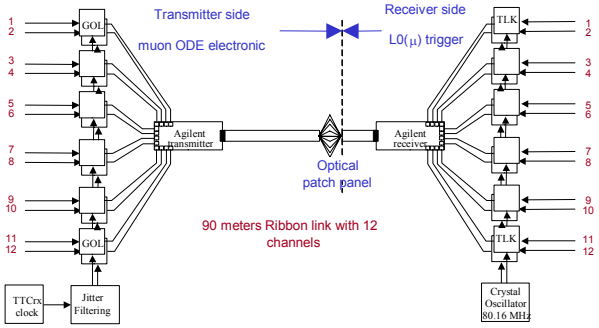

Figure 1 : Overview of Parallel Optical Link

In the transmitter side, we have :

- Twelve serializer chips. Each one converts 32-bit data word into a serial signal at 1.6 Gbit/s ;
- One parallel optical transmitter driving 12 optical links at 1.6 Gbit/s ;
- One jitter filtering circuit generating a low jitter clock compatible with the requirements of the high speed communications.

In the receiver side, we have :

- One parallel optical receiver runing at 1.6 Gbit/s ;
- Twelve deserializer chips recovering the original 32-bits data words from the high speed signals.

The optical modules are designed to operate on multimode fiber at a nominal wavelength of 850 nm.

After 90 meters, the optical ribbon cable is broken out in 12 individual fibers connected to a patch panel. In the other side of the patch panel, 12 individual optical links are merged into a ribbon cable connected to the muon trigger. This optical distribution is required to group data coming from different stations.

In the muon trigger, we have to integrate up to 24 deserializers in one 9U board. Thus, a low power consumption device is required. The power consumption is less than 300 mW for each TLK250 device, less than 1.5 W for the optical transmitter and less than 2.7 W for the receiver.

Our experimental set-up is based on : the TLK2501 from Texas Instrument for serialization and deserialization ; and the parallel optical devices from Agilent (HFBR712 and HFBR722) for optical emission and reception. In that set-up only one channel was equipped over the twelve.

In the emission side, it is possible to replace the TLK2501 by the GOL chip developed by the CERN microelectronic group. This device uses the same transmission protocol (8B/10B) as the TLK2501. It has been designed to be less sensitive to radiation effects [1].

II. ESTIMATION OF THE THEORETICAL BIT ERROR RATE

Good design practices in digital communication system consists in maximizing the bandwidth while minimizing the bit error rate.

The bit error rate depends on optical attenuation, jitter of serial data and on external system perturbations such as electromagnetic interference.

A. Optical power attenuation

The maximum power attenuation allowed for an optical link is called the loss budget. It is the sum of losses due to the length of optical fiber, connectors and splices.

The attenuation coefficient for the multimode 850 nm fiber is 3.75 dB/km. Each connector pair introduces an attenuation of 0.75 dB and each splice an attenuation of 0.3 dB.

The typical distance between the muon detector front-end electronics and the muon trigger processor is 100 meters. We have 2 pairs of connector per link and 2 splices corresponding to a loss budget of 2.5 dB.

On the other hand, the minimum optical transmitter power is -8 dBm and the minimum receiver sensitivity is -16 dBm [3]. Thus, the power budget is equal 8 dB in the worst case. We have a margin of 5.5 dB making the attenuation effect on the bit error rate negligible. In the rest of this note, we will only consider the jitter effect.

B. Jitter issues

The choice of devices for an optical link is not arbitrary. We can select devices specified to work individually at a rate of 2.5 Gbit/s. But when components are chained together, the jitter cumulated along the chain might reach an unacceptable level. Thus, we have to select individual components keeping in mind the jitter budget for the whole chain.

The time duration of one bit is called the unit interval (UI). The jitter budget is defined as the time allocated for one bit of data : 400 ps at 2.5 Gbit/s and 625 ps at 1.6 Gbit/s.

If the overall jitter of the chain is above the unit interval, the received data will be corrupted.

Jitter is divided into two fundamental types, called random and deterministic jitter.

Random jitter (RJ) is unpredictable and has a Gaussian probability density. It is caused by thermal or noise effects. Random jitter is normally described in term of the standard deviation value σ. The ratio α of the peak to peak value to standard deviation depends on the bit error rate required by the system as shown in Table 1. For example, if a bit error rate of 10^{-12} is required, the peak to peak value of the random jitter (RJ peak-to-peak) is 14 times the standard deviation.

Table 1 : Gaussian waveform probabilities

BER	10^{-9}	10^{-10}	10^{-11}	10^{-12}	10^{-13}	10^{-14}	10^{-15}	10^{-16}
α	12	12.72	13.41	14.07	14.7	15.3	15.88	16.44

Deterministic jitter (DJ) is caused by components interaction in the system especially the effect of limited bandwidth on specific patterns of 1 or 0 in the bit stream. Deterministic jitter is always described in term of peak to peak value.

Total jitter (TJ) is the combination of all random jitter and deterministic jitter components. In order to compute the total jitter, RMS value for the random part is converted to peak to peak values. The total jitter is given by the linear sum of the peak to peak values of random and deterministic jitter.

C. Jitter budget of our configuration

When the overall jitter exceed the unit interval, the clock can not be extracted properly and the data transmitted contains a excessive number of errors. For this reason, it is necessary to check that the jitter budget of the chain does not exceed the critical value.

To obtain the total jitter we add linearly the deterministic jitter components and quadratically random jitter components.

Table 2 : Optical Link jitter Budget calculation

System component	Total jitter (ps-p-p)		Deterministic jitter (ps p-p)		Random jitter (ps p-p)	
	TJ(UI)	TJ(ps)	DJ(UI)	DJ(ps)	RJ(UI)	RJ(ps)
Serializer	0.13	80	0.06	40	0.06	40
Optical transmitter	0.21	132	0.1	60	0.12	72
Fiber added	0.13	80				
Optical receiver	0.24	153	0.07	46	0.17	107
deserializer	0.58	361				

Table 2 shows that the total jitter is 0.58 UI at the input of the deserializer. This corresponds to an opening eye diagram of 0.42 UI which is better than the 0.4 UI required by the deserializer for clock recovery. Thus, we conclude from this evaluation that the optical link has a bit error rate lower than 10^{-12} at 1.6 Gbit/s in the worst case when the jitter of the input clock is lower than 40 ps.

III. TTCRX CLOCK JITTER FILTERING

The input clock must be jitter free as much as possible in order to minimize jitter introduced into the high speed clock and latter in the high speed data stream.

For the TLK2501 the jitter of the input clock has to be lower than 40 ps peak to peak to guarantee an acceptable bit error rate [2].

The 40.079 MHz bunch clock output provided by the TTCrx has a jitter of about 300 ps peak to peak [9]. Such a jitter does not match requirements of a high speed optical link. Thus, the TTCrx clock can not drive directly any serializer or deserializer running at 1.6 Gbit/s. The bit error rate measurements for the link driven by TTCrx clock confirm this : we obtained a value of 10^{-3}.

A. Jitter filtering technique

The most common technique to filter jitter is shown in Figure 2. It uses a narrow bandwidth phase locked loop which is locked to the incoming reference clock.

To reach a value of jitter as low as 40 ps peak to peak, we must use a voltage controlled crystal oscillator (VCXO) with a very low phase noise.

The jitter filtering circuit implemented in our set-up is based on the Maxim PLL device(MAX3670) [4]and low phase noise VCXO (CTS333) [5].

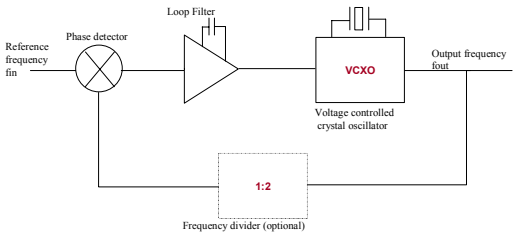

Figure 2 : Narrow bandwidth PLL based on the VCXO for jitter filtering

This filtering system is based on only commercial devices. It would be replaced by the QPLL ASIC designed by the CERN Microelectronic group using radiation tolerant layout practices to meet the LHC radiation requirements [6].

B. *Clock distribution to several devices*

In our system, we have to distribute a clock with a very low jitter. The clock distribution system shown in Figure 3 is designed to preserve this low jitter.

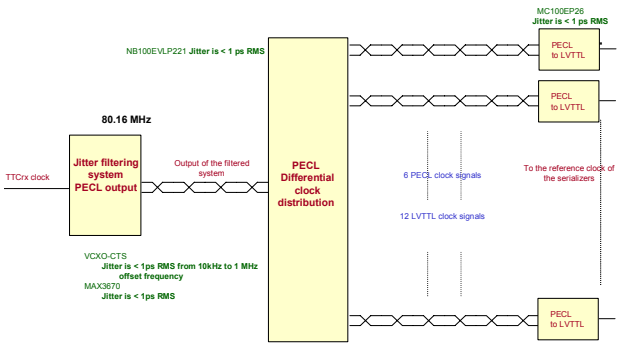

Figure 3 : clock distribution technique

We use PECL logic to produce fast rise and fall times. The output signal with a fast transition time around the transition region is well suited to minimize the jitter.

The NB100EVL110 clock distributor from Onsemiconductor adds in the worst case a jitter of 1 ps RMS.

If we assume that the clock at the output of the TTC filtering system has a jitter of 4 ps RMS, the jitter of the clock at the input of the serializer will be below 4.3 ps RMS.

IV. Experimental Results

The test bench designed to characterize the optical link allows to estimate the bit error rate of the optical link. We use two methods to estimate the bit error rate of the optical link:

- The pattern generator method
- The eye diagram display method.

1) *Pattern generator method*

The pattern generator method is shown in Figure 4.

In the transmitter side, the FPGA is programmed as a 2^{31} - 1 pseudo-random data generator. It is driven at 80 MHz and generates 16 bits parallel data.

In the receiver side, these data are then compared to the same pseudo-random generator as the one implemented on the transmitter side.

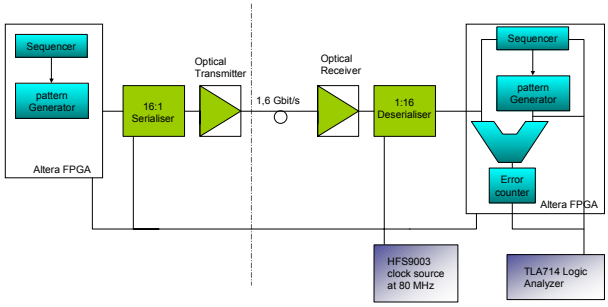

Figure 4 : Optical link test board and bit error rate estimation method

The bit error rate is thus given by $BER = \frac{N_C}{N_T}$, where N_C is the number of words corrupted and N_T is the total number of words transmitted at 1.6 Gbit/s.

If the mean time between errors is one hour, the bit error rate is 3.47×10^{-12}. Measuring a bit error rate at a level of 10^{-14} requires to run the link during several weeks.

To reduce this time or to access to a lower bit error rate, we use another method based on the eye diagram display.

2) *Eye Diagram and jitter measurement method*

The performance of the optical link is often evaluated using the eye diagram display. The quality of the eye diagram depends on the input signal and on the trigger source.

The most precise technique is to trigger the oscilloscope with a clock at the same speed as the serial bit rate. Unfortunately, this clock is not accessible in the TLK2501 deserializer. For this reason, a specific clock recovery is included in some oscilloscope.

We take the 80 MHz clock used for serialization since we do not have such equipment. This clock used as trigger can provide inaccurate results if it exhibits itself some jitter. We have to take care to use a low jitter clock. In addition, we have to use random patterns in order to obtain a complete eye diagram.

Measuring the opening of the eye diagram at the input of the deserializer, gives access to a quantitative estimation of the bit error rate through the measurement of the RMS value of jitter.

B. *Measurements of the bit error rate*

Figure 5 shows the test bench built to characterize the high speed optical link where the logic analyzer (TLA714) is

running in transitional mode to capture the errors. It is possible to store all errors with a corresponding time stamp.

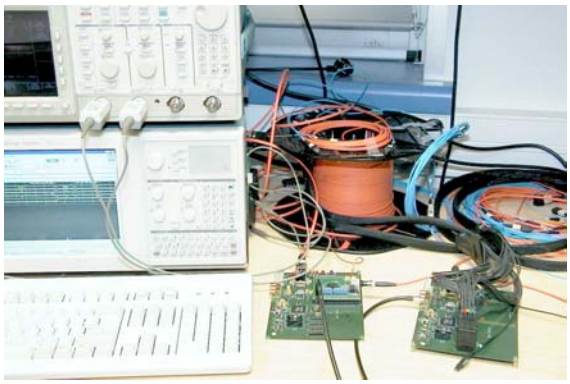

Figure 5 : Optical link test bench

C. Bit error rate in standard conditions

The link prototype was tested using the pattern generator method, from bit rate of 1.6 Gbit/s to 2.5 Gbit/s. At 1.6 Gbit/s, the test was done continuously during 10 days without errors. Over 1.3×10^{15} bits were sent, received and checked by the bit error rate tester integrated in the FPGA. We estimate the bit error rate below 10^{-14}.

D. Sensitivity of our setup to optical attenuation

Figure 6 shows the bit error rate as a function of the optical power at the input of the optical receiver. We measured a bit error rate of 10^{-13} when the optical power at the receiver input is –26.5 dBm.

In normal operation, this optical power is -12.4 dBm when the fiber length is 100 meters. Thus, the bit error rate of our configuration can be can be extrapolated well below 10^{-15}.

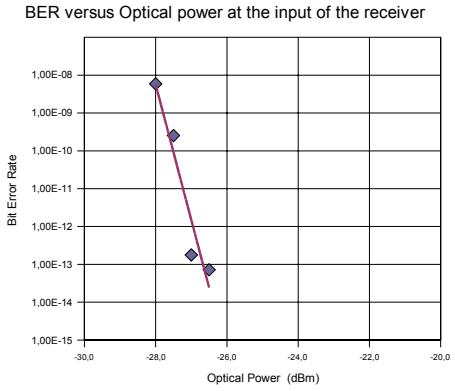

Figure 6 : Bit error rate versus optical power at the input of the optical receiver

E. Experimental results of the jitter filtering circuit

1) Test set-up for clock jitter measurements

Figure 7 shows the test set-up realized to test the jitter filtering circuit. The TTCrx mezzanine board was installed on our prototype board. The 40 MHz TTCrx clock drives the jitter filtering circuit. The 80 MHz low jitter clock drives the TLK2501 serializer.

Since the jitter analysis has to be very precise, we use the TDS694C oscilloscope including a specific software (TDSJIT1V2). The measurement is based on single-shot jitter and allows to measure an RMS jitter down to 1.5 ps [10].

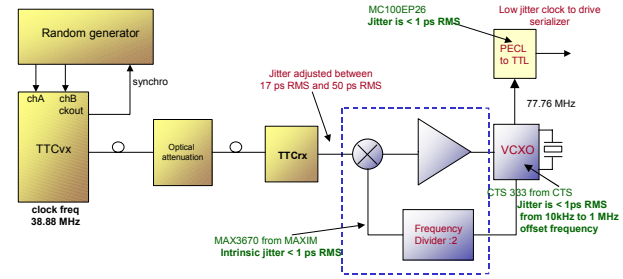

Figure 7 : Test set-up for jitter measurements

The TTCrx module is connected to the TTCvx board through a 5 meter optical fiber.

To vary the rate of jitter, we use an optical attenuator between the TTCvx and the TTCrx boards to adjust the signal level at the input of the TTCrx module and we use a random generator synchronized to the TTCvx to adjust the activity rate in channel A and channel B for the TTCvx module.

For an optical input level at the TTCrx of -38 dBm and a high activity rate in channel A and channel B, the measured jitter is 48.2 ps RMS and 450 ps peak-to-peak.

When there is no broadcast control words and for 5 meters of fiber between TTCvx and TTCrx module without any optical attenuation, this jitter is only 17 ps RMS (~170 ps peak-to-peak).

2) Measurements o f the TTCrx jitter filtering circuit

Figure 8 shows the output jitter versus the input one. The jtter of the filtered clock remains around 10 ps RMS when the TTCrx jitter varies from 17 ps RMS to 48 ps RMS.

Reducing again this value would require to use a very low noise VCXO as the S1559 from Saronix [7]. The jitter of the filtered clock will then be as low as the jitter required by the TLK2501 serializer.

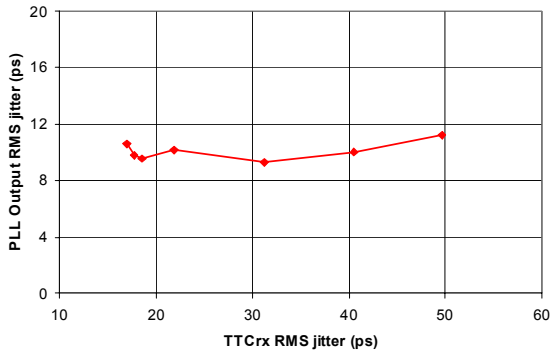

Figure 8 : PLL output jitter versus the TTCrx jitter

F. Optical link driven by the filtered clock

The input clock of the deserializer is now driven by the filtered clock. The link was tested for several hours without errors.

Figure 9 shows the eye diagram measured at 1.6 Gbit/s. The RMS value of the jitter is about 18.6 ps.

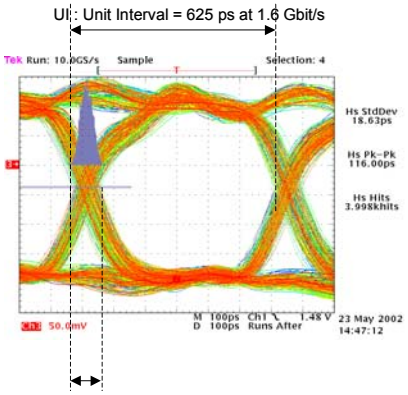

Figure 9 : Eye diagram at the deserializer input

At 1.6 Gbit/s, 0.6 UI corresponds to 375 ps which is higher than 17 times the measured RMS jitter value. This corresponds to a bit error rate lower than 10^{-16} as shown in Table 1.

We confirm that the low phase noise clock is a key parameter to ensure a low bit error rate in the high speed optical links.

V. Conclusion

To design a high speed optical link, we have chosen a set of components that guaranties, in the worst case, a bit error rate lower than 10^{-12}.

To check the robustness of our conception against various perturbations, we have built a test bench setup to characterize high speed optical links.

The results of measurements are the following :

- We are able to transport data with a bit error rate of about 10^{-14} in lab conditions using a low clock jitter ;
- Our design is quite insensitive to power supply variations ;
- The design is very sensitive to the input clock jitter ;
- The level of clock jitter of the TTCrx is not acceptable for a reliable transfer of data (bit error rate is around 10^{-3}) ;
- A jitter filtering solution allowing to use the TTCrx clock has successfully been tested. It allows to obtain a bit error rate around 10^{-16}.

In the coming months, we will design an emission board driving 24 optical links on two twelve way ribbons. Seriliazers will be the GOL chip as well as TLK2501. To filter the TTC jitter we will implement the circuit based on the Maxim chip and the QPLL components. This board will be irradiated to measure the effect of the single event upsets and single event latch up on the parallel optical transmitter.

References

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