Test System for the Front End Chip of the ALICE Silicon Drift Detectors.

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Abstract

In this paper the implementation and performance of the test system for the front-end chip of the ALICE silicon drift detectors (SDDs) are described.

The front-end electronics for the SDDs is based on two ASICs. One of these, named PASCAL, performs the amplification, analog storage and analog to digital conversion of the signals delivered by the detector. The second chip, AMBRA, is a 4-event digital buffer that allows the reduction of the data transfer rate to the data acquisition system. This chip performs also baseline equalization and a first compression of the data from 10 to 8 bits. The test system developed for PASCAL uses commercial instrumentation to operate, program and readout the chip. The chip operation and programming are controlled from a computer by means of a graphical user interface, which furnishes a number of data analysis tools as well.

I. Introduction

The Inner Tracking System (ITS) [1] of the ALICE Experiment [2] will make use of pixel, drift and strip silicon detectors for vertex reconstruction, momentum resolution improvement and particle identification purposes. The two intermediate layers of the ITS will be equipped with a total of 260 large area silicon drift detectors (SDDs). Each one of these detectors has 512 readout channels, adding up to more than 133 thousand channels for the intermediate layers of the ITS.

Since the front end chips for the SDD will be mounted in the particle trajectory (on the same structure as the detector) their design specifications are constrained to very stringent boundaries. In particular, the material quantity allowed in the particle trajectory limits the capacity of the cooling system, which in turns limits the power dissipation of the ASIC's to a maximum of 5mW/channel. Besides, radiation tolerant layout techniques had to be used in the design.

The most recent prototype of the PASCAL ASIC embeds 64 low noise amplifiers, a 64x256 capacitor array for temporal storage of the amplifiers' output samples and 32 10-bit successive approximation ADC's (one ADC converts the samples from two contiguous channels).

The amplifier [3] is a two-stage circuit with a trans-conductance feedback loop in the second stage to fix the DC level at the output. The design peaking time and gain of the amplifier are 35 ns and 40 mV/fC, respectively.

The analog memory [4] samples the amplifier output every 25 ns (40 MHz clock) allowing for a maximum drift time of the charges in the detector of 6.4 μs.

Since the ADC [5] is the larger and the most power consuming component in the chip, it is only activated when a trigger validates the sampled data. This also permits using the same ADC to convert the samples from two channels and thus reducing the total area. In the case of no trigger signal the data is not digitised and the analog memory is overwritten.

This prototype has also a number of testing features, which enable to efficiently explore the most critical functions of the chip. Among them are, for example, we have:

- baseline control of the DC output level of the amplifier via a 9 bit DAC.
- gain control of the amplifier – low, medium and high gain;
- on-chip test pulse generation with programmable amplitude;
- clock frequency divider for the ADC – the ADC can work at full or half frequency;
- ADC reference voltages and critical biases of the analog memory can be supplied externally;
- Critical control logic signals can be supplied externally permitting the control of part of the digitisation process;
- test pads for monitoring several control logic signals;
- independent access to the amplifier, analog memory and ADC of one channel.

Using the JTAG standard four registers can be written to program the gain and baseline of the amplifier, the amplitude of the internal pulse and the channels this pulse is fed to. The DAC's are then used to actually set the corresponding analog values.

The main features the system has to measure are linearity, baseline controllability, noise (both random and common mode), uniformity between channels and chips, cross talk, frequency stability and critical aspects of the performance of the ADC. Since the ASIC integrates on board the ADCs , the signal exchange with it can be purely digital. Taking advantage of this aspect, we built a compact and flexible set-up that makes use only of commercial digital equipment.

II. The Test System

The implementation of our system was guided by two needs; one of them is obviously providing a means of automate the systematic testing of the pre-production prototype. On the other hand, we also intend this system to be the core of a more complex and automated one that would be used for massive chip testing in view of the imminent submission for production of the final version of the chip.

A. System Hardware

Since the chip operation is quite simple we were able to implement the system using standard instrumentation *i. e.* a pattern generator, a logic analyser and a PC for controlling the system and data analysis.

Figure 1 depicts the system hardware implementation. The PC controls the pattern generator and the logic analyser (which are actually part of the same instrument – *16702B* in the figure) via a TCP/IP connection through which data are also sent back to the PC.

The chip operation is controlled directly by the pattern generator. In the other hand, the logic analyser triggers for reading data on the *write request* signal from the chip. In this way one is able to drive the chip operation from the PC through these instruments.

The LVDS board is just a single-ended CMOS – LVDS signalling translator since the chip uses LVDS signals.

Using an interface board serves between the LVDS board and the probe card provides flexibility to the system allowing the interconnection of a test board in its place. In this way one can easily exchange between probe-card and board testing modes. The use of a test board, in which the chip can be mounted, is very helpful since it includes some features the probe card does not, like voltage regulators that supply reference voltages for the ADC.

B. Software

The control of the chip needs only a trigger signal to stop writing the analog memory and to start the conversion. So the sequence of signals needed is quite simple. An overview of the control program is shown in figure 2. The second block serves to write the baseline, amplitude and gain registers whose values are set at the user interface. The block labelled Read Data is not actually inside the loop since data are only acquired when the user gives the command at the PC.

Indeed, since PASCAL has a 20-bit data bus and a small output buffer, data must be read in synchronization with the conversion process. The chip generates a *write request* signal after converting the first sample from each channel and then outputs digital data from two channels at every clock cycle. In this way one can simply make the analyser trigger on this signal and run it independently from the pattern generator's loop of figure 2. Therefore the system control program has only to set the parameters of the second block and assure that the pattern generator is run before the analyser.

The user interface for our system was entirely developed using LabVIEW including the drivers necessary for communicating with the instruments. This graphical interface gives general control of the system and permits to start the procedures for different tests and for analysing the resulting data. From the main panel of the interface several other panels can be open from which measurements can be launched. For example,

- general turn on parameters (power supply, clock frequency, baseline, amplitude, gain register settings);
- baseline and noise calculation;
- common mode calculation;
- linearity plots;
- ADC code histograms;
- frequency stability of the baseline;
- charge cluster analysis tool;
- data storage.

The most time consuming part of any of the measurements is evidently acquiring data. Setting the JTAG registers values takes, actually, the longest time. The user interface must first find the correct place within the pattern generator program to write to, depending on what one wants to set. (The values are serially sent to the chip in the *tdi* signal along with the register's "address" in the *tms* signal).

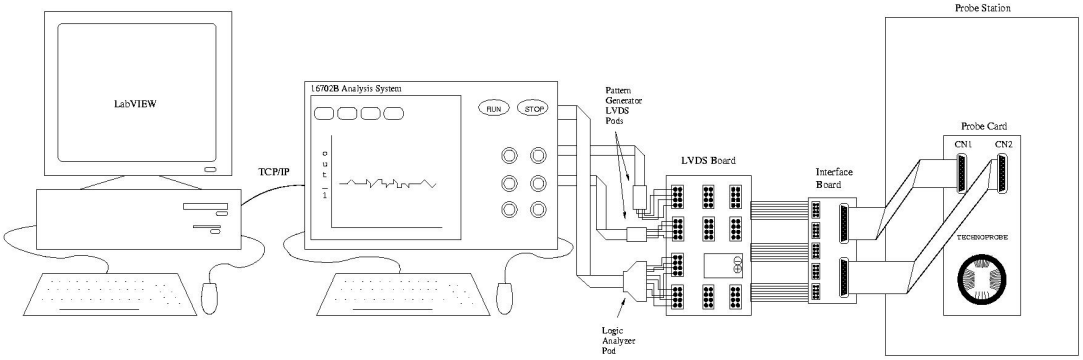

Figure 1: Hardware schematic.

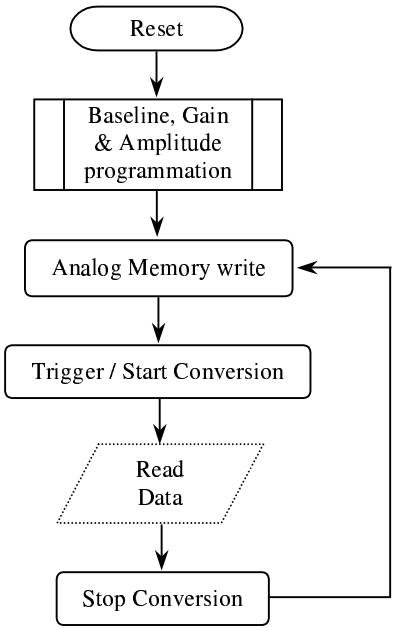

Figure 2: System operation overview.

The typical test cycle starts with the JTAG configuration and with the measurement, trough the digital power supply system of the static and dynamic power consumption. Then, a linearity plot and a baseline scan are performed for all the channels in two different working conditions, i.e. with the ADC working at full and half frequency. The overall time required to make the tests depends, of course, on the granularity required to the measurements and may range from a few minutes to several hours.

It must be pointed out here that extremely detailed tests are necessary only in the first part of the characterization procedure, when the architecture has to be validated and possible design bugs have to be found. At a later stage, the aim of the tests is instead to distinguish between good and bad dies. It is important, in this case, to identify a subset of measurements that give the best compromise between test speed and fault coverage. With our system we were able to reliably screen the chips in an average time of ten minutes.

III. System Performance

We show in this section some representative examples of the performance of our system. We describe in the following the results of some screening tests as well as of some detailed measurements. In particular, we present here firstly basic integral tests i.e. baseline, noise and linearity plots. Then we discuss specific tests which have been used in the study of the ADC control logic and in optimisation of the read amplifier of the analog memory.

The graph in figure 3 shows the noise level for all channels. The average value is 1.7 ADC counts, which gives an ENC of approximately 265 electrons in agreement with the target noise of 250 electrons.

Figure 4 is an example of a linear fit to data generated using the internal pulse generator. The only action the user needs to take is entering the input signal amplitudes and then the interface sets the calibration register values, averages the output amplitude and does the linear fit automatically. The standard deviation of the data points from the fit is, in average, 7 mV; which represent a 4.5% deviation for the smallest input amplitude.

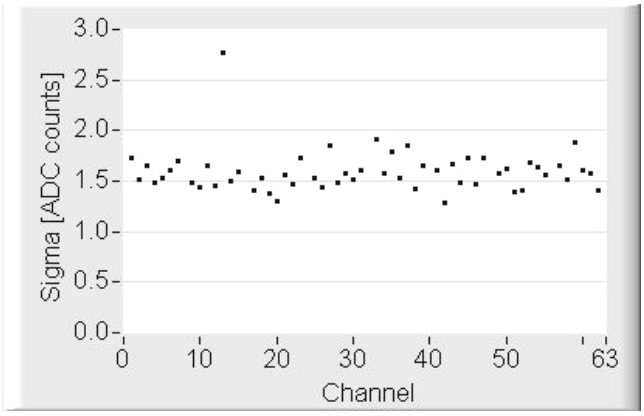

Figure 3: Example of noise measurement.

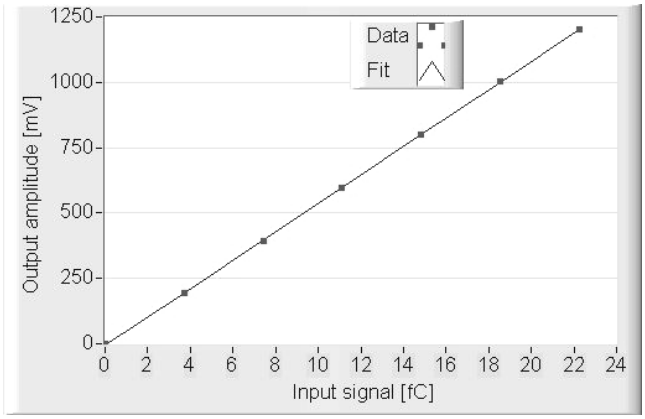

Figure 4: Linear fit for a typical channel.

The gain obtained with the linear fit is showed in figure 5 for the odd channels.

We observe a very good uniformity; quantitatively, the standard deviation is 0.3 counts/fC or less than 1%. The average gain is 41.42 mV/fC that is a 3.5% deviation from the expected value of 40 mV/fC.

Performing fine control of the baseline we were able to find a control fault of the ADC. Being a successive approximation ADC, this circuit determines one bit at every clock cycle starting with the MSB.

However, the conversion is erroneously performed in twelve clock cycles instead of ten so *only* the two MSB's are decided a second time. Consequently, if a sample whose voltage level is very close to the middle of the dynamic range of the ADC —where the MSB changes— is to be converted, it is possible that the second time the ADC determines the MSB it "changes its mind" and puts it to high when it had previously decided it low, or vice versa. In such a case, the LSB's would (almost) all be 1's and changing (rising) just the MSB would produce a wrong output code with (almost) all ten bits high. We see an example of this problem in the graph of figure 6, where we

set the baseline to obtain output codes very close to 512 ADC counts.

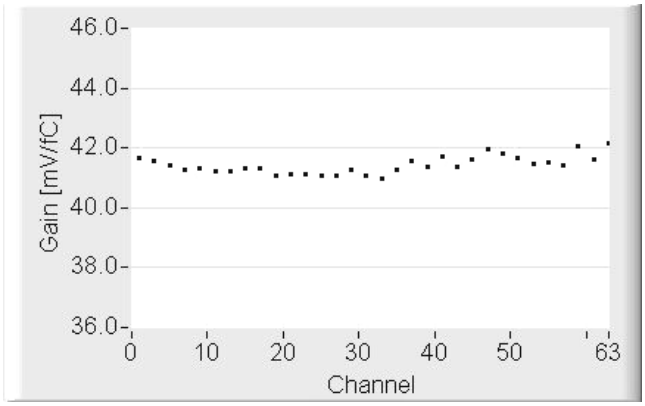

Figure 5: Gain uniformity.

Finally we also evaluated the performance of the read amplifier of the analog memory by observing the signal degradation as a function of two parameters. We measured the signal amplitude as we shortened the reading time of the analog memory and repeated this for different power conditions of the read amplifier.

Figure 7 shows the amplitude of a 4-fC signal for several lengths of the EoR (End Of Read) delay, which is the time allocated for the amplifier to load a single analog memory cell value into the ADC before conversion. The continuous curve of figure 8 corresponds to the nominal power consumption of the amplifier and the other two to less power consuming cases. This test allows us to determine an optimal compromise between reducing the total dead time for the conversion and reducing the total power consumption of the chip.

We see that even for the lowest-power mode of the amplifier we can reduce the EoR delay by 300 ns, from the nominal 500 ns, without appreciable degradation of the signal amplitude. This would allow reducing the dead time of PASCAL by almost 154 µs.

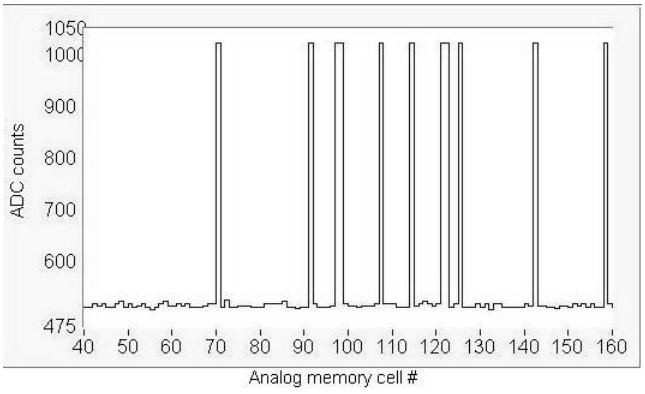

Figure 6: ADC conversion error.

IV. Conclusions

We have built and proved the reliability of the test system of the front-end chip for the SDD. We observed a good performance of both the last prototype and the system itself. Even though we oriented the implementation of the latter for better flexibility and detailed testing rather than for speed and comprehensive automation, we still obtained acceptable performance for faulty-piece selection.

Nevertheless we have also identified some aspects which have to be either improved or added to our system, like data acquisition rate, JTAG programming time, acquisition of all the analog parameters (reference voltages, etc.) and the development of an interface with a data base for mass data storage. Yet the present system is adequate as the core of the final test set-up.

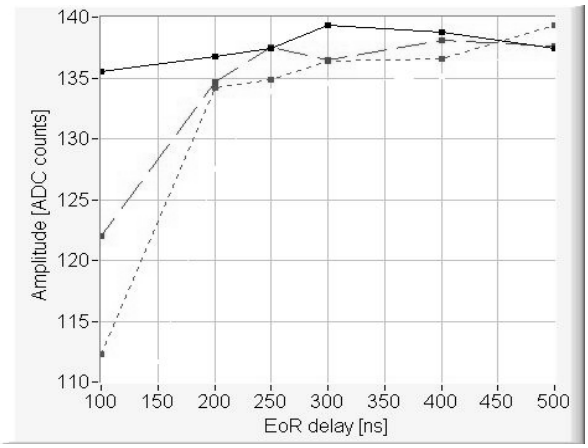

Figure 7: Analog memory read amplifier performance. The dotted curve represents the lowest-power mode of the amplifier.

V. Acknowledgements

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VI. References

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