Industrial Production of Front-End Hybrids for the CMS Silicon Tracker

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Abstract

The design of the Front-End Hybrid for the readout electronics of the CMS silicon tracker has been completed and a fully industrial production of ca. 15 000 modules needed for the CMS tracker has started. We describe the final design of the multi-layer board and its implementation in a full flex polyimide technology with a ceramic carrier substrate. In the second part of the paper we report on our experience with the start-up of the production in industry.

I. THE CMS FE-HYBRID

The CMS tracker consists of about 15000 silicon detector modules arranged in 10 cylindrical layers and 18 disk-like structures around the LHC interaction point in the central/barrel and end-cap region, respectively. Each detector is read out by four or six analogue integrated circuits, the APV25[1] chip. As described in ref. [2], the FE-hybrids have been designed and developed by a team of two laboratories in Strasbourg[1,2] and supported since the end of 2002 by the CERN[3] group for the mechanical integration of the ceramic substrate. An automatic test station for the industrial production has been built by a collaboration of two university laboratories in Louvain-la-Neuve[4] and Aachen[5].

A. *The Design of the Front-End Hybrid*

The FE-hybrid carries the APV read-out chips and three control ASICs: the PLL chip for decoding the level_1 trigger from the 40 MHz clock signals and the synchronisation of phases, the MUX circuit to multiplex a pair of two APV analogue outputs onto a single differential line and the DCU (Detector Control Unit), a chip with six input lines multiplexed on a 12-bit ADC used to measure temperature and to monitor power supply voltages and the leakage return current of the silicon detector. No HV is present on the hybrid.

The locations of the different ASICs are clearly visible in Fig. 1 showing the upper metal layer of two different types of FE-hybrids. Only the APV-readout chips are mounted as naked die, the other ASICs are as packaged components, LPCC. A polyimide cable has been integrated into the layout of the hybrid; the length of this cable is 5 mm longer for the otherwise identical TEC hybrids, not shown in the figure. For further details see ref [2].

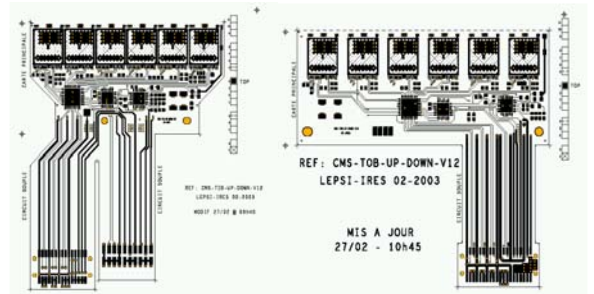

Figure 1: TIB and TOB layout on the left and right hand side, respectively. Clearly one can distinguish the positions of up to 6 APV read-out chips and of the three auxiliary ASICs mounted as LPCC together with the SMD components.

Table 1: Different types of FE-Hybrid required for the CMS tracker

Hybrid type	Required number of hybrids for the tracker
TOB	
4_ r down	540
4_ r up	1908
6_r up	1680
4_ stereo up	540
4_stereo down	540
TIB	
4_r down	1428
6_r down	768
6_stereo down	288
6_stereo up	1056
TEC	
4 up	4112
6 up	1152
6 down	1200
Total	**15212**

B. *Modularity*

Two basic geometries of the electrical circuit had to be developed: the very high-density layout for the very inner part of the CMS tracker (TIB and TID) and a slightly larger circuit for the outer barrel (TOB) and the end-cap (TEC) regions. There are hybrids with four and with six APV25.

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4 Institut de Physique Nucléaire, UCL, Louvain-la-Neuve, L.Bonnet, V.Lemaître and X.Rouby,
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For stereo modules identical hybrids are used, but the connectors are mounted on the back side of the cable. In addition, stereo and r-φ modules use different ceramic substrate. In total, 12 different types of hybrids have to be produced in parallel. However, for most types of hybrid at least 500 objects will be produced. The precise numbers of each type are listed in table 1. Examples of the outlines of the ceramic substrates are shown in Fig. 2, 3 and 4 for the TIB, the TOB and the TEC, respectively. In total 15212 hybrids plus at least 6% spares will have to be produced over the period of one year.

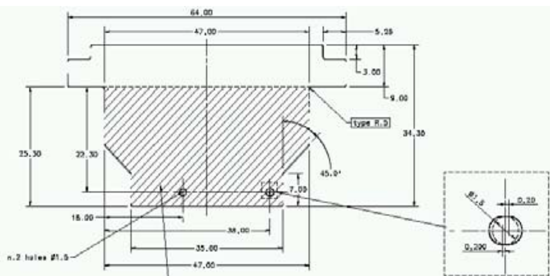

Figure 2: The ceramic substrate for the r-φ TIB hybrids.

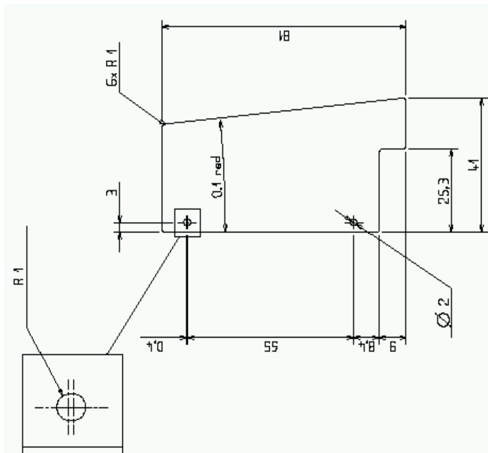

Figure 3: Ceramic substrate for the stereo TOB hybrids.

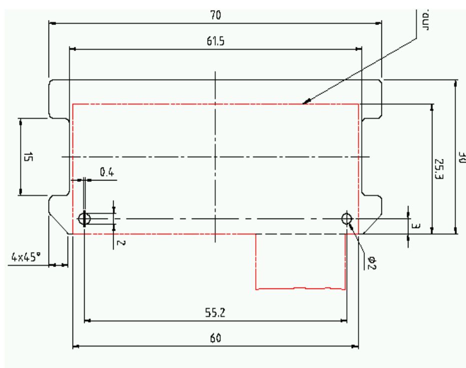

Figure 4: The same substrate is used for the r-φ and stereo TEC hybrids.

II. TECHNOLOGY CHOICE

Reference [2] presented the first proto-types realised in a thick-film technology on a ceramic substrate. The Al_2O_3 substrate is well adapted to evacuate the heat. We also reported on other prototypes in various technologies using Cu-metallized polyimide layers to fabricate the circuit in combination with FR4 and Carbon fibre rigidifiers to obtain sufficient mechanical stability and flatness.

The structure of these multi-layer board consisted of different materials of un-matched CTE-coefficients. This and possibly also inappropriate handling lead to hybrids of moderate flatness, which are considered impractical for the automatic assembly procedure of FE-hybrids and pitch-adapters. Much effort has been invested to obtain flatter and more rigid hybrids.

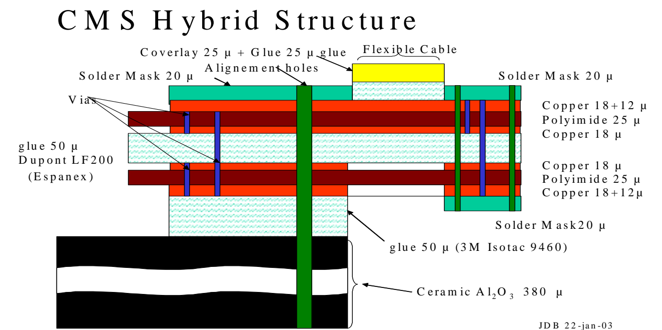

Figure 5: Vertical layer composition of a hybrid (final version).

Fig. 5 shows the finally chosen vertical layer-composition of the FE-hybrids. The hybrids are fabricated by two polyimide circuits of 25 μm thickness, with 18 μm thick Cu layers laminated to it, yielding a structure of four metal layers. Two of the Cu layers increase their thickness by 12 μm during the metallization of their via. The two Polyimide sheets are laminated together with Dupont LF200 (Espanex) to form the 4-layer printed circuit.

The minimal feature sizes of this circuit are 100/300 μm ∅ via, line width of 120 μm and distances of 180 and 90 μm for line-to-line and via-to-line separations, respectively. Large metallized through holes are implemented under the ASICs to transfer the heat to the underlying ceramic substrate from where the heat is evacuated to the frame of the detector module.

A crucial and sensitive step is the lamination process to the ceramic carrier substrate developed by the CERN group in collaboration with the circuit manufacturer: A double sided radiation-hard acrylic adhesive (type 3M 9460PC, ISOTAC) is used to glue the polyimide circuit to the ceramic at moderate temperature (40°C) and pressure (5 Kg/cm²). The alignment for the polyimide circuit relative to the ceramic has to be better than 100μm.

The radiation hardness of the hybrid was verified by irradiating its SMD components with neutrons at UCL Louvain, and exposing a complete hybrid to a 24 MeV proton beam at the compact cyclotron in Karlsruhe with a flux of $2.4 \ 10^{14}$ 1 MeV neutrons equivalent and a dose of 340 kGy. The hybrid was powered, clocked and triggered and did not stop functioning or lose performance.

III. TECHNICAL SPECIFICATIONS

The detailed technical specifications are available in ref [3]. They contain the electrical schemes, the layout of the circuits, the specifications of the multilayer circuits, the lamination procedures, precise prescriptions for the mounting of SMD components and ASICs, in particular for the APVs and their bonding diagrams and a description of the required test procedures.

The specifications refer in general to established industrial standards for the production and assembly of multilayer circuits and multi-chip modules, ASIC mounting and bonding. They are IPC-A-600-F, IPC-A-610C, IPC-SM-782A and IPC-SM-784.

Further than these standards we give very precise instructions for all mechanical parameters like dimensions, relative and absolute alignment, placement of components, in particular of the ASICs and we provide detailed bonding diagrams which have to be followed meticulously.

IV. INDUSTRIAL PRODUCTION

From the beginning it was the strategy for the supply of the required over 15 000 FE-hybrids to rely fully on industrial capacities and standards for all steps of the production:

- Electrical circuit,
- Lamination on ceramic substrate
- Loading with SMD components and connectors
- Precision mounting of ASICs and bonding
- Temperature cycle and
- Final functionality test before delivery

In the following paragraphs we will present some results from the industrial pre-production runs from spring to summer 2003: first, some verifications of the electrical performance and secondly the results of our visual inspections concerning the mechanical properties and the quality of soldering, ASIC positioning and bonding.

A. Front-End Hybrid Industrial Tester (FHIT)

To test the functionality of each hybrid by the manufacturer before delivery, an industrial portable test station was developed by UCL-Louvain and RWTH-Aachen described already in reference [2] and [6, 7], the so called Front-end Hybrid Industrial Tester (FHIT). A bar-code scanner is used to register the individual hybrid and to recognise the type of hybrid. The test station performs a simple electrical and continuity test and then a full functionality test including read-out. Also a calibration of the DCU ADCs is performed. A protocol of the entire test is written to a log-file, which is transferred to the CMS database. The full test of a hybrid takes about one minute.

Complex mechanical adapters have been designed by UCL to accommodate the 12 different hybrid geometries as seen in Fig. 6. The mechanics serves in particular to test the detector bias return line on the hybrid with needle probe placed carefully on a test pad.

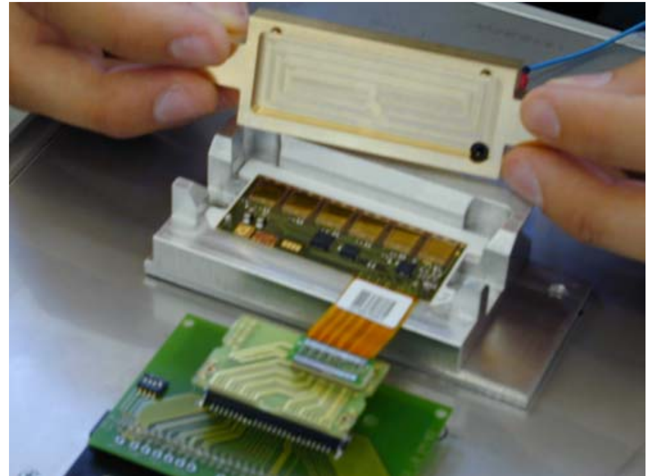

Figure 6: Mechanics to adapt the hybrid geometry to the FHIT.

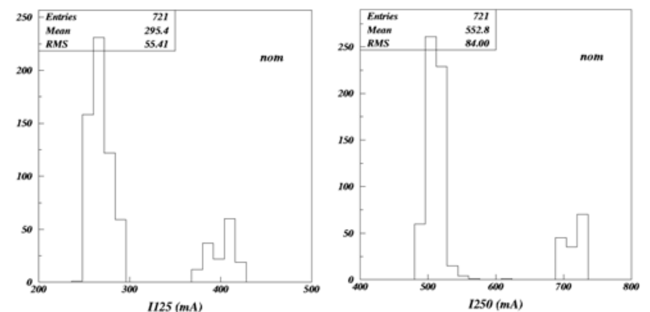

Figure 7: The power distributions of over 700 hybrids as measured with the FHIT. The two peaks are related to hybrids with 4 and 6 APVs.

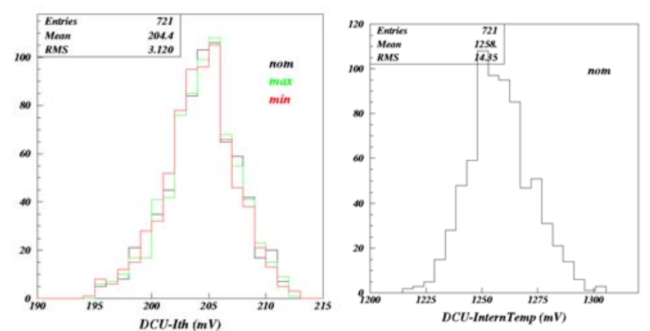

Figure 8: Two different measurements on over 700 hybrids with the FHIT. The left distribution refers to a measurement of the reference current used to feed two external thermistors mounted on the detector module. The histogram on the right is a reading from a temperature sensitive element in the DCU chip. The RMS values of these distributions correspond to 1-2 %.

B. Results from the Electrical Measurements

The FHIT served to detect defaults in the production like missing connections or shorts, wrongly mounted components and destroyed or missing non-redundant

bonds. In addition many important data are collected during the test to characterize the hybrids and in particular the DCU control chip. As an example we show in Fig. 7 and 8 the distribution of the over 700 hybrids on the power consumption and two different temperature measurements, respectively. The narrowness of these distributions indicates good control over variations of components and the environment of the tests.

C. Results of the Visual Inspection

The most difficult part in starting up the production was related to the tight specifications with respect to mechanical properties, wire bonding quality and cleanliness.

Circuit lamination on the ceramic substrate: This procedure could be stabilized within 3-4 runs. Critical issues were the alignment of the circuit relative to the ceramic within 100 µm and to guarantee the integrity of the adhesive used.

SMD loading, soldering and cleaning: Although we considered this to be a standard industrial process several difficulties were encountered. The required cleanliness to ensure the long term functioning of the hybrids, namely the absence of loose solder balls and of solder flux reminisces on the circuit, was only achieved after a larger series of hybrids.

ASIC mounting and bonding: The APV chips are loaded directly from the wafer using the map from the wafer tests indicating good dies. A record is kept by the loading machine so individual chips on each hybrid can be traced to their wafer of origin later on.

The precision mounting of the APV ASICs and bonding was one of the most difficult tasks to achieve in an industrial process. The difficulty of this task is illustrated in Fig 9. The design of the APV chip included a very special feature w.r.t. the pad layout for the power bonds being interleaved with the pads of the analogue inputs. This requires a very high precision of the order of 30 µm with which the APVs have to be mounted, in order to insure that the bonding to the pads of the pitch adapter can be performed for all input pads. The required mounting precision is in fact at the limit of industrial feasibility. Also to follow the exact geometry for the bonding of the power pads of the hybrid, crucial for the subsequent bonding of the input pads, required some learning process by the manufacturer.

In order to increase the reliability of the bonds related to controlling and reading out the chip, it was decided to use both bonding pads available on the chip to increase the redundancy of the bonding. Although both pads are very close to each other it was possible to have both bonds within the specifications, as shown in Fig. 10.

Polyimide cables: Very recently a problem was identified only after first detector modules had been assembled in September 2003: The cable shows a weakness close to the connectors, leading to damage of the conductive lines whenever the cable is manipulated.

The reason is the brittleness of the Au-Ni metallization of the copper lines chosen to facilitate bonding and soldering.

By now a possible solution has been found, namely to reintroduce a stiffener behind the connector in order to reinforce the cable. This stiffener had originally been foreseen and then been suppressed to facilitate the production of the circuit. First tests indicate that the stiffener is compatible with the soldering of the connector.

Further, a small modification of the existing masks for cover layers and the solder mask is in preparation in order to limit the area of Ni metallization for the rest of the production.

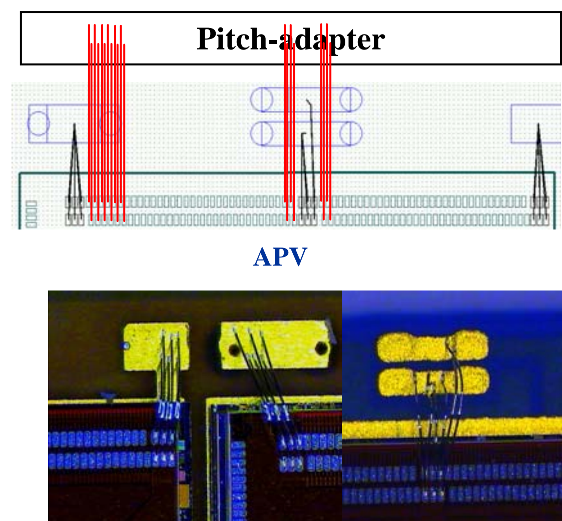

Figure 9: View of the bonding task in the front of the APV chip.

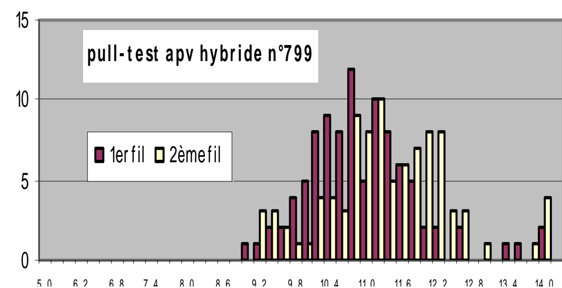

Figure 10: Result of a pull test on a hybrid delivered in September.

D. Production Yield and Quality Assurance

About over 700 hybrids of the “final” version described here have been produced and delivered in 2003 by the hybrid manufacturer [4, 5] before the time of this workshop. These are deliveries of the first large order of nearly 5000 hybrids, which serve to assure the start of the production of silicon detector modules and to qualify all procedures used in the production of the hybrids in an industrial environment.

Yield: Looking at the last three production batches of 541 hybrids, we can derive a tentative figure for the production yield. Depending on the selection criteria, between 41 and 56 hybrids have been classified as bad. A summary is listed in table 2. The difference between these two numbers lies in tight selection cuts on noise and the response to calibration pulses of the APV chips used in these tests. The numbers include all hybrids, those already classified as bad by the manufacturer (on the basis of the FHIT-functionality test) and the hybrids we considered as not being conform to the technical specifications. Presently we find a fraction of about 10% "bad" hybrids, clearly to be improved in the forthcoming runs. Not included in the numbers of failing hybrids are all cases rejected by the manufacturer already before the step of mounting the components. The anticipated goal is to have a yield of over 97%.

Table 2: Reasons and numbers for the rejection of hybrids in three recent production batches

Rejection cause	**in batch**	**all**
APV noise or calibration	8 + 4 + 3	15
Broken ceramic	0 + 5 + 7	12
Damaged Bonds (manipulation)	5 + 2 + 5	12
Bad solder (polluted)	0 + 1 + 3	4
DCU badly positioned	0 + 1 + 0	1
Cuts on bonding pad	0 + 3 + 0	3
Connector suspect	0 + 1 + 0	1
De-lamination	0 + 0 + 1	1
Connectivity	0 + 0 + 1	1
Not fully understood	0 + 4 + 2	6
Total	13+21+22	56

E. Quality Assurance

We expect that the large volume of our production will automatically ensure a high level of uniformity and quality. First experience with (not so large) prototype runs shows however, that a continuous inspection of the hybrids is absolutely necessary at all stages.

The industrial tester FHIT plays a very important role to reject bad hybrids already at the manufacturer. This serves also to indicate possible problems in the production process. All hybrids with ASICs already mounted have to be returned to us in order to guaranty the tracing of all chips in this sensitive technology. We use these hybrids for destructive tests.

Whereas in the beginning we inspected visually all hybrids received in large detail, we reduced this fraction now to a sample of 20% for the runs being received now. Once production is running at full speed we hope to reduce this fraction to about 2% of received good hybrids.

All hybrids are being exposed to 5 over night thermal cycles of low (-30°C, 5×) and high (80°C, 4×) temperature before the acceptance and functionality test at the manufacturer. Further more, a fraction of hybrids have been running for long periods in test set-ups and special installations with temperature cycling. So far we have no indication for aging or dying components or connections. Burn-in stations for larger quantities of hybrids are in preparation.

V. SUMMARY AND CONCLUSIONS

We presented the successful development of the final version of the FE-Hybrids for the CMS tracker and our experiences with the start of the industrial production. We encountered two difficulties to produce the CMS hybrids in an industrial production chain related to two important features imposed on the hybrid design.

First, the layout of the very successful APV readout chip could not be re-optimized for the final design of the hybrid and the automated module assembly procedures. The complicated geometry of the read-out chip entailed many constraints with respect to the required precision in mounting and bonding of the ASICs.

The second element, which constrains the production in industry by tight specifications, was the mechanical interface to the detector module and its assembly leading to a special lamination procedure of the substrates and 12 specific types of hybrids necessary.

Despite these difficulties we succeeded to identify a qualified industrial consortium [4, 5] and to start the mass production of the hybrids.

VI. ACKNOWLEDGMENTS

We would like to thank F. Hartmann, A.Furgeri and Th. Weiler for the irradiation of our hybrids at the Cyclotron in Karlsruhe and E. Forton and G. Gregoire of UCL Louvain for the irradiation of SMD components.

VII. REFERENCES

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