Design, Realization and Test of a DAQ chain for ALICE ITS Experiment

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Abstract

The paper presents a new version of a rad-hard digital chip together with a full data acquisition system for the DAQ chain of the ALICE ITS experiment. The chip has been designed and realized on a rad-hard digital library provided by CERN and, in addition to the previous version of the chip; it includes an on-line bi-dimensional compressor. The chip is part of a full data acquisition chain that has been tested both in Bologna and at CERN. The data collection has been executed throughout an interface card and an optical fiber to a hard disk on a PC.

I. Introduction

The paper explains the design and the realization of a small size digital rad-hard chip submitted at CERN multi-project run Multi-Project-Wafer-9 in December 2002 and tested successfully in March-April 2003. The design is a part of the ALICE ITS [1], [2] experiment, at CERN. Nevertheless, within the ALICE ITS, that is a portion of the whole ALICE detector, the chip takes the functions of data compressor and packer for a data acquisition chain. Particularly the chip is a device that will take part of an electronic ITS front-end board. The chip, hereafter named CARLOSv3, is third version ([3], [4] for version v2) of a VLSI Application Specific Integrated Circuit (ASIC) device that has been designed and developed, within the ALICE collaboration, both in the Physics Department of Bologna University and at CERN. Indeed, it has been designed mostly by means of the VHDL language and implemented in a 0.25µm CMOS 3-metal rad-hard digital library [5], [6], [7]. Apart from the VHDL the chip implements 4 RAMs cells, also designed to be rad-hard, that have been developed full-custom and treated as black-boxes in the context of the chip. The library itself has been developed at CERN to be applied into LHC electronics even though is basically derived from a standard 0.25µm CMOS commercial technology. CARLOSv3 is composed of nearly 10k gates, 88 user pads out of the 100 total pads, it is clocked at 40 MHz, and the whole die area is 4x4 mm^2. The library and the design techniques guarantee the radiation hardness of the chip under the radiation dose of the experiments that is expected to be some tens of krad. The implementation of the on-line data 2D-compressor has been carried out, apart from digital control logic, by means of previously mentioned full-custom dual-port static RAMs divided into 2 256x9-bit words per data channel. Altogether there are 4 RAM macro cells. Also these macro cells have been implemented by means of the rad-hard library.

Within the whole DAQ chain the chip takes its functions after the data coming from the silicon drift detector have been sampled and digitalized by other dedicated chips. Then, after CARLOSv3 has compressed and packed the data they go to a receiver card named CARLOSv3_rx that acts as a concentrator for several CARLOSv3. All in all the data are serialized into an 800Mb/s optical link and received into a mirror receiver card that de-serialize the stream and re-construct the incoming data. So the paper presents both the chip design and tests and the tests of the full DAQ chain that have been executed in Bologna and at CERN.

As far as the chip technical features, CARLOSv3 is composed of nearly 10k gates, 88 user pads out of the 100 total pads, it is clocked at 40 MHz, and the whole die area is 4x4 mm^2. The enclosed gate transistor technique guarantees the radiation hardness of the circuits under a given radiation dose. In ALICE SDD experiment it is expected that radiation dose will be some tens of krad. As far as the chip functions, the implementation of the on-line data 2D-compressor [8] has been carried out, apart from digital control logic, by means of the previously mentioned RAM memories. These are full custom designed, dual-port static RAMs [9] composed of 256x9-bit words each. Altogether there are 4 RAM macro cells. Also these macro cells have been implemented by means of the rad-hard library. The chip, besides the mentioned enclosed gate transistor technique, has been provided with internal self-checks such as parity error controls on configuration registers and on RAM data. This is in order to have the full chain even more robust and to be able to recognize any failure flag to let, for example, the acquisition restart. It should be noted that all the expected radiation doses and all the foreseen data distributions are just extrapolated from other experiments and adapted to ALICE SDD features. Only when the entire machine at CERN will run in some years it will be known how the predictions fulfill the experiment. On the other hand we feel confident on the calculations since margins have been left during the machine design. The chip was submitted at CERN multi-project run Multi-Project-Wafer-9 in December 2002 and tested successfully in the early 2003. The design is a part of an ALICE SDD DAQ chain [10] that is going to be developed both in Bologna University and at CERN.

II. CARLOSv3 Prototype

CARLOSv3 can work in two different main modes: RUN mode and JTAG mode. Run mode is the normal working one that allows the chip to take its functions and to transfer the compressed and packed data to other cards in the DAQ chain. Conversely, the JTAG mode allows the chip to set-up its internal registers or simply to modify their values. The two modes can only work one at a time.

As far as the chip interfaces it directly connect 3 main kinds of devices:

1. two hybrids where a hybrid is a board containing the front-end electronics acquiring data from a SDD. Each hybrid sends an 8-bit data stream that corresponds to an input channel for CARLOSv3;
2. a rad-hard serializer chip that sends data to a receiver card named CARLOSv3_rx. This is done by means of an 800 Mbit/s optical link. The serializer directly receives the 16-bit output channel of CARLOSv3. Particularly the 16-bit word is composed of a 15-data word plus 1 enable bit;
3. CARLOS_rx that, as previously mentioned, is a receiver card. Moreover it is an FPGA-based device that takes place in a counting room with the purpose of collecting the incoming from different SDD chains. Then CARLOSv3_rx sends data towards the DDL system. In addition it remotely controls CARLOSv3 using a 40 MHz serial back-link and a JTAG port for what concerns CARLOSv3 RUN mode and JTAG mode.

transmitters for fiber channels. All the boards are inserted in a radiation environment. The whole acquisition system electronics performs analog data acquisition, A/D conversion, buffering, data compression and interfacing to the ALICE data acquisition system. Particularly the data compression and interfacing task is carried out by CARLOSv3 chip. Each chip reads two 8-bit input data, is synchronized with an external trigger device and writes a 16-bit output word at 40MHz. Then the data are serialized and transmitted by means of an optical link at 800Mbit/s [11].

CARLOSv3 itself contains a JTAG unit: this is a block driven via a JTAG port, which allows CALOSv3 chip to run in two different ways: RUN mode or JATG mode. The mode selection and some dedicated commands such as reset are read by means of a *serial back-link* channel shown in figure 1. For example once in JTAG mode the JTAG Unit allows all internal registers to be initialized, read, written and so on. For what concerns JTAG, CARLOSv3 also acts as a JTAG switch

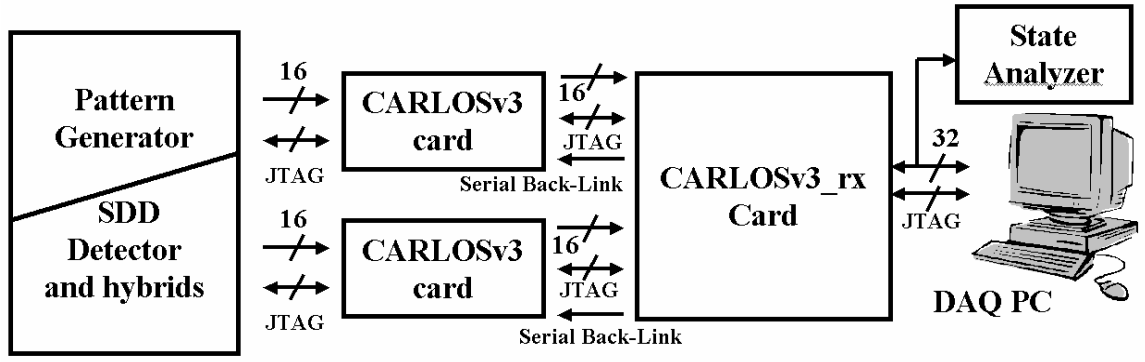

Figure 1: Readout architecture sketch for ALICE SDD experiment

III. Readout Architecture

The requirements for the SDD readout system derive from both the features of the detector and the ALICE experiment in general. A sketch of the SDD DAQ chain is shown in figure 1 where both cards for CARLOSv3 and CARLOSv3_rx are present. On the left side of the figure the *SDD Detector* and the *Pattern Generator* are mutually exclusive so that just one at a time can provide the input data vectors. This way the designed chain has been used firstly for test purposes with the *Pattern Generator*, and then it will be replaced in the experiment by the real *SDD detector*. The amount of data generated by the SDD is due to 2 half detectors for each CARLOSv3 chip. This is why in the figure are shown two CARLOSv3 cards and one CARLOSv3_rx card. Nevertheless the system can work also with one CARLOSv3 board only. Each half detector is composed of 256 anodes and, for each anode, 256 time samples have to be taken in order to cover the full drift (time) length. Altogether each detector is able to generate an event made of up to 256x256 data words. The data outgoing from two half detectors are read by one of the two channels of CARLOSv3 chip. The readout electronics is composed of front-end boards (i.e. hybrids in figure 1) that collect data directly from the silicon detectors and end-ladder boards that contain CARLOSv3 chips, serializers and optical

providing three JTAG ports in output: one for the left hybrid, one for the right hybrid and one for the serializer chip. In other words CARLOSv3 receives one input JTAG port and provides in output 3 JTAG ports, thus allowing opening JTAG connection towards different devices.

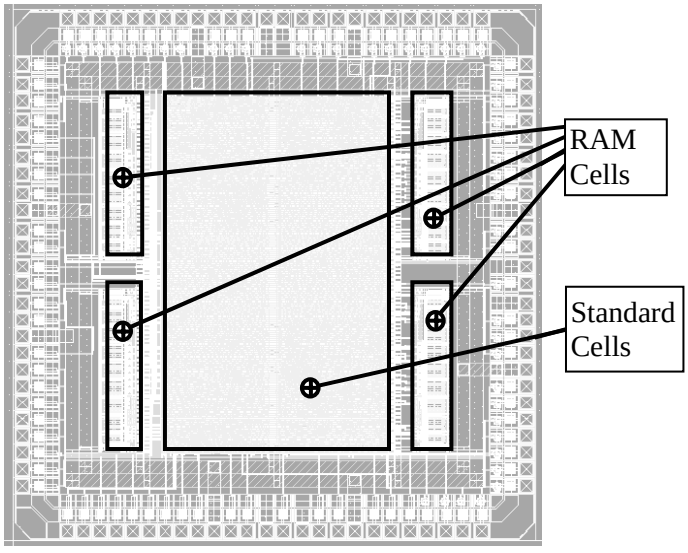

Figure 2: CARLOSv3 layout

Figure 2 shows a picture of the final layout of CARLOSv3. It is a 16 mm^2 squared chip, RAMs included, with 100 pads; it contains 10k gates and is packaged on a CQFP100 ceramic package.

IV. Controlling CARLOSv3 via Serial Back-Link

As previously mentioned CARLOSv3 is remotely controlled using a *serial back-link* coming from the CARLOSv3_rx device. Data transferred on the serial link are synchronous to the incoming master clock. CARLOSv3 has a synchronization state machine that is responsible for handling link initialization and synchronization as shown in figure 3. Upon power up or external reset via the *serial back-link*, the state machine enters the acquisition state ACQ and searches for the IDLE pattern. Upon receiving three consecutive IDLE patterns after the first one, the state machine enters the synchronization state SYNC. Whenever a valid code is detected in SYNC state the machine remains in the state. Conversely, if an invalid code is received, the state machine transitions to the CHECK state. If, in the CHECK state, CARLOSv3 receives 4 consecutive valid codes, the state machine determines that the link is good and transitions back to the SYNC state for normal operation. If, in the CHECK state, CARLOSv3 recognizes 3 invalid codes (not required to be consecutive), the state machine determines that a loss of the link has occurred and transitions back to the ACQ mode.

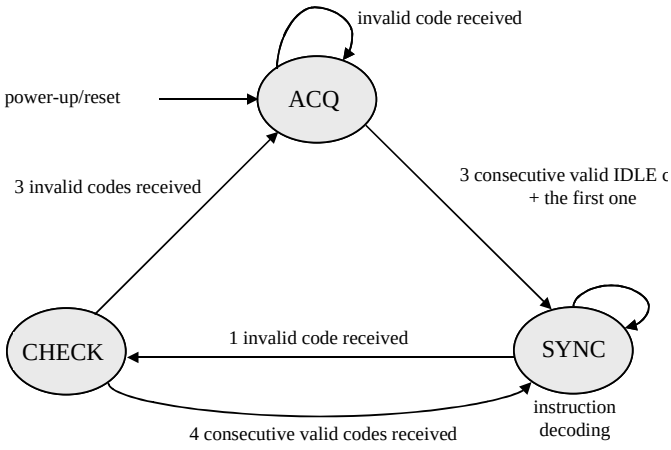

Figure 3: Synchronous serial back-link state machine decoding

V. CARLOSv3 and DAQ Tests

A PCB dedicated to test purposes only has been designed for CARLOSv3 tests. This is a four-layers PCB that provides I/O signals by means of strip-line connectors and by inserting the CQFP100 packaged chips on dedicated ZIF sockets. These chips derive from one silicon wafer out of the two used for the multi-project-wafer run at CERN; in addition they have been randomly selected from the central lines of the wafer. The chips have been stressed up to 60 MHz while for higher clock frequencies they begin to fail. In addition, even though the CARLOSv3 layout has been done with separated core and periphery power supply pads, the tests have been executed with 2.5V for both powers. Moreover, at required 40MHz clock frequency the chips work with an average power consumption of 200mW.

The very first test performed on CARLOSv3 was to stimulate it with the same test vectors used for the post-layout simulation during the chip design. The pattern generator provided a 100 k-word test bench containing the JTAG configuration and two 50-kword events. Then data obtained using the logic analyzer have been processed using a dedicated SW tool written with the purpose to reconstruct the inputs values starting from actual CARLOSv3 outputs: in other words the tool performs the reverse function that was carried out by the chip. As a second step the tool compares actual input values to reconstructed inputs and draws a list of errors in case of mismatch. This software tool has automated the CARLOSv3 tests and made us able to take conclusions upon the results.

Running the test bench on the 35 packaged chips the following results have been obtained:

1. 32 chips are working as expected;
2. 2 chips do not work at all since the output data are completely wrong and away from the expected ones;
3. 1 chip contain only one of the two processing channels perfectly working, while the other gives bad results.

The second test on the 35 chips concerned the *BIST* that is activated and controlled using the JTAG port. The *BIST* on CARLOSv3 has been designed to show the result of the test on the output JTAG output pin with a given code if successful. 32 chips out of 35 passed the BIST, while 3 exited with a failure code. This test proves that the BIST gives the same results as the more complete test did before. Even if 35 chips do not allow getting statistical results, the BIST might be chosen as a very simple and reliable test in order to select working from failing chips, before any other test. Other test benches have been used to stimulate CARLOSv3 are 50k-word events with random generated values, with gaussian generated values and with data coming from previous test beams. Repetitive tests have also been run on the 32 selected chips with good results.

Figure 4 shows the DDL card, the CARLOSv3_rx card and CARLOSv3 card connected altogether into a main box. On the left hand side an optical link send the data to a local data

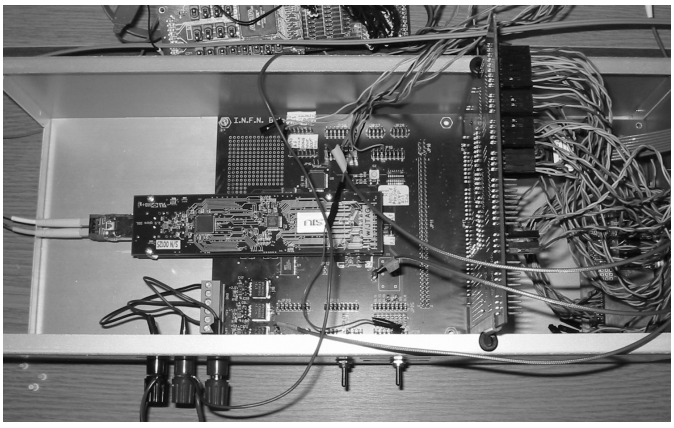

Figure 4: The DAQ chain tested at CERN and used in Test Beam

concentrator in counting room while on the right end side of the picture the wires mean that input data derive from a pattern generator. This configuration allowed acquiring several million events. Nevertheless, as previously mentioned, the real detector has replaced the pattern generator during test beam acquisitions on August 2003 at CERN. Particularly it was an ALICE ITS SDD beam test.

VI. Test Vectors

The chip has been tested as described above and, particularly, it has been tested the internal 2D-compressor. Particularly the compressor has been provided with an off-line *2D-compressor Simulator* and an output-to-input back data generator. In figure 5 this latter block is named *Event Reconstructor*. This way once an input event has been processed by the CARLOSv3 chip the output data set can be both checked by means of the *2D-compressor Simulator* and back-annotated to recreate a new input data set. Thus, it is possible to compare bit-to-bit the first actual input data set with the corresponding recreated one. Obviously these two data sets somehow differ each other since the compressor cuts under-thresholds data. Nevertheless, if the thresholds are properly set to not waste significant data, the 2D-compressor can be tuned for just rejecting the noise. In case of doubt the

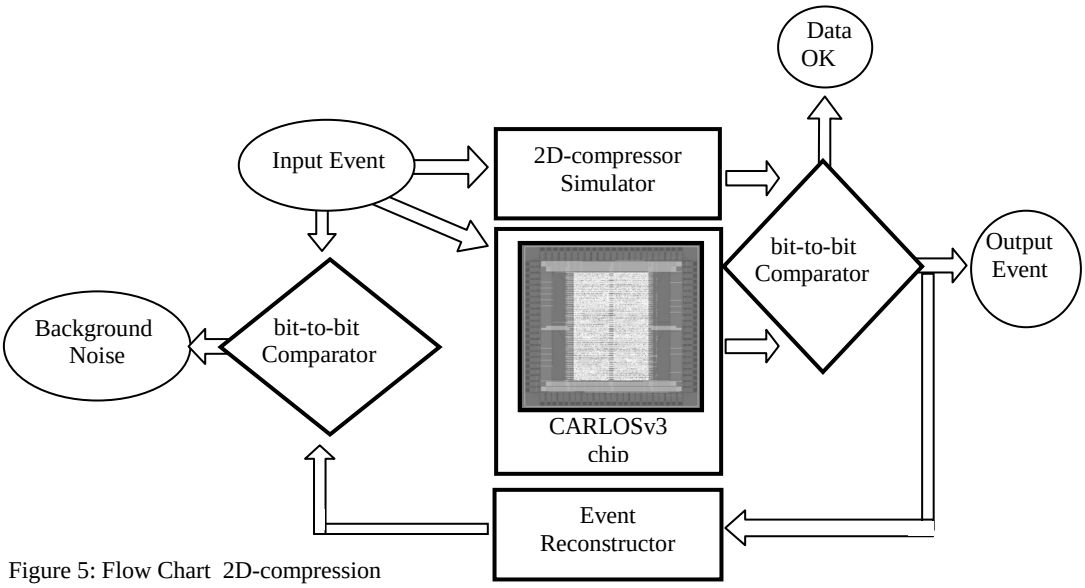

Figure 5: Flow Chart 2D-compression

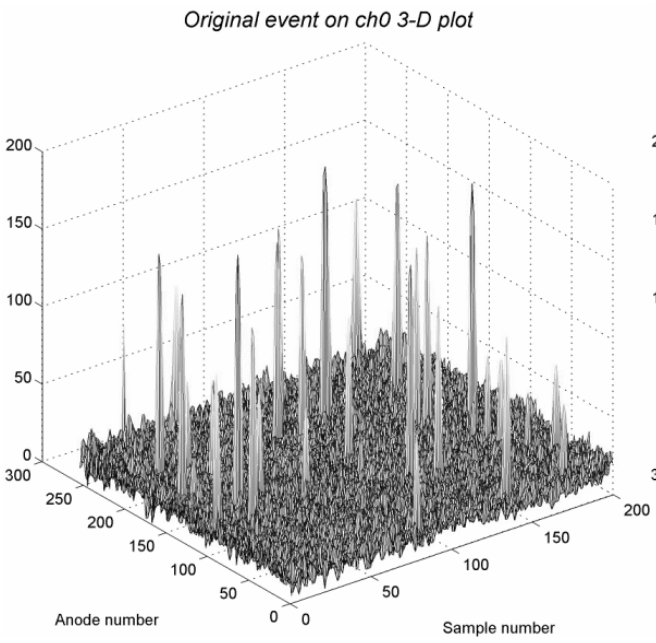

Figure 6a: Original 256 x 200 x 8-bit event before 2D compression

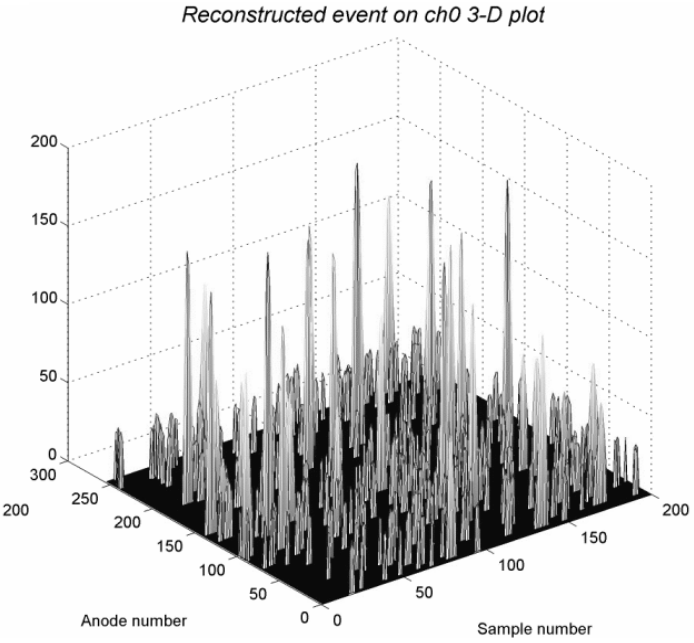

Figure 6b: Reconstructed 256 x 200 x 8-bit event after 2D compression

data must be saved so the thresholds have to be tuned in the lower range. Figure 6a and 6b show two pictures that represent an incoming data set (event) and the reconstructed one. It is clear that all the clusters are properly reconstructed both in position and in height while the background noise is present in the original event but is cut in the reconstructed one. This test has been performed of course on several sets of data to be confident the 2D-compressor does not reject any cluster. On the other hand the *2D-compressor Simulator* is able to extract the compression factor after any event elaboration. This factor is an index of how much the algorithm shrinks the incoming data. The figure shows data that have been extracted by a physics experiment; it has been used a 256 x 200 x 8-bit event that corresponds to a SDD made of 256 anodes each of which is time-scanned for 200 timing slots. The analysis performed shows that the compression factor is nearly 26. In this case the lower and higher thresholds of the compressor were set to 21 and 26 respectively. If they were set to higher levels the figure 6b would show less clusters since the higher are the thresholds (even just the higher one), the smaller is the number of detected clusters. The test vectors have been used both for testing CARLOSv3 alone and for the DAQ chain shown in figure 4.

VII. Conclusion

The chip CARLOSv3 has been implemented using CERN library 0.25µm CMOS technology that employs radiation tolerant layout design. CARLOSv3 is a prototype tailored to fit in the ALICE SDD readout architecture. Taking into account that the CERN 0.25µm library contains a small number of standard cells and they are not so well characterized as commercial ones, it has been decided to try and test first the design flow. Thus the chip has been sent to the foundry in November 2002 and have been tested starting from February 2003. Then the described chain has been used for the ALICE ITS SDD beam test on August 2003 at CERN.
A specific PCB has been designed for the test task; it contains the connectors for probing the ASIC with a pattern generator and a logic state analyzer. The chip is inserted on the PCB using a ZIF socket. This allowed testing the 35 packaged samples out of the total amount of bare chips we have from the foundry. The test phase has shown that 32 out of 35 chips work well. Nevertheless it is planned to redesign a new version of the chip by adding extra features. This will not substantially increase the chip area of 4 mm^2 since this is mainly determined by the memories and by the FIFOs and should be close to the final version of the chip for the ALICE SDD experiment. It is planned to submit the final version of CARLOSv3 upon the final DAQ chain will be totally tested both in Bologna and at CERN.

VIII. References

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