Circuit design with a commercial 0.13 µm CMOS technology for high energy physics applications

K. Hänsler[1], S. Bonacini[2], and P. Moreira[3]

CERN, 1211 Geneva 23, Switzerland

[1] Email: Kurt.Hansler@cern.ch
[2] Email: Sandro.Bonacini@cern.ch
[3] Email: Paulo.Moreira@cern.ch

Abstract

Circuits designed in a commercial 0.13 µm CMOS technology were evaluated in view of the potential use of this technology for high energy physics applications. Prototypes of a bandgap voltage reference, a static random access memory, and a time to digital converter are presented and the consequences of total dose irradiation and single event upsets are evaluated.

I. Introduction

The European Organization for Nuclear Research (CERN) currently uses a commercial 0.25 µm CMOS technology with special layout techniques (enclosed transistors and guardrings) [1] to develop most of the integrated circuits for the Large Hadron Collider (LHC). To explore the possible benefits of more advanced technologies, CERN's EP/MIC group is currently looking at a 0.13 µm CMOS technology, which entered production in 2002 [2].

This 0.13 µm generation application-specific integrated circuit (ASIC) and foundry technology was developed for static random access memories (SRAM), logic, mixed-signal circuits, and mixed-voltage I/O. It is also a platform technology for embedded dynamic random access memory (DRAM). Its main features include supply voltage of 1.2 V or 1.5 V, twin well CMOS technology on nonepitaxial p-substrate, shallow trench isolation (STI), three gate oxide options (1.7 nm, 2.2 nm, and 5.2 nm), and low-resistance cobalt-salicided n+ and p+ doped polysilicon and diffusion areas. Its minimum lithographic image is 0.11 µm. It offers four to eight metal levels, either all copper or copper and aluminium (last level only) with up to three thick metal levels. Its device options contain NMOS and PMOS with several different threshold values, devices for native 2.5 V and non-native 3.3 V operation, n+ diffusion and p+ polysilicon resistors, as well as metal-insulator-metal (MIM) precision capacitors.

Our objective was to examine the possible use of this technology for future high energy physics applications. First irradiation results let us assume that this technology presents a natural radiation hardness [3]. For verification purposes we therefore designed test vehicles and prototype circuits based on both linear transistors and enclosed devices. In this paper we present an insight into three different prototype circuits, namely a bandgap reference, a SRAM and a time to digital converter.

As dies fabricated with different process parameters were available to us, we gained additional information about performance variations circuits might present due to fabrication uncertainties.

In order to examine the device behaviour in the environment of high energy physics experiments, irradiation of some devices was performed using CERN's in-house X-ray generator SEIFERT RP149. The X-rays, peaking at 10 keV, were produced by a W target. The ambient temperature during irradiation was 25 ˚C and different dose rates were applied. The devices were biased and driven with nominal operation conditions during irradiation. Circuit performance was monitored during and after irradiation as well as after annealing periods.

II. Bandgap Reference

A. Circuit Presentation

Several reasons led to the design of a bandgap reference (BGR) for studying the application possibilities of the technology under evaluation. First, BGR are basic cells for analogue designs, ranging from biasing circuits to analogue-to-digital converters; which are fundamental design blocks in silicon detectors and trigger ASICs. Second, BGR can easily reveal the accuracy of models and matching effects of a technology. Third, the existing BGR architectures reveal the difficulties of analogue design with supply voltages below 1.5 V.

In previous technology generations, with supply voltages of 2 V and above, conventional BGR circuits produce output voltages close to 1.25 V which is nearly the same voltage as the bandgap of silicon. They are based on the sum of the built-in voltage on a diode and of a thermal voltage, having negative and positive temperature coefficients [4]. However, this approach prevents low supply voltage operation. We therefore integrated a BGR based on two currents proportional to these two voltages [5]. Figure 1 presents its general architecture.

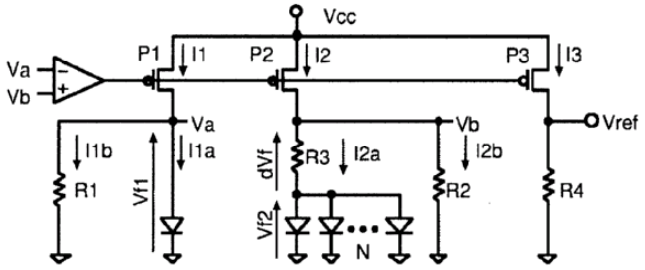

Figure 1: Principle of the integrated bandgap reference circuit [5].

Analyzing this circuit with the assumption that R1=R2 leads to an output voltage of

$$V_{ref} = R4\left(\frac{V_{f1}}{R4} + \frac{dV_f}{R3}\right). \quad (1)$$

If the resistor and diode parameters for this BGR are the same as those for a conventional BGR, its output voltage becomes

$$V_{ref} = V_{BG} \times \frac{R4}{R2} \quad (2)$$

with $V_{BG} \approx 1.25$ V. Thus, reference voltages proportional to the silicon band gap can be obtained at low power supply voltages. Figure 2 presents the layout of the implemented BGR in 0.13 µm CMOS technology measuring 360 µm x 130 µm. The layout does not use dedicated radiation tolerant layout techniques; no enclosed devices or guardrings have been used.

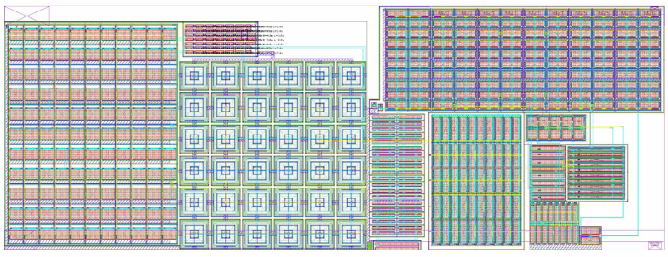
Figure 2: Layout of the implemented bandgap reference circuit.

B. Results

We evaluated several chips and were interested in the output reference voltage of the BGR, its variation with supply voltage and temperature. All tested circuits were fully operational. Table 1 opposes the simulation results and measurements of the important circuit parameters for one random selected device.

Table 1: BGR results summary

	Simulation	Measurement
V_{ref}	0.589 mV	0.587 mV
$\Delta V_{ref}/\Delta V_{supply}$	12 mV/V	14 mV/V
$\Delta V_{ref}/\Delta T$	0.075 mV/K	0.22 mV/K

The measurements show a good agreement with the simulation results. The difference in temperature sensitivity is mainly based on the fact that accurate transistor models for this technology were only available at measurement time but not at design time. This led to a non-optimum internal bias point of the BGR and hence to a higher temperature sensitivity.

The evaluated minimum supply voltage was 1.0 V and the current consumption (for one full BGR cell and one extra test operational amplifier) was evaluated to be 310 µA @ 1.5V.

Therefore, this BGR prototype can already be used as a standard cell for low-precision applications needing a relatively large supply voltage range.

One BGR chip was irradiated with X-rays at a dose rate of 500 rd(SiO_2)/s. Table 2 presents the variation of the band gap reference voltage with dose.

Table 2: BGR variation with dose for a BGR with a pre-irradiation reference voltage of 587 mV

Applied dose [Mrd(SiO_2)]	Variation of V_{ref} [mV]
0.1	0.47
1	0.01
9.1	7.78
18.1	15.17
47.8	26.83
125.2	36.02
24h annealing at 25 ºC	37.42
168h annealing at 100 ºC	18.1

We observed a maximum variation of the reference voltage with radiation of 6 %. This drift is caused by a leakage current in the diode, which is affected by charges trapped in the field oxide above the diode. A slight variation of the operation point of the BGR will strongly reduce this leakage and hence make this BGR radiation hard. However, taking into consideration the applied dose rate, the annealing behavior and in particular the dose rates and levels in front end electronics in the LHC, we conclude that this BGR prototype, designed without enclosed devices, can already be considered radiation tolerant for LHC applications.

C. Comparison to 0.25 µm

The impact of a new technology might be assessed best by comparing its results with a similar application designed in a previous 0.25 µm CMOS technology of the same manufacturer.

Table 3: Comparison of characteristics of BGRs in two different CMOS technologies

	0.13 µm	0.25 µm[6]
Die area	46800 μm^2	110000 μm^2
Nominal supply voltage	1.5 V	2.5 V
Operational supply voltage range	1...1.7 V	1.4...2.7 V
Temperature sensibility of reference voltage	+0.22 mV/K	-0.22 mV/K
Reference variation over supply voltage range	<10mV	<1mV
Nominal output reference voltage	0.587 V	1.175 V

Table 3 compares the main parameters for BGRs in two technologies. Although the circuits are based on different architectures, their main features may be compared as a BGR mostly is only referred to as a black box with exactly these specifications. The new 0.13 µm prototype shows lower die area, lower nominal and lower minimum supply voltage. The temperature sensibility is for both circuits in the same order of magnitude, the different sign is given by the different bias points. However, in terms of power supply dependence the prototype is still far off from the final 0.25 µm circuit. This will be corrected in the next version.

III. DUAL PORT SRAM

A. Circuit Presentation

The aim behind this design was to conceive a complete digital demonstrator circuit in the 0.13 µm CMOS technology, designed with enclosed devices, which could serve as a standard cell for a future digital library. A comparable cell had been designed in a 0.25 µm CMOS technology [7], serving as a benchmark in this test. This design is currently a major cell in several circuit developments for LHC ASICs, and the new conceived cell in 0.13 µm CMOS is foreseen to replace it on the long run. The main constraints in this development were – in order of importance - radiation tolerance, flexibility and modularity, die size and speed.

The circuit is a 1.5 V supply dual-port SRAM with a data range of 256x9 bits, organized in two 128x9 bit blocks. Figure 3 shows the internal architecture of the SRAM design.

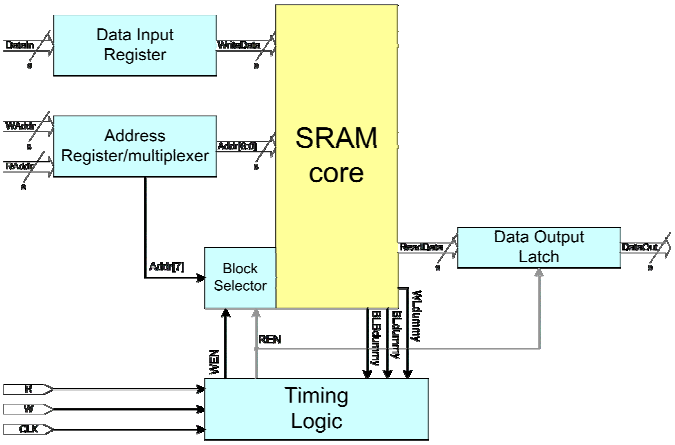

Figure 3: Block diagram of the dual port SRAM.

It consists of an array of single-port static memory cells coupled with the necessary write drivers and read logic circuitry, a row decoder, a column decoder, a set of registers for the address and the data input ports, a latch for the data output port and a timing logic circuitry controlling the operation of the SRAM macro-cell.

The macro cell is based on a conventional cross-coupled inverters design [7, 8] using PMOS pass transistors as access devices. The resulting size of the memory cell is only 3.73 µm x 2.58 µm. The layout of the cell using special layout techniques is shown in Figure 4.

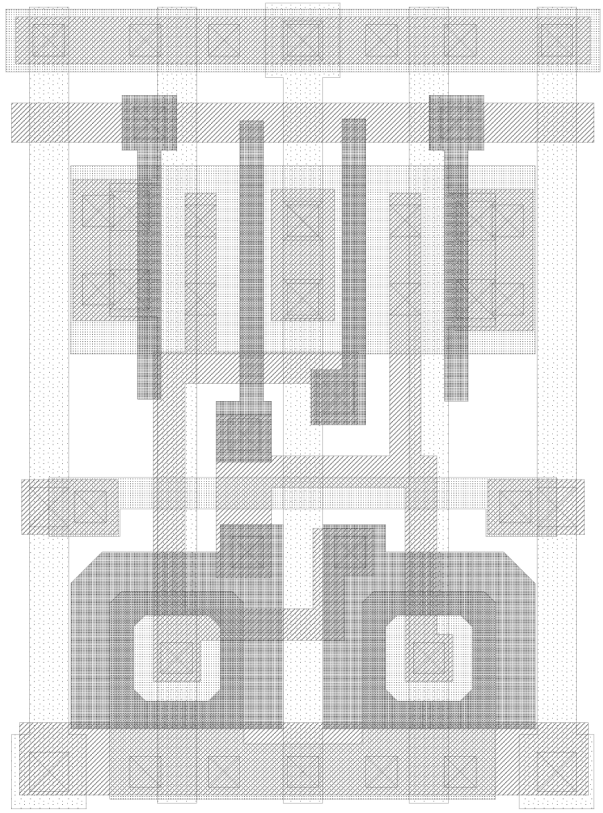

Figure 4: Layout of the SRAM memory cell using radiation tolerant layout techniques.

The complete SRAM core measures 553 µm x 129 µm, and was integrated as a rectangular chip of 1.84 mm x 1.90 mm with 46 pads.

B. Results

Several chips of this circuit were tested using CERN's mixed signal IC test system [9]. All circuits were fully functional for supply voltages above 1.6 V and frequencies up to 75 MHz, executing one read and one write operation within one clock cycle. The performance limiting circuit part was found to be the output drivers. The measured read access time was 5.1 ns.

Full reading functionality was possible for supply voltages as low as 0.8 V. Writing functionality was limited and could

not be guaranteed at nominal supply due to underestimated resistance of the bit lines resulting in too narrow sized pass transistors in the memory cell.

The power consumption of the chip is 3.84 mW at 25 MHz with an increase rate of 104 µW/MHz. The reason for this very high power consumption is understood and measures to decrease it will be made in the final design.

Although radiation tolerance was the most important design criteria, neither total ionizing dose irradiation nor single event upset (SEU) tests have yet been performed. Nonetheless, simulations on the SEU sensitivity of the memory cell have been executed, and the critical charge for upset was determined to be 12 fC. However, SEU cross section data for another memory in this technology, using linear devices, is already available and shows a saturation cross section in the order of 10^{-14} cm^2/bit [3]. We can thus assume a saturation cross section for this device below this value. This expectation is also supported by comparison of SEU results obtained with linear and enclosed designs in older technology generations [7, 10-12]. However, taking into account the TID hardness of this technology [3] and the reduction of the SRAM cell size with linear devices, it should be considered to use Error Detection And Correction (EDAC) means for SEU robustness instead of enclosed device geometry.

C. Comparison to 0.25 µm chip

A similar design had been developed in our 0.25 µm CMOS technology [7]. Table 4 compares the main parameters of both designs.

Table 4: Comparison of characteristics of dual port SRAMs in two different CMOS technologies

	0.13 µm	0.25 µm
Cell size	9.62 µm^2	47.15µm^2
Nominal supply	1.6 V	2.5 V
Access time	5.1 ns	4.5 ns
Maximum operation frequency	75 MHz	70 MHz
Power consumption @ 25MHz	3.84 mW	305 µW

In terms of data functionality the two chips show overall the same performance. However, the circuit produced in the 0.13 µm CMOS technology requires only one fifth of its predecessor's die size and is fully functional with only two third of the previous supply voltage. On the other side, its power consumption is far off expectations, but the reason for this is understood and will be corrected in a final version. There, additional speed gain will also be obtained as new I/O structures shall be available.

IV. 100 MHz Time To Digital Converter

A. Circuit Presentation

A time to digital converter (TDC) is a key circuit in high energy physics experiments and therefore an interesting circuit for our study. Two main motivations stood behind this development: the examination of the radiation hardness of a system designed without special layout techniques, and the need for a better understanding of the behaviour of mixed signal circuits at very low supply voltages.

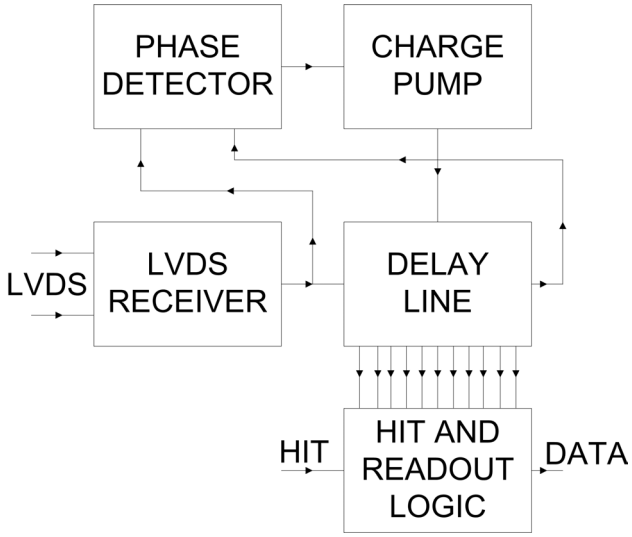

Figure 5: Block diagram of the time to digital converter.

Figure 5 shows a block diagram of this circuit. The TDC follows a well known approach based on a delay locked loop (DLL) [13, 14]. A differential clock signal is sent to the chip and acquired by a LVDS receiver, generating a single-ended clock signal. This signal is fed into an array of 128 delay cells. The phase input and (delayed) output signal of this array are compared with a phase detector controlling a charge pump which sets the delay of the delay cells. At the arrival of an impulse on the hit input, the current state of the DLL is captured into the hit registers and serially read out. This serial data pattern thus reflects the delay between the LVDS reference clock signal and the arrival of the hit impulsion.

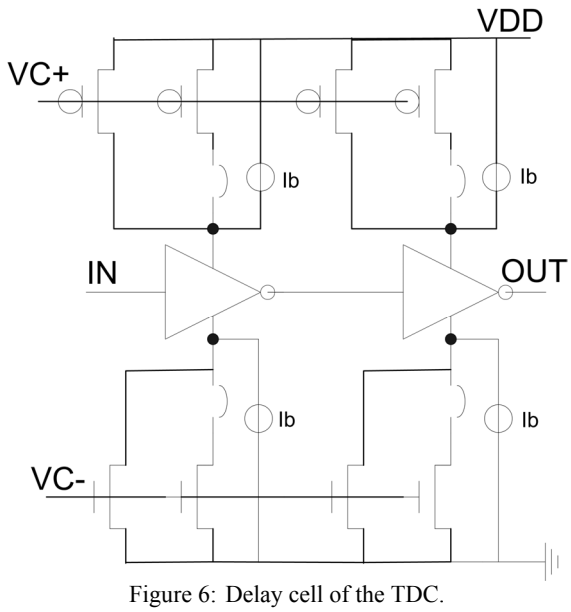

Figure 6: Delay cell of the TDC.

The main element of the TDC is the delay cell, shown in Figure 6. It consists of two current starved inverters. The current fed into the inverters is defined by the controlling voltages (VC+, VC-) generated from the charge pump and the number of parallel MOS transistors selected with an external signal, thus allowing to choose between a fast and a slow speed mode of the cell. Current bleeders – symbolized as current sources in Figure 6 - limit the maximum delay of the cell. The design was based on the most conservative transistors of this technology, namely regular NMOS and PMOS, thus allowing fabrication independent of device options available in a run. A single ended delay cell was chosen to allow for operation down to a minimum supply voltage of 1.2 V, where (faster) differential delay cells have already ceased to work. The nominal supply voltage of the circuit is 1.5 V.

B. Results

Several chips manufactured in nominal and slow process were tested with an input clock frequency of 100 MHz, leading to a theoretical bin size of 78.125 ps. All chips are fully functional and the DLLs locks in a supply voltage range of 1.2 V to 1.65 V.

1) Delay Characteristic

Figure 7 presents the delay characteristic measured on one circuit processed with nominal parameters, and one chip manufactured with slow process parameters.

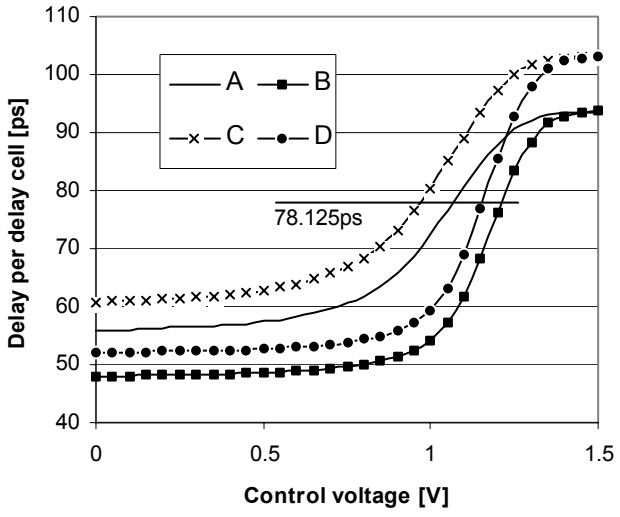

Figure 7: Delay characteristic of two chips with all operation modes at nominal supply voltage of 1.5 V: Chip manufactured in nominal process in its slow mode (A) and fast mode (B); chip manufactured in slow process in its slow mode (C) and fast mode (D).

The proposed architecture works at the requested speed for all tested chips, independently of process variations. The influence of different processes and speed modes can also easily be spotted. The delay of the slow process chips is on average 10 ps longer than that of nominal circuits. Assuming that fast process variations would take the delay characteristic symmetrically to the other side of the nominal characteristics, it can be concluded that at a bin size of 78.125 ps (or, for convenience, also 80 ps, requiring an input clock of 97.65 MHz), functionality of a production-ready chip could be guaranteed for all possible operation conditions and fabrication process variations. However, the further use of interpolation mechanisms [15] would allow bin sizes of one fourth of these results.

If, additionally transistors with either ultra thin gate oxide or low threshold voltages were used, we would estimate that a cell delay of 50 ps could be guaranteed with the same architecture of the delay cell.

2) Code Density Test

In order to determine the differential (DNL) and integral (INL) non-linearity of the TDC, code density tests (CDT) were performed [16-18].

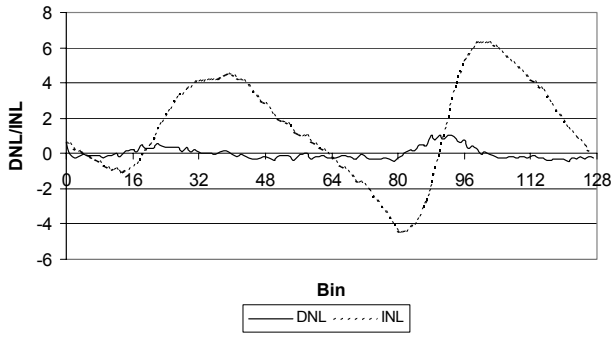

Figure 8: Differential non-linearity (DNL) and integral non-linearity (INL) versus delay line bin of the TDC. Characteristics based on 62464 random hits resulting in a tolerance of 7.5% for DNL and 42% for INL with a confidence range of 90% [19].

This test highlighted a maximum non-negligible DNL of 1 and a very high maximum INL of 6.3. We assume that these high values are caused by noise in the substrate, as we observed a dependency of the position of the relative maxima/minima on the duty cycle of the input clock signal. This higher level of noise is mainly caused by the high-resistive nonepitaxial p- substrate whose specific resistance is approximately 1000 times higher than in epitaxial substrates. A more thoroughly contacted substrate would thus allow to decrease the noise levels and subsequently DNL and INL.

3) Irradiation

One device was irradiated up to a total ionizing dose of 75 Mrd(SiO_2) with an applied dose rate of 28.3 krd(SiO_2)/min. It was biased and clocked during irradiation.

The device was fully operational after irradiation. The delay line characteristic, presented in Figure 9, showed changes within the measurement uncertainty; DNL and INL were within statistical limits of pre-irradiation results. As this TDC was completely designed without enclosed devices, it is

proved that high dose levels – as they could appear in future detectors - do not influence the general circuit behaviour.

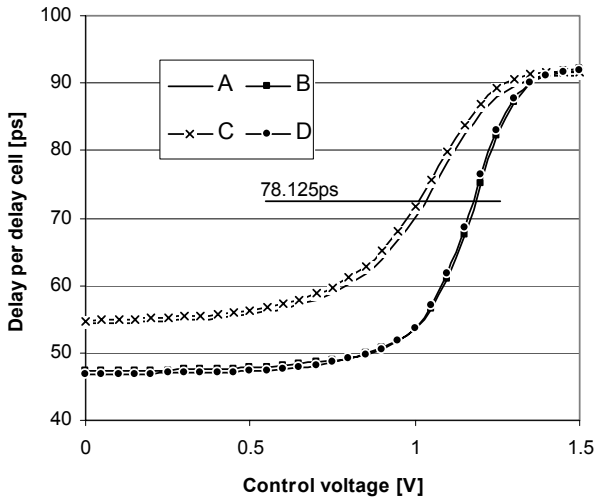

Figure 9: Delay characteristic of one chip with fast (A, C) and slow (B, D) operation modes at nominal supply voltage of 1.5 V before (A, B) and after (C,D) irradiation.

In the light of the TID tolerance of this technology [3], these results were expected. The only change was observed in current consumption as outlined in Table 5.

Table 5: TDC current consumption variation with and without total ionizing dose of 75 Mrd($Si0_2$) at 1.5 V

	Stand-by Mode (no input clock)	Full operation
Before irradiation	2 mA	49 mA
Immediately after irradiation	19 mA	73 mA
After one week annealing at room temperature	19 mA	72 mA

The measurements highlight that the major part of the higher current consumption is due to an increase in static power consumption. Annealing of one week at room temperature shows minor changes on the supply current towards the pre-irradiation value. Therefore, and also with respect to measured annealing behaviour of test vehicles (single transistors) in this technology [9], full annealing can be expected. We assume that this increase is mainly leakage caused by charge trapping in the field oxide above reverse biased diodes required for antenna protection [20-22].

V. Conclusion

CERN currently uses a commercial 0.25 µm CMOS technology with special layout techniques for its ASICs to be used in the LHC. As this very common process will phase out in the near future, we evaluated a commercial 0.13 µm CMOS technology as possible successor.

Based on first irradiation data pointing towards the possibility of inherent radiation hardness of this new technology, we realized and presented herein three prototype circuits of importance in the development of ASICs for detectors in this possible successor technology. Their results confirmed our expectations of radiation tolerance of systems. The prototypes show only negligible variations of parameters with radiation; even the circuits designed without special layout techniques. Taking into consideration the natural statistical spread of process parameters during fabrication, this technology is appropriate for harsh environments like in the detectors. We therefore can consider the use of a commercial library with this technology for future circuits foreseen for application in high energy physics environments. The study also confirmed other expected advantages of the 0.13 µm technology generation. The power consumption of digital applications will be reduced by up to 75%, and circuit size can shrink down to 20% of the size in a quarter micron technology, allowing producing more chips per wafer and thus decreasing per chip costs once this technology is available at reasonable prices. However, design challenges will appear to the analogue world where low voltage designs will have to be implemented and therefore new design strategies and guidelines will have to be followed.

VI. Acknowledgment

K. Hänsler is indebted to Jorgen Christiansen and Federico Faccio for the hints and fruitful discussions on the topic of time to digital converters.

S. Bonacini would like to thank Kostas Kloukinas for the constant support and the help on the design of the memory.

VII. References

[1] G. Anelli, M. Campbell, M. Delmastro, F. Faccio, S. Florian, A. Giraldo, E. Heijne, P. Jarron, K. Kloukinas, A. Marchioro, P. Moreira, and W. Snoeys, "Radiation Tolerant VLSI Circuits in Standard Deep Submicron CMOS Technologies for the LHC Experiments: Practical Design Aspects," *IEEE Trans. Nuclear Science*, vol. 46, no. 6, pp. 1690-1697, Dec. 1999.

[2] *International Technology Roadmap for Semiconductors,* Sematech, Inc., Austin, TX. Available www.sematech.org

[3] K. Hänsler, G. Anelli, S. Baldi, F. Faccio, W. Hajdas, and A. Marchioro, "TID and SEE performance of a commercial 0.13 µm CMOS technology", to be published in *Proc. 7th European Conference on Radiation and Its Effect on Components and Systems*, 15-19 September 2003, Noordwijk, The Netherlands.

[4] K. E. Kuijk, "A precision voltage reference source, " *IEEE Journal of Solid-State Circuits*, vol. 8, no. 3, June 1973, pp. 222-226.

[5] H. Banba. H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsume, and K. Sakui, "A CMOS Bandgap Reference Circuit with Sub-1-V Operation," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, May 1999, pp. 670-674.

[6] P. Moreira, "Bandgap Macro Cell in Quarter Micron CMOS", [Online]. Available at http://cern.ch/deepsub

[7] K. Kloukinas, G. Magazzu, and A. Marchioro, "A Configurable Radiation Tolerant Dual-Ported Static RAM macro, designed in a 0.25 μm CMOS technology for applications in the LHC environment," in *Proc. 8th Workshop on electronics for LHC Experiments*, Colmar, France, 9-13 September 2002, pp 319 – 323.

[8] K. Endo, and T. Matsumura, "Pipelined, Time-Sharing Access Technique for an Integrated Mulitport Memory,", IEEE Journal of Solid State Circuits, vol. 26, no. 4, April 1991, pp. 549-554.

[9] J. Christiansen, "Testing LHC Electronics," in Proc. *5th Workshop on Electronics for LHC Experiments*, Snowmass, CO, USA, 20-24 September 1999, pp 41-50.

[10] C. Poivey, B. Doucin, M. Brüggemann, R. Harboe-Sorensen, "Radiation Characterization of Commercially Available 1Mbit / 4 Mbit SRAMs for Space Applications," in *Workshop Record of 1998 IEEE Radiation Effects Data Workshop*, Newport Beach, CA, USA, 24 July 1998, pp. 69-73.

[11] E. L. Petersen, "The SEU Figure of Merit and Proton Upset Rate Calculations," *IEEE Trans. Nuclear Science*, vol. 25, no. 6, December 1998, pp. 2550-2562.

[12] C. Dyer, S. Clucas, C. Sanderson, A. Frydland, R. Green, "An Experimental Study of Single Event Effects Induced in Commercial SRAMs by Neutrons and Protons from Thermal Energies to 500 MeV," to be published in *Proc. 7th European Conference on Radiation and Its Effect on Components and Systems*, 15-19 September 2003, Noordwijk, The Netherlands.

[13] T. E. Rahkonen, and J. T. Kostamovaara, "The use of stabilized CMOS delay lines for the digitization of short time intervals." *IEEE Journal of Solid-State Circuits*, vol. 28, no. 8, August 1993, pp 887-894.

[14] C. Ljuslin, J. Christiansen, A. Marchioro, and O. Klingsheim, "An integrated 16-channel CMOS time to digital converter,", *IEEE Trans. Nuclear Science*, vol. 41, no. 4, pt. 1, August 1994, pp. 1104-1108.

[15] M. Mota, and J. Christiansen, "A high-resolution time interpolator based on a Delay Locked Loop and an RD delay line," IEEE Journal of Solid-State Circuits, vol. 34, no 10, Oct. 1999, pp. 1360-1366.

[16] J. Doernberg, H. S. Lee, and D. A. Hodges, "Full-speed testing of A/D converters," *IEEE Journal of Solid-State Circuits*, vol. 19, no. 6, Dec. 1984, pp. 820-827.

[17] B. Ginetti, and P. Jespers, "Reliability of code density test for high-resolution ADCs," *Electronic Letters*, vol. 27, no. 24, Nov. 1991, pp. 2231-2233

[18] M Bossche, J. Schoukens, and J. Renneboog, "Dynamic testing and diagnostics of A/D converters," *IEEE Transactions on Circuits and Systems*, vol. 33, no. 8, Aug. 1986, pp. 775-785.

[19] M. Mota, "Design and Characterization of CMOS High-Resolution Time-to-Digital Converters," *PhD-Thesis, Instituto Superior Técnico, Universidade técnica de Lisboa,* Oct. 2000, Appendix 4.

[20] W. Lin, "A multiple-terminal gate charging model," *IEEE Electron Device Letters (USA)*, vol. 24, no. 8, August 2003, pp. 521-523.

[21] C. T. Gabriel, and E. de Muizon "Quantifying a simple antenna design rule", in *Proc. 5th International Symposium on Plasma Process-Induced Damage*, Santa Clara, CA, USA, 22-24 May 2000, pp. 153-156.

[22] J. P. Carrere, and D. R. Heslinga, "Charge protection and degradation by antenna environment on NMOS and PMOS transistors," in *Proc. 4th International Symposium on Plasma Process-Induced Damage*, Monterey, CA, USA, 9-11 May 1999, pp. 184-187.