FEROM, The ALICE SSD read out system

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(For the ALICE collaboration)

Abstract

The main FEROM (Front End Read Out Module) task is the digitalization of the 2.6 million SSD (Silicon Strip Detector) strip values in 160 µs. This is achieved by digitizing in parallel the 1698 double-sided SSD module signals (each containing 1536 strip values). The FEROM also performs the zero-suppression and offset correction, the event-data de-randomization using Multiple Event Buffers (MEB) and the event data transfer to the DAQ.

The FEROM system consists of 8 6U VME crates, each containing 216 ADCs. These crates also interface with the CTP (Central Trigger Processor), DAQ and DCS (Detector Control System). Special precautions are taken to reduce SEU problems. As the FEROM is installed in the cavern and inaccessible during beam-time, much emphasis has been put on high reliability design techniques. JTAG is used to check connectivity of the large number of cables that go to the detector.

I. The ALICE SSD subdetector

The ALICE SSD sub-detector consists of 1698 SSD modules. Each SSD module (see Figure 1) consists of a double-sided SSD with 1536 strips (786 strips per side) and 12 HAL25 front-end chips.

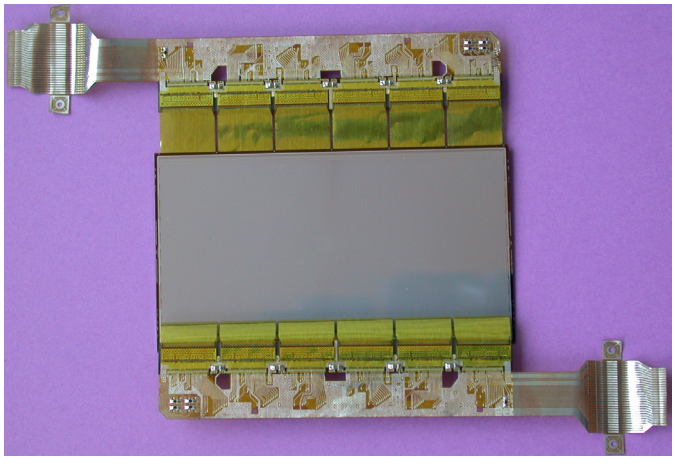

Figure 1: SSD-module

Each HAL25 [1] has 128 input-preamp-shaper-Sample/Hold circuits and an analog output multiplexer. The HAL25 has the following 5 control signal inputs: HOLD, RCLK (Read Clock), TK_IN (Token in), FSTRB (Fast Reset) and PULSE. The HOLD-input controls all 128 Sample/Hold-circuits in parallel. Under control of RCLK, TK_IN and FSTRB the analog output multiplexer forwards one of the 128 S/H circuit outputs to the HAL25 differential analog output buffer. A token passing mechanism allows the analog output buffers of several HAL25 chips to be connected together. This is achieved by daisy-chaining the HAL25 TK_IN and TK_OUT signals. The FSRTB can be used for resetting the output multiplexer, which is useful for quickly terminating the readout, e.g. in case of an L2r (=level 2 trigger reject). The PULSE input injects a specific charge into one of the input channels, which can be used for test and calibration purposes.

Each HAL25 also has a JTAG port, which can be used for control tasks like setting shaping time, setting the test-PULSE channel and bypassing the token when the HAL25 chip does not operate in a proper way.

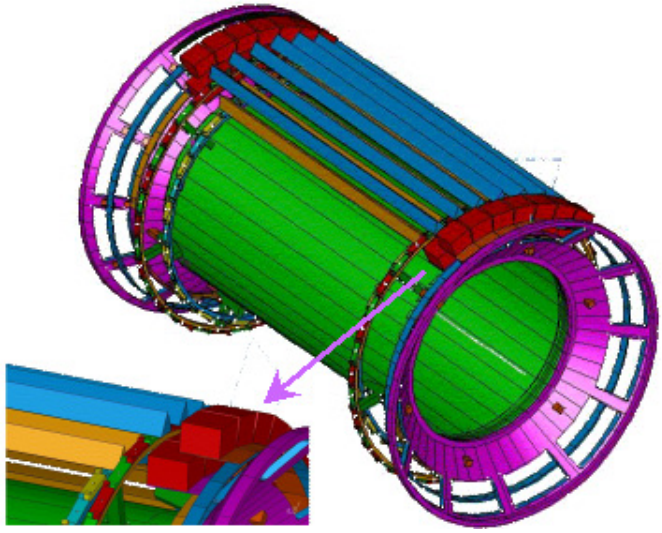

Figure 2: The ALICE SSD sub-detector: ITS layer 5 & 6.

The 1698 SSD modules are mounted on 72 ladders, forming two cylindrical silicon layers surrounding the interaction point. They are layer 5 and 6 of the ALICE ITS (Inner Tracking System). Each ladder end has an ECM (End Cap Module [2]), which provides the interconnection between the outside world and the (10…13) SSD-modules on a half ladder. Layer 5 ladders have 22 SSD-modules where 10 modules are connected to the ECM on one side and 12 modules to the ECM on the other side. For layer 6 (25 modules), these figures are 12 and 13.

Each ECM has a JTAG interface (for front-end configuration and interconnectivity check), readout out control lines (5) and (10…13) SSD-module analog output lines. The HAL25 token mechanism allows the ECM to have one analog output for each SSD-module. During readout, each analog output shows sequentially in time the 1536 strip values of the corresponding SSD-module. The ECM also has an error output signal to indicate token errors and power supply problems. The ECM also takes care of the double-sided SSD bias voltage difference by using a ground level separator.

Table 1: Numbers about ladders, ECMs, SSDs and strips.

Layer	# ladders	# ECMs	#SSD/ ladder	#SSD	#Strips
5	34	68	22	748	1148928
6	38	76	25	950	1459200
5+6	72	144		1698	2608128

II. FEROM SYSTEM

The FEROM system has the following 2 main tasks. First, after receiving a L0 trigger, the FEROM system will activate all ECM HOLD signals on the proper time and perform the read-out by driving the all ECM control signals and taking 1536 samples from each of the 1698 SSD-module analog outputs. Then the FEROM system performs the offset correction and zero-suppression and sends the unsuppressed data to the DAQ. The second main FEROM task involves the distribution of the JTAG to the ECMs.

A. FEROM system interface

To perform the tasks mentioned above, the FEROM has to interface with the following 5 systems (see Figure 4):

1) SSD sub-detector via 144 ECMs: Each ECM has a JTAG port, 5 control input signals, 1 real-time error output and 10…13 differential analog outputs. Digital signals are LVDS.

2) CTP [3]: The L0 trigger decision is distributed via copper cables. The L1 and L2 are distributed via the fiber optic TTC [4] system. The FEROM system BUSY flag goes via copper cable to the CTP.

3) DAQ: The FEROM-systems sends the unsuppressed measurement data to the DAQ via a bi-directional fiber optic link called DDL (Detector Data Link [5]). The DDL is also used for sending for each strip the offset correction values and zero-suppression thresholds to the FEROM system.

4) DCS: DCS accesses the FEROM system via a JTAG link.

5) Slow Control: accesses the FEROM via the CAN-bus.

B. FEROM system partitioning

The FEROM system is located in the cavern just outside the L3 magnet and interfaces with the ECMs via 25 meter long twisted pair cables. As shown in Figure 4, the FEROM system will be accommodates in 8 6U VME crates, 4 crates on each side of the magnet.

Each crate contains two 10 slots VME430 backplanes. Each VME430 backplane accommodates 1 link module and 9 AD-modules. The FEROM system also has 2 BUFMUX modules, one on each side of the detector. The BUFMUX module distributes the L0, and multiplexes the BUSY signals for the 4 nearest crates. The BUFMUX JTAG port allows masking and monitoring of individual BUSY signals.

C. FEROM

As shown in Figure 4, a FEROM is a combination of a V430 backplane, a link module and 9 AD-modules. Each AD-module interfaces with one ECM. . Since the whole FEROM-system has 144 AD-modules (& ECMs), much effort has been made to reduce the AD-module cost price.

Each AD-module drives the corresponding ECM JTAG and readout control-lines. The AD-module has only 12 analog SSD inputs. For ECMs with 13 analog outputs, the 13th output will be routed to a free input of an AD-module that interfaces with an ECM with only 10 analog outputs. Limiting the number of analog input channels to 12 allowed the AD-module to be implemented on a 6U high VME boards giving a significant cost reduction.

The AD module performs on the digitized SSD data the offset correction and zero suppression. The unsuppressed data are then stored in an event buffer. The link-module reads out the AD-module event buffers via the V430 backplane and sends the data to the DAQ. The ECM readout control signals are generated by the link-module, distributed via the FEROM-bus to the AD-modules where they are converted to LVDS and sent to the ECM. By keeping the AD-module functionality simple, low cost PFGAs can be used on the AD-modules.

1) AD-module

Figure 3 shows the AD-module architecture. The AD-module has 12 12-bit 10 Msps ADCs. Although digitizing the analog SSD-module signals with 10 bit resolution would be sufficient, the AD-module uses 12-bit ADCs which increases the accuracy and dynamic range. The extended dynamic range makes matching the ADC input range less critical, and allows the strip individual offset correction to be performed digital.

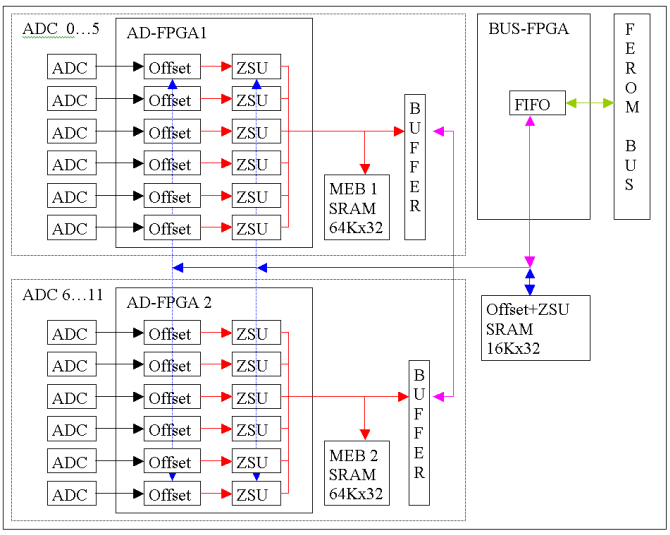

Figure 3: AD-module architecture

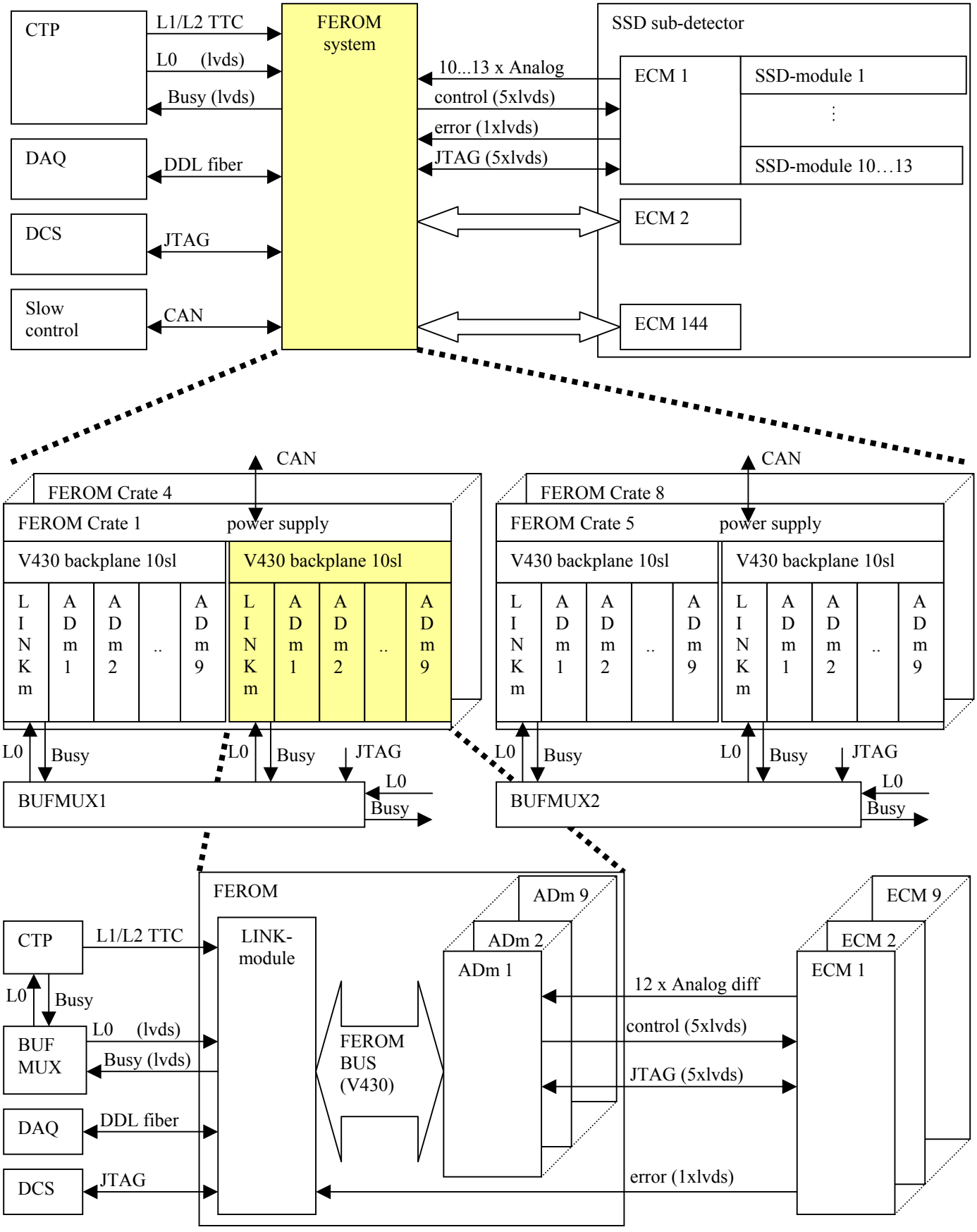

Figure 4: FEROM system interface, partitioning and architecture

As shown in Figure 3, the AD-module has 2 AD-FPGAs (Field Programmable Gate Array). Each AD-FPGA reads out 6 ADCs and adds parity bits to enable SEU detection. Afterwards, the AD-FPGA performs the offset and zero suppression for the 6 channels. The unsuppressed data is stored in a 4 deep MEB (Multiple Event Buffer). Compared to a SEB (Single Event Buffer), the introduction of the MEB reduces the deadtime from 400 µs (@ 5% occupancy) to almost the theoretical minimum, i.e. the ECM readout time (154 µs @ 10MHz readout clock). The BUS-FPGA interfaces between the MEBs and the FEROM bus.

For the MEB implementation, several memory technologies like FIFO, Dual Ported (standard, netram or FPGA internal), QDR, and SRAM were investigated. FIFOs are not suitable because data stored from rejected events (after L2r) cannot be removed from the FIFO. Dual ported memories would allow such actions by simply changing the address pointers, but is still rather expensive. QDR memories are not used to avoid high frequencies and high-density BGA packages.

SRAM is cheap, but has the disadvantage that it is inaccessible by the BUS-FPGA during ECM readout. This is not likely to be a problem because the ECM read-out will take place at most 10 % of time. So the SRAM is 90% of the time available for the BUS-FPGA. Moreover, the MEBs only contain the unsuppressed data, which is typical only 5%. This is also illustrated by **Figure 5**, which shows the maximum sustained trigger rate against the occupancy. The dual-ported MEB sustained trigger rate is constant, and limited by the ECM read-out time only. The SRAM-MEB sustained trigger frequency decreases slightly with increasing occupancy because of the additional time needed by the BUS-FPGA to readout the MEB. **Figure 5** also shows that the DDL (25 Mword/sec) and FEROM bus (60 Mword/sec) data bandwidth quickly put a limit on the sustained trigger frequency.

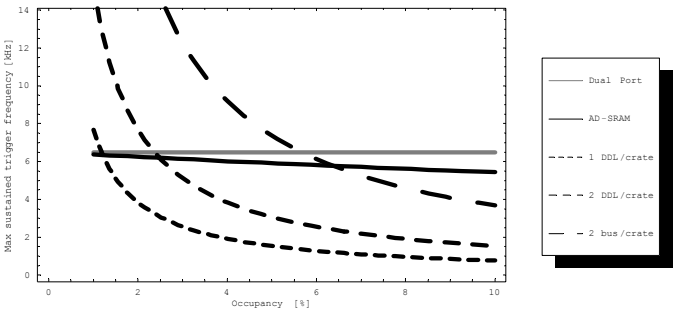

Figure 5: sustained trigger frequency for MEB and DDL.

2) FEROM bus

The link-module is connected with the AD-modules via the FEROM-bus. Several bus implementations have been considered like standard VME64, cPCI and a dedicated synchronous protocol on a standard backplane. The data bandwidth of standard VME64 is too low, and there is no 3,3V distribution, which is desired since most of nowadays digital circuits operate with 3,3V or lower. The dedicated protocol on a standard backplane is favoured above cPCI because of the low price and the large flexibility, e.g. it allows distribution of the proper power supply voltages (3,3V for digital, 1,8V for the FPGAs) and extending the data bus width for sending double words. Moreover, the dedicated protocol has been optimised for easy interfacing with the DDL.

Initially [6] a FEROM crate was to have one full size backplane with up to 19 AD-modules and one link-module with one DDL. To improve the sustained trigger rate, it has been decided to double the number of DDL-links by splitting up the FEROM backplane in two 10 slot backplanes, each containing 9 AD-modules and one link module with one DDL. **Figure 5** shows the sustained trigger rate increase after doubling the number of DDLs. Splitting up the backplane also reduces the range of single point failures.

Table 2: backplane features

Backplane	2 x 10 slots available at ESS	Slot Numbering	Extra IO
VME64	Yes	No	NO
VME64x	No	Yes	Yes
VME430	Yes	Yes	Yes

The initial [6] token passing protocol for sending event-data from AD-module to the link-module is sensitive to SEU and is replaced by a protocol where the link module addresses the AD-modules. For improved SEU immunity, the address comparator, which enables the AD-module bus buffers, is not implemented in the FPGA, but with TTL components.

The backplane must have slot numbering since this is used by the dedicated synchronous protocol (address comparators) and the JTAG-switches. The crates will be ordered via the CERN ESS group to ensure good availability and servicing and easy integration with the ALICE slow control systems. The crate power supplies and fan-trays have CAN port for slow control purposes. Table 2 indicates that the VME430 backplane fulfil all requirements.

3) Link-Module

The link module interfaces with the CTP, DAQ, FEROM bus and DCS. Almost all link module functionality is implemented in one FPGA, which simplifies the information exchange between the systems connected to the link-module. Using a FPGA also introduces a lot of flexibility.

For interfacing with the DAQ, the link-module accommodates the DDL SIU (Source Interface Unit). For interfacing with the FEROM-bus, the link-module FPGA provides the FEROM-bus controller functionality. For interfacing with the CTP, the link-module accommodates a TTCrq piggy-back. Besides triggers, the TTC–system also distributes a 40 MHz clock, from which the link-module can generate the RCLK (10 MHz) and system clk (60 MHz = 6 * RCLK, because the AD-FPGA multiplexes 6 input channels). The TTC allows the RCLK to run exact synchronous on the different FEROMs, which reduces the cross talk.

The TTCrq piggyback is preferred above the TTCrm piggyback because of the smaller form factor, which allows the link-module to occupy only one slot. The TTCrq also has

a QPLL, which provides a lower jitter clock, and can generate a (1,5 * 40) 60MHz clock directly.

Because of the many signals, the link module FPGA has a BGA package. The link-module has a small event-buffer, implemented with FPGA internal Dual Ported Memory.

The link-module will also accommodate the configuration PROMs for the link-module and AD-module FPGAs. Sharing the AD-module configuration PROMs introduces another cost reduction. Pin compatible radhard PROMs can be used if increasing SEU rates necessitate this.

D. JTAG

DSC communicates with the FEROM with JTAG. JTAG enters the FEROM on the link-module, via a front panel connector or via the DDL. The link-module distributes JTAG via the FEROM-bus to the AD-modules, from where it goes to the ECMs. The VME430 back plane daisy chain lines allows the creation of one large JTAG-chain, but one failure can corrupt the whole JTAG-chain. Therefore each AD-module (and link-module) has a multi-drop addressable JTAG switch. In this way the scope of a single point failure is reduced to the branch behind the switch. The subdivision of the JTAG chain with JTAG-switches also reduces the access time of individual JTAG-registers.

The JTAG-switch uses the VME430 slot number as identification address. The AD-module JTAG switch has 3 local JTAG ports. The signals from JTAG port 1 are converted to LVDS, and go to the ECM. JTAG port 2 goes to the FPGAs, which allows the detection and correction of SEU in the FPGA configuration data by readback and partial reconfiguration procedures. JTAG port 3 is used for DCS functions like reading the LED and power supply status.

Within the SSD sub-detector JTAG is used for 2 tasks:

1. control: e.g. setting the HAL25 shaping time, bypass HAL25 token or reading the ECM error status bits.
2. Testing the interconnectivity

The second function has now been extended because JTAG now also allows testing of the interconnectivity of the control signal cabling between the ECMs and AD-modules.

III. CONCLUSION

This paper presents the FEROM system, which is designed for reading out the ALICE SSD sub-detector. The FEROM system has the following features:

- Large dynamic input range by using ADCs with 12 bit resolution
- Low dead time by using MEB on AD-modules
- High data bandwidth bus with dedicated synchronous protocol
- High data bandwidth to DAQ by doubling DDLs

The FEROM system cost & complexity has been reduced by:

- Limiting the number of AD-module inputs to 12 (rerouting ECM output 13)
- Using SRAM based MEB
- By keeping the AD-module functionality as simple as possible, which allows the use of low cost FPGAs.
- Sharing the AD-module configuration PROM
- Using a low cost FEROM bus

Simulations [7] show that for 10 years of operation, the FEROM will be exposed to the following fluences above 20MeV: Total Ionising Dose: 4x10E-4 Gray, neutron fluence: 3.5x10E6, Proton, pion fluence: 2.5x10E5. Despite the low fluenes, the following techniques are used to reduce the SEE effects (SEU & latch up).

- Dedicated addressing protocol with ttl comparators
- Parity over the measurement data
- AD-module & link-module have poly switch fuses to protect the power supply system against latch up.
- JTAG can be used for FPGA configuration readback and partial reconfiguration

As the FEROM is installed in the cavern and inaccessible during beam-time, much emphasis has been put on reducing the range of single point failures:

- Split backplane, thus halving the number of channels per DDL link.
- Using JTAG switches
- Modular design (e.g. one AD-module interface with one ECM) optimized to minimize the loss of detector area in case of failures.

IV. REFERENCES

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