

# A testing device for the CMS Silicon Tracker Front End Driver cards

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## Abstract

A 9U 400mm VME FED Tester card (FT) has been designed for evaluation and production testing of the CMS silicon microstrip tracker Front End Driver (FED). The FT is designed to simulate both the tracker analogue optical signals and the trigger digital signals required by a FED. Each FT can drive up to 24 FED optical input channels. The internal logic of the FT is based on large FPGAs which employ fast digital logic, digital clock managers and memories. Test patterns and real tracker data can be loaded via VME to the memories. DACs operating at 40MHz convert the data to analogue form and drive the on-board CMS tracker Analogue-Opto-Hybrids (AOH) to convert the data to analogue optical format. Hence, they are identical to the signals produced by the CMS tracker. The FT either transmits the clock and trigger information directly to a FED or to the CMS Trigger and Timing Control (TTC) system. Four such cards will be used to fully test a FED. One FT prototype has been manufactured and is currently being used to evaluate the CMS tracker FED. This paper describes the FED Tester design and architecture.

## I. INTRODUCTION

The signals produced when charged particles pass through the silicon tracker are processed and stored within the analogue pipelines of APV25 ASICs [1,2]. On a positive Level 1 Accept (L1A) decision, the data from multiplexed pairs of APV25s are converted to analogue optical signals using the CMS tracker Analogue-Opto-Hybrid (AOH) [3,4]. These are transmitted from the detector to the Front End Drivers (FEDs) [5], located in the CMS counting room, via optical links.

Testing the FED prototypes requires a device that emulates both the tracker analogue optical signals and the trigger digital signals required for the proper operation of the FED. This is a challenging task because it requires the CMS Trigger and DAQ environment to be created 'on the bench' providing signals whose shape and timing is identical to those that will eventually be available at CMS.

A FED can receive data from 192 APV25s on 96 optical fibres. The front end is split into 8 sections, each of which digitises and processes data from 12 fibres. Each section contains a 12 way analogue Opto-Rx module [3, 4], 6 dual 10bit AD9218 dual ADCs [6], three Virtex-II

XC2V40 FPGAs [7] for ADC clock skewing and a Virtex-II XC2V1500 FPGA [7] which performs APV25 data frame recognition, common mode subtraction, pedestal subtraction and cluster finding.

The variable length clustered data fragments from the 8 front end sections are sent to a back end FPGA which collates the information into a single event and stores them in an external 2MB buffer to absorb fluctuations in the data rate. A VME transition card enables the events to be sent to the DAQ via 400MB/s copper links using the S-LINK64 protocol [8, 9]. Alternatively the events can be read via VME64x which will be used during system commissioning and for calibration and monitoring.

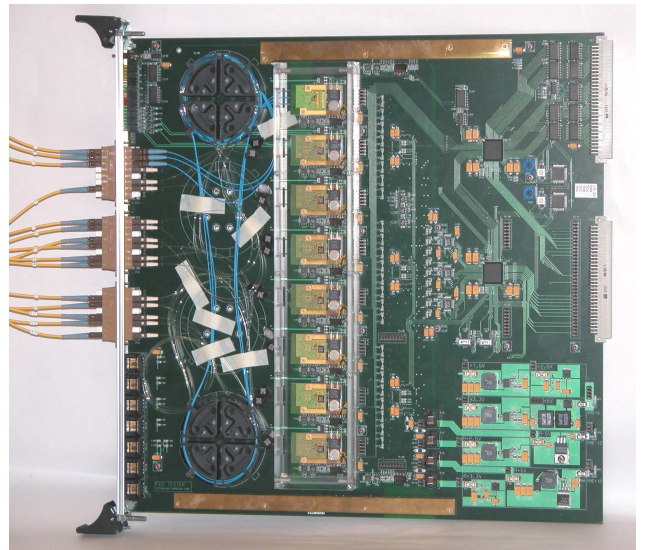


Figure 1: The FT with one 3-channel and seven 2-channel AOHs mounted underneath the perspex cover. Fifteen optical fibres can be seen connected on the left side of the photograph.

The immediate goal of the FT (fig. 1) is to verify the FED front-end, but it should also provide a versatile tool for debugging the FED back-end FPGA and S-LINK64 interface. The FT needs to be programmable so that it can accommodate any type of test pattern required to characterize the FED front end. It needs to be flexible, robust and compatible with the FED crate electronics and software so that it can eventually be used for large scale automated production testing. Finally it needs to be able to be loaded with real tracker data, which will have real hits,

pedestals and common mode noise, so that it can be used to perform validation tests of the FED cluster finding zero suppression algorithms. This last test is essential before commissioning the firmware of the FED algorithms for real data taking in 2007.

## II. REQUIREMENTS

The primary task of the FT is to mimic the data sent to the 96 fibre inputs on the FED by the APV25s on receipt of a L1A. The data consist of a pair of APV25 data frames multiplexed together. The APV25 frames comprise a 12 bit digital header followed by 128 analogue values (one for each microstrip) (fig. 2)

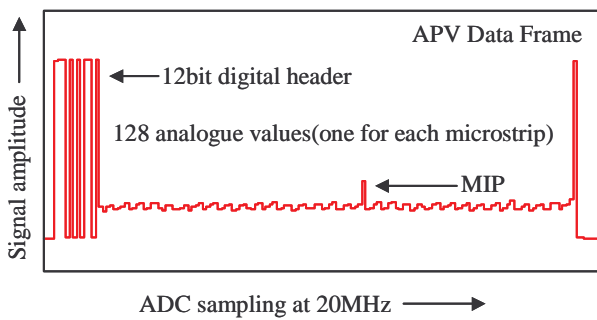


Figure 2: An APV25 data frame with a Minimum Ionising Particle (MIP) event in one strip.

A large number of these multiplexed frames will need to be sent to the FED to verify that it performs as expected. In addition to this the FT analogue performance should be sufficient that the analogue performance of all 96 channels on the FED can be characterised.

## III. ARCHITECTURE

The FT architecture is shown in figure 3. The logic is contained within two Xilinx Virtex II XC2V1000 FPGAs [7]. The VME FPGA acts as a VME to Wishbone bridge. Wishbone [10] is a set of rules for creating a standard interface to firmware cores thus making design re-use easier. This FPGA also allows I<sup>2</sup>C access to the AOHs and performs the AOH temperature control again via I<sup>2</sup>C. The System FPGA generates digital data for the three DACs and contains an emulation of the Trigger Control System (TCS) [11].

On the System FPGA the APV25 frame data for all 6 virtual APV25s (3 multiplexed APV25s) are stored in a 12bit wide by 233 deep frame pattern memory. This memory is quite small, but new frames can be uploaded "on the fly" without stopping the virtual APV25s. If this proves insufficient then the digital I/O daughter card region allows for memory chips to be added later. The 6 virtual APV25s access this frame pattern memory sequentially at 120MHz. Each virtual APV25 also has a 1k deep frame pointer memory that contains pointers to the start of frames in the

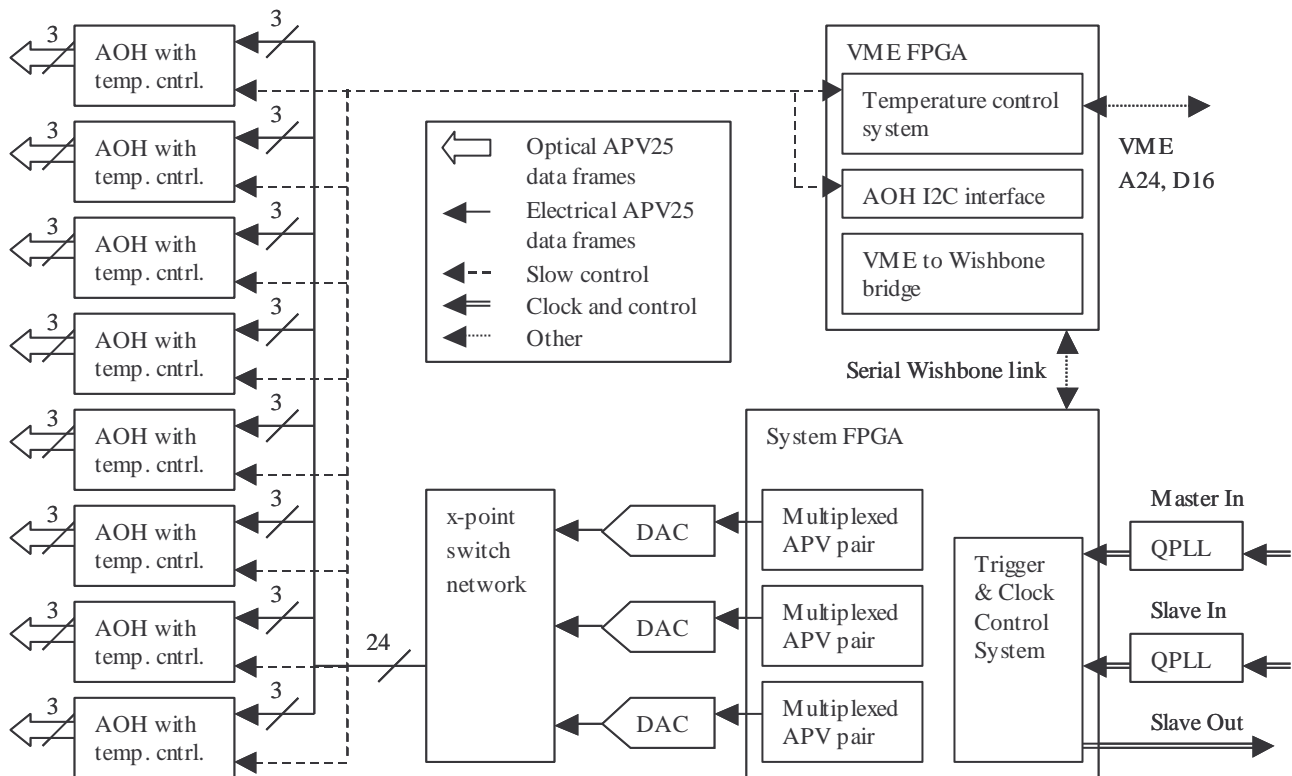


Figure 3: The FED Tester architecture

pattern memory. Consequently, the FT can receive 1024 LIAs before the sequence of frames is repeated.

The extracted frame pattern data is then multiplexed with the output from another APV25. It can then be delayed by up to 32 clocks to replicate fibre delays. To mimic fibre delays of less than the 40MHz clock period the DACs are driven by 3 separate clocks which can be skewed in steps of  $\sim 100$ ps.

The three AD9753 DACs [6] and an external input drive the three AD8108 programmable analogue cross-point switches [6] which act as a 3-to-24 fan-out. The outputs of the switches drive 8 CMS tracker AOH modules which convert the electrical signal to an optical signal for the FED channels. To supply 96 optical analogue inputs we will require 4 FTs. To ensure synchronisation between all of them they are all clock and control slaves while one of them is also a master supplying clock and control information from the TCS emulation. QPLLs [12] provide a redundant 40MHz clock that stays within the Xilinx FPGA clock specifications even after synchronisation loss.

The FT design is implemented on a VME 9U 400mm card which acts as an A24/D16 VME slave. The FT printed circuit board has 8 layers; 2 signal, 4 power and 2 ground. The board thickness is 2mm. All software has been written under the XDAQ framework [13] so that it is compatible with the FED. One FT has been built and has been integrated in the FED test setup.

#### IV. TEMPERATURE CONTROL OF AOHs

The AOH is temperature sensitive. This will not be a problem for the tracker because it will be operated at  $-10^{\circ}\text{C}$  at which the temperature sensitivity is less than at room temperature. Furthermore, the tracker temperature will be carefully controlled and the FED will apply a common mode subtraction to each APV25 data frame. However, the temperature in the laboratory has been measured to fluctuate by  $6^{\circ}\text{C}$  peak to peak and the AOHs are operated at  $\sim 30^{\circ}\text{C}$ . The AOHs are mounted on a 9U, 400mm deep VME card and thus for practical reasons its is not feasible to place them in an environmental chamber.

To decide whether an AOH temperature control system was necessary a prototype system of that used on the FT was built and used to investigate the magnitude of the AOH temperature sensitivity and evaluate if our control system would work. It was not intended as a detailed study of the temperature sensitivity of the AOH at  $\sim 30^{\circ}\text{C}$  and it should be noted that the results presented are from a single channel of one AOH. However, the limited statistics were sufficient to persuade us that a temperature control system was necessary.

The temperature sensitivity is shown in figure 4a in which the laser output is plotted versus laser bias current at different nominal temperatures for channel 0 of a 3-channel TOB type AOH. The actual temperature at which the measurements were made is shown in figure 4b. The temperature control system maintains temperature stability

to approximately  $\pm 0.2^{\circ}\text{C}$ , except at the nominal temperature of  $26^{\circ}\text{C}$ .

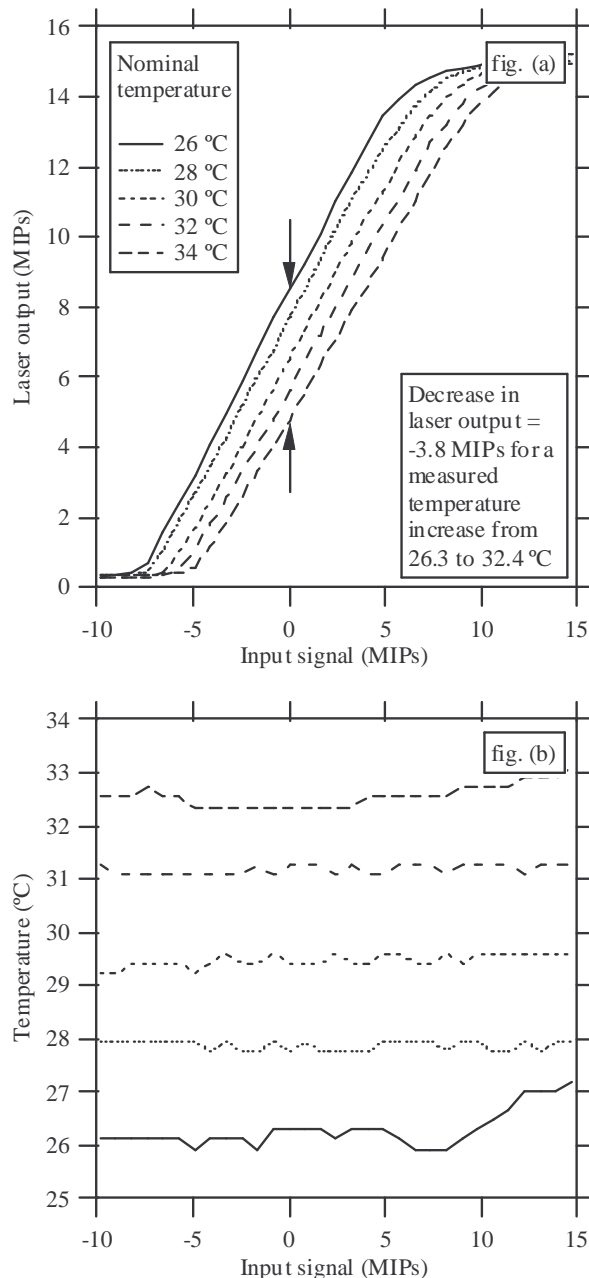


Figure 4: (a) The effect of temperature on the AOH laser output signal (b) The temperature measured for a given nominal set-point temperature. The key in (a) applies to both graphs.

At the lowest nominal temperature of  $26^{\circ}\text{C}$  the temperature gradient between the AOH and the PCB is too small to provide sufficient cooling to compensate for the heat being dissipated in the AOH at large laser bias currents. However, at these large laser bias currents the 12way Opto-Rx is already saturating and we are beyond the

+/- 4 MIP range required for the FT. Alternatively, if a larger temperature stability region is necessary the system can be operated at a higher nominal set-point temperature, although this will require more heating power.

The axis in fig 4 have been rescaled so that the laser output measured in volts by channel 0 of a 12 way analogue Opto-Rx is in MIPs. Similarly the laser bias current controlled by setting an I<sup>2</sup>C register in the linear laser driver [14] has been rescaled into MIPs.

The calibration was performed at 30°C and had 2 stages. The first stage consisted of determining the scaling factor to convert from laser output in volts to MIPs. The laser bias current register was set to 22, the centre of the laser output versus laser bias current transfer curve. The laser bias current was then modulated by driving a differential square wave of ~100kHz and magnitude +/-100mV, +/-200mV and +/-300mV into channel 0 of the AOH. The remaining 2 channels were driven with a 0mV differential signal. A MIP was defined as a differential signal of magnitude 100mV across the AOH termination resistors. A straight line graph of laser output in volts versus input signal in MIPs could therefore be plotted, with gradient providing the laser output in volts per input MIP.

The second stage consisted of re-plotting the laser output in volts versus laser bias current register setting as laser output in MIPs versus laser bias current register setting. The gradient of a straight line fit allowed the MIPs per register setting to be calculated and thus the laser bias current register axis for all temperature measurements to be rescaled in terms of MIPs.

At the centre of the transfer curve of laser output versus laser bias current the laser output was seen to decrease 3.8 MIPs as the temperature was increased from 26.3°C to 32.4°C, which is equivalent to ~0.6 MIPs/°C. To put this into perspective the nominal input range to the FED is 13 MIPs, of which the output frames from APV25s occupy 8 MIPs. Consequently, in the absence of a temperature control system we would expect large drifts in the input signals to the FEDs. The risk is that APV25 data frames drift out of the input range of a FED or that automatic APV25 frame finding logic within the FED fails because the digital header onto which the FED locks has fallen out of preset limits.

For precise analogue measurements it will be necessary to use common mode subtraction. The 128 analogue samples from an APV25 data frame are digitised in 6.4µs. Temperature fluctuations should not be apparent on these timescales.

A temperature control system was therefore developed. It relies on maintaining the AOH temperature a few degrees above ambient by supplying heat from a resistor via a thermal bridge. The temperature is monitored once per second by using a combined ADC/DAC to first measure the temperature. The data is then sent to an FPGA via an I<sup>2</sup>C bus where the optimum heating power is calculated with a PID algorithm. The latter should be better than a simple on/off switch because it should avoid temperature

overshoot/ringing and the average temperature should be the set-point temperature and not a degree or so below it. The heating power is written back to the DAC via I<sup>2</sup>C and the process starts again.

The temperature control system can be seen implemented in figure 5 which shows two AOH mounting positions with one occupied. Three optical fibres are exiting the picture in the top left. A brass support structure acts as a thermal bridge conducting heat generated in the large resistor on the right to the AOH. The same thermal bridge conducts heat down to the temperature sensor situated on the PCB.

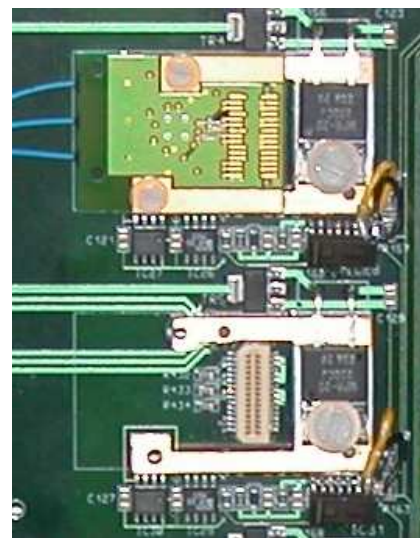


Figure 5: Two AOH mounting positions on the FT, with the top one occupied.

The main challenge is to insulate the structure sufficiently in order to obtain a sufficiently large temperature rise without dissipating too much power in the heating resistor. Consequently the thermal bridge is insulated from the PCB with perspex except for a small area close to the temperature sensor. A perspex cover (not shown) protects the AOHs and reduces cooling from air flow. The power planes are removed around the area that thermal bridge makes contact with the PCB and a perspex sheet is attached to the back if necessary to further reduce heat loss. This insulation is necessary to achieve ~10°C temperature rise with the resistor dissipating 0.7W. The low power consumption of the digital logic of the board has allowed us to increase the maximum power dissipation per heating resistor to 1.6W which should allow the system to absorb larger temperature fluctuations in the laboratory.

## V. TESTING

After ensuring that the FT powers up correctly the FT digital interconnects were verified with JTAG boundary scan. Preliminary tests indicate that all the firmware works as expected. The 3-channel AOH and seven 2-channel

AOHs that are currently mounted on the FT provide 17 optical outputs. All these appear to function correctly. The FT is currently being integrated into the FED testing set-up (fig. 6) and the first sets of data are being recorded. Preliminary measurements indicate that the analogue performance meets requirements.

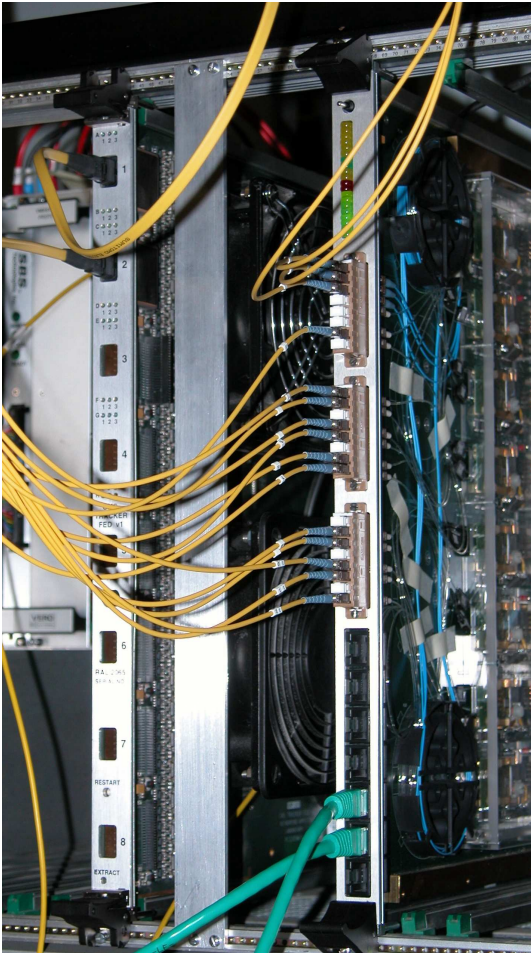


Figure 6: The FT (right) driving 2 out of the 8 FED (left) front-end sections. The FT shown was forced to use seven 2-channel AOHs and one 3-channel AOH and thus only 17 out of a possible 24 optical channels are being driven. Consequently, not all fibres in the 2nd FED front-end section are being driven.

## VI. FUTURE

The prototype FED Tester has passed preliminary tests and therefore a further 4 have been ordered and will be delivered within the next month.

In the meantime the prototype FED tester will continue to be used for debugging FED firmware and to speed up software development.

## VII. ACKNOWLEDGEMENTS

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