

# Data Concentrator Card and Test System for the CMS ECAL Readout

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## Abstract

The Data Concentrator Card (DCC) is part of the Off-Detector (OD) Electronics sub-system of the CMS Electromagnetic Calorimeter. The DCC is responsible for crystal and trigger data collection from the Front-End system and from the ECAL Trigger system respectively. From the DCC, data are transmitted to the central CMS DAQ system. This is done after achieving a reduction factor of 20 in order to get an average transmission data flow of 200 MByte/s. Data reduction is obtained through selective readout (SR) of calorimeter regions and the application of crystal zero suppression (ZS).

The test system includes a DCC Tester Card (DCC-TC), which emulates all the external interfaces to the DCC. In this paper we summarize the design architecture and functionality of the DCC and the DCC-TC and we describe the developed test bench.

## I. INTRODUCTION

The CMS ECAL comprises approximately 77000 PbW<sub>4</sub> crystals organized in supermodules, in the barrel, and in D-shaped modules in the endcaps. After amplification, crystal signals are digitised and then pipelined in the Front-End (FE) boards waiting for the first-level trigger decision (L1A). Each FE board deals with the data from 25 crystals, corresponding to one trigger tower in the barrel and one super-crystal in the endcaps. In parallel, these rad-hard boards compute the tower trigger primitives [1] in the barrel and the pseudo-strip energy sums in the endcaps.

In Fig. 1 the ECAL OD electronics and readout architecture are sketched. Trigger data or pseudo-strip energies from different FE boards are transmitted to the Trigger Concentrator Card (TCC). The TCC performs the final calculation of the trigger primitives in the endcap. After a non-linear compression [2] and synchronization [3], trigger data are sent to the Regional Trigger. The Selective Readout Processor (SRP) receives trigger data from the TCC and processes the selective readout flags [4]. The Clock and Control System (CCS) distributes the clock and control signals to the DCC, the TCC and the FE boards, being also responsible for their interface to the Trigger Throttling System (TTS) [1].

The DCC [5] is a common collection point for crystal and trigger data. After each L1A, the DCC collects crystal data transmitted from 68 FE boards (comprising one supermodule in the barrel) and trigger data transmitted from the TCC (1 TCC in the barrel and 4 TCCs in the endcaps). The DCC also receives the selective readout flags from the SRP.

The DCC main functions include opto-electric conversion and deserialization of the input data streams, verification of data integrity, reduction of the front-end data (through the combination of SR and crystal ZS), event formatting and its transmission to the CMS DAQ system. The DCC is also responsible for reading data from two monitoring channels (MEMs), and its transmission with the spy events to the local DAQ.

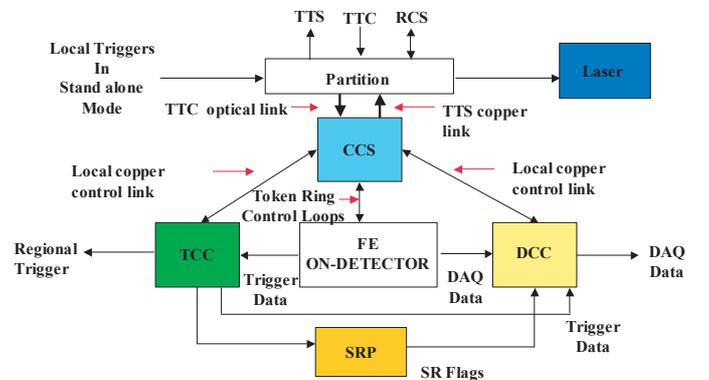


Figure 1: ECAL Off-Detector Electronics and Readout Architecture.

In order to proceed with the DCC prototype validation, a DCC-TC was developed. In Section II we describe the design and functionality of the DCC. Section III is devoted to the description of the DCC-TC. In section IV we present the developed test bench, and the raw data generation in order to simulate the input events. Finally, the summary can be found in Section V.

## II. DCC DESCRIPTION

The DCC is a VME-9U format board (Fig. 2), VME64x compliant, following the new proposed design rules for custom VME hardware in CMS [6].

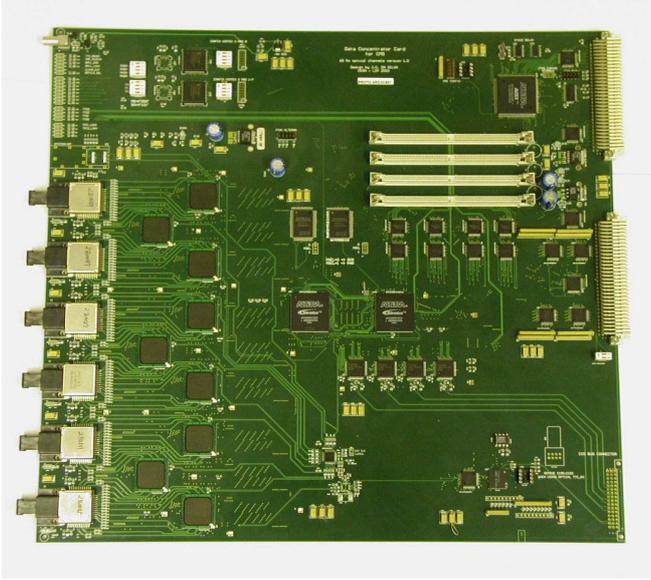


Figure 2: DCC prototype.

In Fig. 3 the DCC design architecture, which was motivated by the studies presented in [7], is shown. After optical to electrical conversion and deserialization into 16-bit words, input data enter the Receiver Block. For each input channel, the Receiver Block performs link and data integrity checks. The received SR flags indicate the level of suppression that must be applied to the FE data (no suppression, level 1 ZS, level 2 ZS, or full suppression). Data are stored in the input memories.

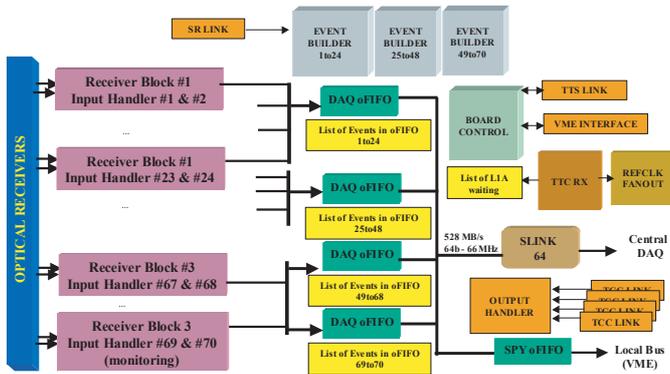


Figure 3: DCC Design Architecture.

The Event Builder assembles the collected data fragments in a single packet (DCC event), and stores it in the output memories ready for transmission. The Event Builder also monitors the input and output memories occupancy to prevent buffer overflows. If a first occupancy level is reached the TTS signal Warning Overflow is issued, requesting a reduction of trigger rate. In a second level a TTS signal Busy inhibits new triggers and empty events are stored. In case of buffer overflow the DCC enters in the error state.

The DCC event is transmitted to the central CMS DAQ using the S-Link64 [8] link. A spy memory is used for local DAQ, allowing VME access to full DCC events and monitoring

data. A combination of SR and ZS yields the necessary reduction factor ( $\sim 20$ ) of the incoming data with no significant effects in the physics reconstruction [9,10], resulting an average transmission data flow of 200 MByte/s. The output data rate is limited by design to a maximum of 528 MByte/s.

### III. DCC-TC DESCRIPTION

The DCC-TC is a VME-9U format board (Fig. 4) and was developed to emulate the interfaces between the external sub-systems (FE, TCC and SRP) and the DCC.

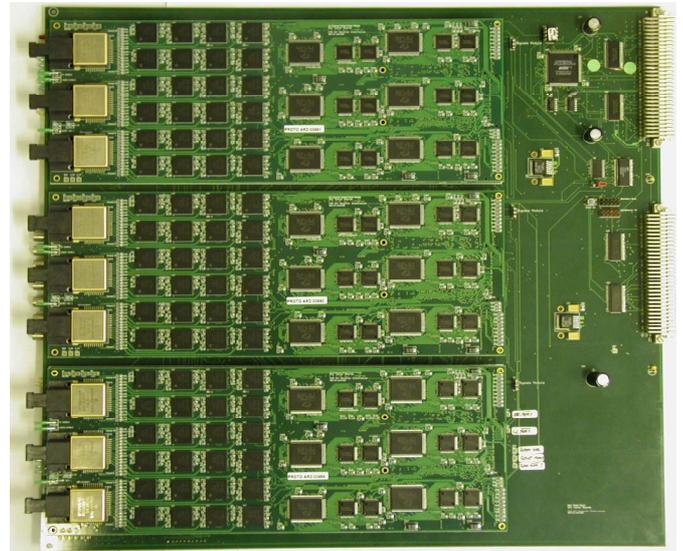


Figure 4: DCC Tester Card.

In Fig. 5 a scheme of the DCC-TC design architecture is presented. The Optical Module (OM) emulates the FE interfaces. Each one of these mezzanine cards has 24 Gigabit Optical Links (GOL) [11] and 3 eight-channel optical drivers. The 3 OM comprise 72 channels, but only 70 are effectively used: 68 for the FE channels and 2 for the MEM channels. The TCC Transmitter emulates the TCC interface through 4 electrical LVDS connections. The SR Transmitter emulates the SR interface through a GOL chip and a single optical driver. The DCC-TC was designed to store approximately 1000 simulated events. Both the TCC and the SR Flags Transmitters have one dedicated memory (8 MBit) for trigger data and SR flags storage. Crystal data are stored in the OMs with a storage capacity of 4 MBit/channel. The trigger position of each event, namely, the bunch crossing (bx) position and the orbit number are stored in the trigger-orbit memory (8 MBit).

The Trigger Timing and Control (TTC) [12] system provides distribution of timing, trigger and fast control signals. The DCC-TC controls the operation of the TTCvi by generating the LHC clock, the orbit signal, the LIA and the fast commands (bx reset, event counter reset, reSync, and monitoring commands).

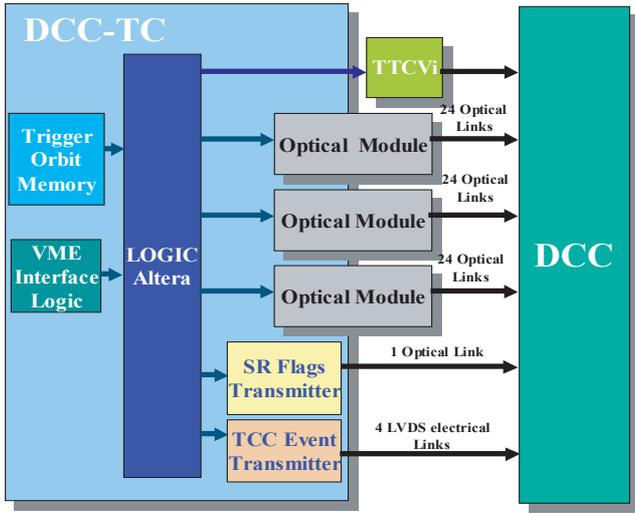


Figure 5: DCC-TC Design Architecture.

The DCC-TC is able to generate physic and monitoring triggers. Physic triggers are generated by issuing a L1A for each trigger position. After generation of the L1A, the FE data, the SR flags and the trigger data for the corresponding simulated event are transmitted. Different latencies can be specified among the different data transmitters. The monitoring triggers (laser and test pulse) are generated with a programmable orbit rate and a programmable bx position. The bx position must lie in the gap region ( $bx \in [3446, 3564]$  position of the LHC bunch pattern). Monitoring triggers are identified through the TTC commands prior to the L1A transmission. During monitoring triggers, the SR and TCC transmitters are disabled.

Four trigger operation modes have been foreseen: the step mode (triggers are transmitted individually upon a VME step command); the continuous mode (triggers are transmitted continuously until a VME stop command); the reSync mode (triggers are transmitted continuously followed by a reSync procedure) and, the auto stop mode (only a programmable number of triggers are transmitted).

#### IV. TEST BENCH AND RAW DATA GENERATION

In Fig. 6 we represent a diagram scheme of the test bench used for testing the DCC.

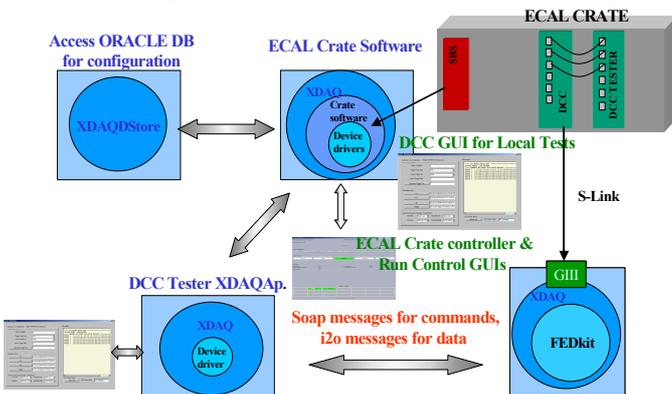


Figure 6 : DCC Hardware and Software Test Setup.

In terms of hardware this comprises a VME-9U crate with a VME-PCI interface, a TTC system (not shown in the picture) and a DCC-TC connected through the required links to the DCC. A generic PCI GIII receiver board [13] is also foreseen to test the DCC S-Link port.

The test system includes software for control, monitoring and configuration of the DCC [14], the DCC-TC and the GIII receiver card [15]. These software are developed in C++ and in the XDAQ[16] environment (the official framework for the CMS distributed DAQ). The DCC and the DCC-TC configuration were specified following the Generic Configurator Model [17,18]. Software for raw data generation, which is performed with the CMS physics simulation and reconstruction software [19], was also developed.

Raw data was generated for jet events ( $50 \text{ GeV} < E_t < 100 \text{ GeV}$ ), which are representative of the CMS triggered events. High luminosity ( $L \sim 10^{34} \text{ cm}^2/\text{s}$ ) was assumed, corresponding to approximately 17 pileup events per crossing. The simulated data were made persistent as ASCII files. After configuring the boards in the crate, the simulated files are parsed and software objects representing the DCC input data blocks are instantiated (Fig. 7).

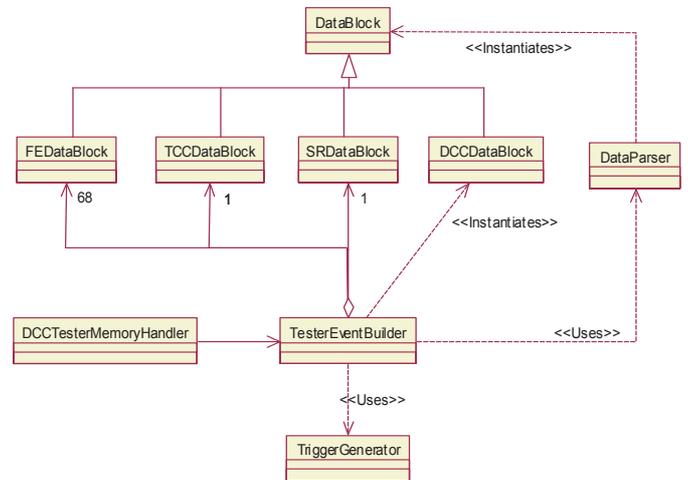


Figure 7 : Data Simulation UML[20] Model.

A trigger generator class is responsible for the simulation of the trigger bx and the orbit number through a Poisson generator, also ensuring that the CMS trigger rules are fulfilled [1]. Different trigger conditions can be tested with the same data. The data blocks objects are updated with the trigger information, which implies an update of the word parity of the headers and the data block trailers.

The constructed data are loaded in the DCC-TC memories. Simultaneously the DCCTester xdaqApplication request to the ECAL Crate Controller the actual readout configuration of the DCC (DCC active channels, readout operation mode, ZS thresholds and crystal weights applied to the ZS algorithm).

Based on the DCC readout configuration the Tester Event Builder emulates the expected DCC events. The DCC-TC transmits data that are processed by the DCC. The output events are made available through the DCC spy memory or the GIII receiver card and finally compared with the emulated events.

## V. SUMMARY

It was described the design and functionality of the DCC and the DCC-TC. The developed test system will allow testing the DCC in LHC-like conditions. The test bench was developed in a distributed environment and is well suitable for DCC laboratorial or on-experiment integration tests.

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