A solution to reduce the latency of a Multi Gigabit Transceiver (Virtex-II Pro). Effect of clock jitter on the Bit Error Rate.

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Abstract

The data transmission between the CMS ECAL sub detector and the experiment counting room is based on serial data links. It has been shown[1] that the use of the embedded receiver in a FPGA device from XILINX is a possible solution to reduce the cost of multi thousand links architecture. Unfortunately, the device latency does not satisfy the ECAL trigger data path requirement. A solution to reduce the latency and to synchronize multiple links is described in this contribution. In addition, when the synchronous LHC clock distribution scheme is used an additional clock jitter margin exists and it has no effect on the BER[2].

I. INTRODUCTION

In the CMS Electromagnetic Calorimeter (ECAL), high speed links operating in the Gbit/s range, transmit both raw and specific trigger data. Unlike the raw data, the trigger data require low latency to minimize the data storage inside the detector until the trigger decision is available. Moreover, for the high speed links a bit error rate (BER) of 10^{-13} per channel is required.

- Many commercial discrete transceiver devices are available on the market today. Recently, some FPGA vendors have started embedding serial transceivers in standard FPGA devices. In the most typical application domain for this technology (telecom systems) a local clock, embedded in the data stream, serializes the data. At the receiver side, another local clock resynchronizes the retrieved data. Specific clock correction hardware is then necessary to manage the sliding effect (phase incoherency) exhibited by the local clocks crystal oscillator. This additional hardware induces a substantial latency unacceptable for the HEP applications. As the LHC provides a specific distribution of synchronous clocks at the transmitter and receiver side, thus no clock correction circuitry is required. This paper reports a possible solution to reduce the receiver latency.
- A serial link requires a low jitter reference clock to work in the Gbit/s range. This characteristic is mandatory for both the emitter and the receiver. With the specific LHC architecture and using the ECAL electronic components, the clock jitter influence on the BER has been studied.

This contribution describes a solution to reduce the latency of a multi gigabit transceiver (MGT[1]) embedded in a XILINX's FPGA. Moreover the results of BER measurements with a calibrated jitter injection on the reference clock of the MGT are presented.

II. A SOLUTION TO REDUCE THE VIRTEX-II PRO MGT "LATENCY"

A. Overview

The Virtex2Pro FPGA family from XILINX can embed 4 to 24 Multi Gigabit Transceivers (MGT) on the same die. Moreover a versatile approach preserves the same package compatibility. Thus 8, 12 or 16 MGTs can be available on the same FF1152[3] package and two PowerPc[4] processor blocks can also be used at same time. In the lower cost package FG456[5], 8 MGTs and one PowerPc processor block are available. Serial data links concentrator solution can be based on these devices for HEP experiments.

The LHC clock distribution scheme guarantees that the same clock is available on both sides of the serial links. In a first approach, this architecture does not need the clock correction circuitry available on the MGT. Clock correction is based on the use of an elastic FIFO[6] buffer to compensate the clock frequency sliding between the local and the recovered clocks. The "write pointer" of the FIFO is under control of the RXRECCLK clock (recovered from data stream), whereas the "read pointer" FIFO is controlled by the RXUSRCLK (from the FPGA fabric). RXUSRCLK is derived from the REFCLK, a low jitter reference clock used to drive the MGT. The dynamic gap between pointers is under control of the clock correction logic that accommodates the differences between the clock rates. For the BER measurements versus the clock jitter (next section), it was observed that the elastic buffer could not be

[1] 8th Workshop on Electronics for LHC Experiments September 2002 at Colmar/France (LHCC-G-014)
[2] Bit Error Rate, unit used in digital serial communication to measure the quality of a serial link
[3] Flip-Chip Fine-Pitch BGA package (1.00 mm Pitch)
[4] PP405 Embedded Processor bloc from IBM
[5] Fine-Pitch BGA package
[6] First In First Out memory

used in the synchronous clock distribution mode. But it was tested and compared with a more classical one using two separate clock sources.

To reduce the latency, XILINX provides a design based on a CUSTOM primitive able to take control of the elastic FIFO buffer pointers. On average, the elastic buffer adds a delay of about 18 RXUSRCLK cycles from RXP/RXN (serial data stream differential inputs) to RXDATA (deserialized data outputs). The latency can then be mainly controlled by moving forward the "write pointer" by 17 or 18 cycles while the "read pointer" is kept fixed (figure 1). Consequently the gap between them is reduced to one or two cycles. The "read pointer" could still be at one or two clock cycles from the "write pointer", depending from the phase between the RXUSRCLK and RXRECCLK. This procedure reduces the total MGT latency from about 25 to 9 clock cycles while preserving safe clock domain crossing (see the time distribution in table 2.7 "Latency through various receiver Components/Processes" of the Rocket I/O Transceiver User Guide[1]).

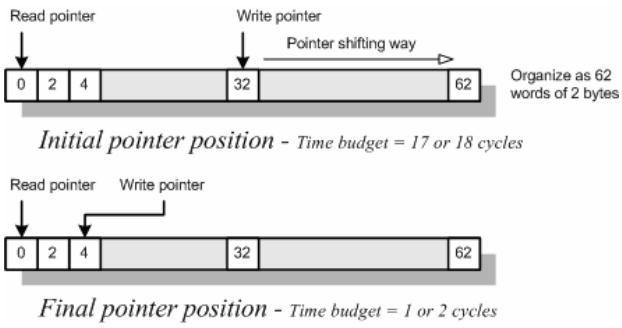

Figure 1 : Elastic buffer pointer positions after the reset and the low latency setting.

B. Setup Implementation

As previously described, it is suitable to choose a scalable implementation that can be easily replicated to all the MGTs of the same device. Special attention must be given to:

- **The available resources**. For example, to guarantee that specific available hardware in limited number (clock multiplexer buffer (BUFMUX) or low skew lines) can be used for all MGTs present in a chip. A MGT can then be interfaced to an output data bus of one, two or four bytes. A two bytes interface is the only one that features a 1:1 frequency ratio between RXUSRCLK and REFCLK. Using this scheme guarantees that no additional resources (DCM[7], BUFMUX) are necessary.
- **Shared block**. The latency controller logic requires a BUFMUX primitive for each MGT. However, as the BUFMUX (16 max in the chip) is used to drive all clocks inside the FPGA, a specific solution must be find for an architecture using the 16 embedded MGTs. Sharing the latency controller between several MGTs can perhaps satisfy this requirement. A test of this hypothesis is under way.

The use of MGT requires a REFCLK dock with a low jitter (dependent on the data stream rate). To satisfy this requirement we have chosen to directly connect this clock to the MGT via a dedicated input.

In the foreseen ECAL HEP application only the receiver part of a MGT is used, and the transmitter function isn't implemented. However, for auto test purposes, it can be useful to use the embedded loop back test features by implementing the transmitter function. It was used in the present GOL[2]–MGT interconnection study. An embedded tester is coupled with each MGT interface to perform the BER measurements. This suggests that it could be useful to implement a PRBS[8] to test in situ the quality of each serial link used for the ECAL FE[9] data links.

C. Tests

A test environment using the ML32x MGT characterization board from XILINX has been setup. The latency reduction of a single MGT was first successfully tested. A design applicable on up to 8 MGTs on the same Virtex2Pro device, including the latency controller and an embedded tester is now under test at LLR using two GOL test boards connected to the ML32x board. A QPLL[3] based solution test will be undertaken in a near future.

III. BER Measurements versus Clock Jitter

A. Overview

In a previous project phase[4], a BER test platform developed by XILINX Design Services (XDS) was used to study the GOL-MGT connection. This platform has been reused to study the effects of the LHC clock jitter on the BER. Tests were performed for an 800 Mbit/s link speed. The main motivation of the present test was to measure the real jitter margin available for the GOL-MGT connection. The configuration of the MGT was based on a standard "Ethernet" primitive where the elastic buffer is in use. This last characteristic is essential to be able to run a test with two different clock sources on each side of the serial link.

The test environment setup, as described in reference[4] is directly issued from the one used by XDS. The capability to inject a programmable calibrated jitter and to drive two GOL test boards at the same clock frequency has been also implemented. This implies a high stability pulse/pattern generator coupled with an arbitrary waveform generator

[7] Digital Clock Manager, based on Delay Lock Loop (DLL) and use to perform clock de-skew, frequency synthesis and phase shifting

[8] Pseudo Random Bit Sequence, electronic system used in telecommunications to provide a pseudo random sequence of data bits

[9] Front End electronic board used in ECAL/CMS

used as a clock noise source. The noise signal drives the control input delay of the pulse/pattern generator. So we can generate a clock output convoluted with a jitter depending of the noise level. Figure 2 shows the configuration of the test platform. The ML32x board provides a direct measurement of the BER and of the synchronization loss for the serial link under test.

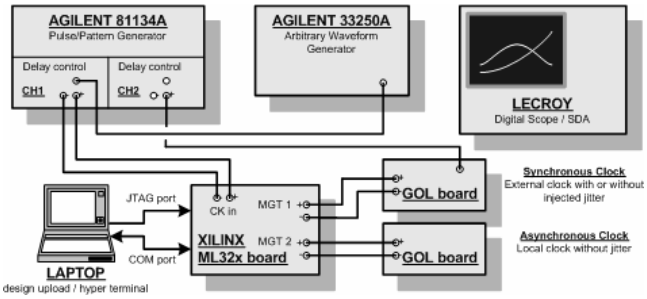

Figure 2 : The test platform

B. Jitter function characterisation

The transfer function of the pulse/pattern generator and the noise source, have been characterized. Figure 3 shows the three representation domains of the noise produced by the arbitrary waveform generator. Figure 4 exhibits the jitter versus noise voltage control for the AGILENT 81134A pulse/pattern generator used to study the effect of the jitter onto the BER.

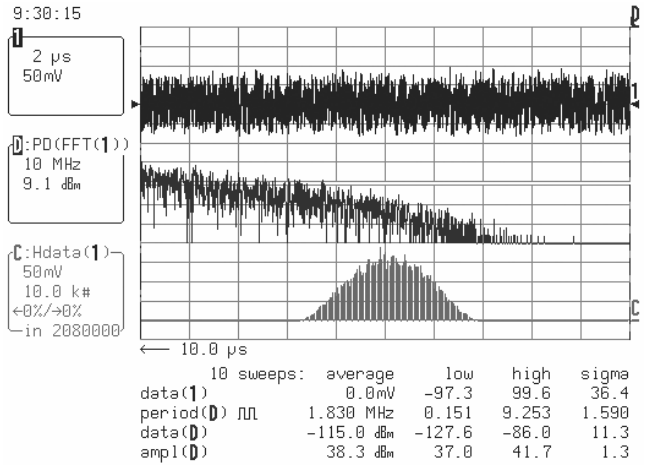

Figure 3 : Injected noise analysis. The upper waveform gives the time domain. The middle one show the frequency domain (Power Distribution with a FFT) and the lower one depicts the Probability Density Function (PDF) of the noise which as expected has a Gaussian shape.

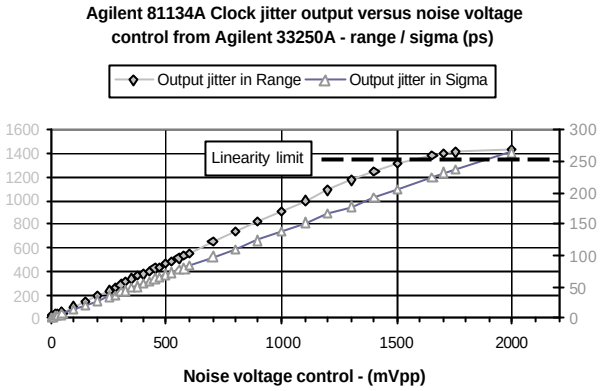

Figure 4 : Transfer function of the pulse/pattern generator. The left/right vertical scales give the jitter range (ps) and the jitter sigma dispersion (ps).

C. BER and Synchronisation Loss measurements

A dedicated logic and a PowerPc processor embedded in the FPGA on the ML32x board are used to analyse the received data and perform the measurements. The PowerPc gives access to the data and displays them via a RS232 interface. In the setup, a noise source was added to the MGT reference clock. No noise was injected on the GOL reference clock.

The measurements were first made for the asynchronous clock scheme. In this mode, the GOL test board uses its own clock source. In a second phase, the pulse/pattern generator providing an 80 Mhz clock to the MGT board was connected to the GOL board with a fixed time delay.

Figure 5 shows the results. A 10^{-13} BER value is taken as reference, based on the serial link ECAL-CMS experiment requirement. The two clock scheme results are compared to this requirement. A statistical confidence level function has been applied to the raw measurements. The tolerable jitter in the asynchronous mode can be as large as 330 ps peak to peak, at 800 Mbit/s transfer speed. This value is significantly larger than the XILINX specification for higher MGT transfer speed (40 ps at 3.125 Gbps). Moreover, an additional 85 ps jitter margin is available for a synchronous distribution clock scheme like the LHC one. These measurements show that an improvement of one order of magnitude in BER is achieved for the synchronous scheme. Figure 6 shows results obtained under the same conditions for the synchronisation loss.

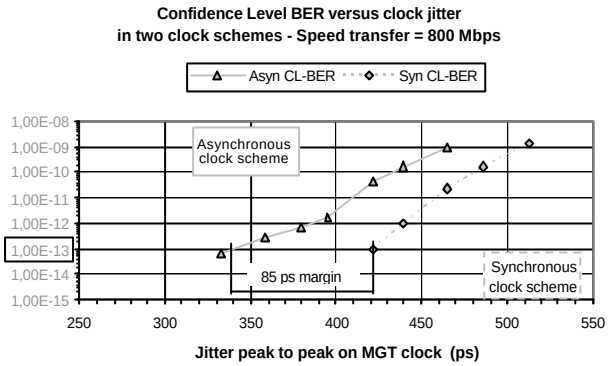

Figure 5 : BER measurements

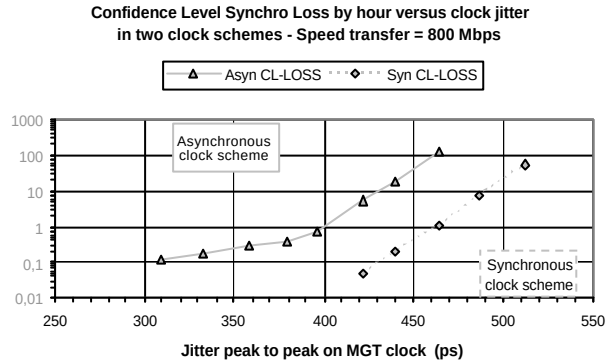

Figure 6 : Synchronization loss measurements

D. Effect of the Distribution Clock Scheme on the Latency

The effect of the clock distribution scheme on the latency has also been checked. Figure 7 shows a 25 ns uniform jitter distribution of the latency (one clock source period) for asynchronous mode (sliding phase effect of the two clock sources). For the synchronous distribution mode (figure 8) the latency jitter is nearly constant.

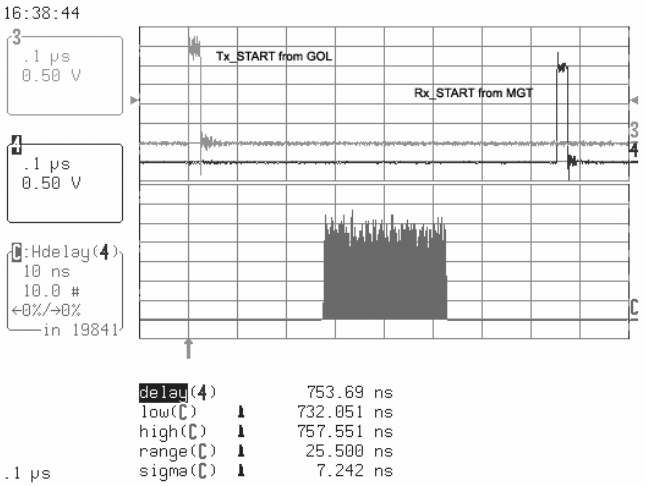

Figure 7 : Latency delay distribution in the asynchronous mode

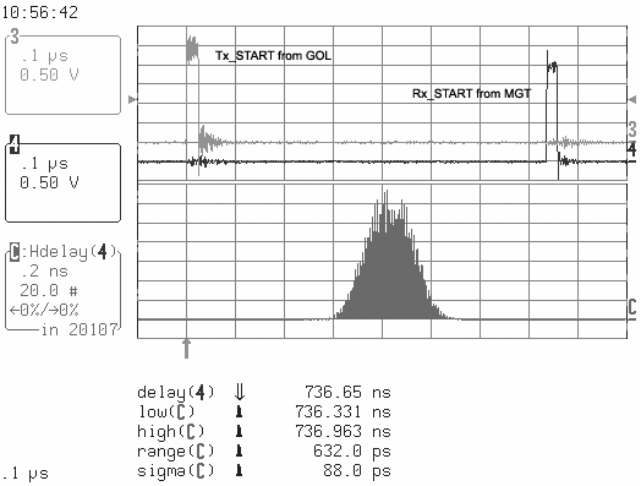

Figure 8 : Latency delay distribution in the synchronous mode. The Gaussian shape, of this jitter, characterizes a pure random source.

IV. CONCLUSIONS

It has been shown that a MGT custom primitive can be used to reduce the latency budget from 18 to 9 clock cycles. It entails an adjustment of the write pointer of the internal elastic FIFO buffer during the reset initialization phase. This solution is directly applicable to the LHC experiments thanks to their specific synchronous clock distribution. It will provide a more integrated solution and an interesting economic alternative to the current approach based on discrete transceivers. A review of the latency budget for the trigger data path has to be envisaged.

In the second section, we have shown that the LHC synchronous distribution clock scheme provides a substantial jitter margin when compared to a more classic asynchronous approach while still meeting the BER requirements. Moreover, for the 800 Mbit/s speed rate, the MGT device provides a large intrinsic jitter tolerance, suggesting that the Virtex-II Pro is a good solution for LHC.

V. REFERENCES

[1] Rocket I/O Transceiver User Guide, UG024, v2.1, June 2003, XILINX

[2] GOL Reference Manual, v1.2, May 2002, CERN Microelectronics Group

[3] QPLL User Manual, v0.2, April 2003, CERN Microelectronics Group. See also Paulo Moreira's contribution in this conference.

[4] Embedding deserialisation of LHC experimental data inside Field Programmable Gate Array (LHC-G-014 / 8th Workshop on Electronics for LHC Experiments – Colmar September 2002)