Prototype of the Muon Sorter Board for the CSC Track Finder at CMS

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Abstract

The Cathode Strip Chamber (CSC) detector [1] at the CMS experiment at CERN consists of trapezoidal 6-layer chambers located in the endcap regions of the CMS. Ultimately, the CSC system is needed for precise muon identification (position and timing) and generation of trigger primitives for the Level-1 trigger system. Up to three trigger primitives can be send from each CSC sector (comprising 8 or 9 chambers) to the Track Finder (TF) crate located in the underground counting room. The second generation of the TF has twelve Sector Processors (SP) [2] and can accept up to 180 trigger patterns (called "muons" later in this paper) every 25 ns from the CSC peripheral electronics. The SP computes the transverse momentum, pseudo-rapidity and azimuthal angle of each muon and sends its data (up to three muons each) to the CSC Muon Sorter (MS) that resides in the middle of the TF crate. The MS selects the four best candidates out of 36 possible and transmits them in ranked order to the Global Muon Trigger (GMT) for further processing.

Our initial approach to MS design and results of simulation were presented at the 6th and 7th Workshops on Electronics for LHC Experiments [3-4]. The design is based on a single programmable logic device that provides all the necessary board functions. Some improvements were made in the past two years. Particularly, we decided to switch from an Altera PLD to Xilinx FPGA and use a common with the SP mezzanine card that carries the Virtex-2 FPGA and associated EPROM's. Hopefully, both the SP and MS designs require about the same number of input/output pins and internal resources for the main mezzanine-based FPGA. Due to optimization of the sorter logic, advances in FPGA technology and design software (Xilinx ISE 5.1) we were able to reduce the latency of sorting comparing to our previous estimate. The results of the FPGA design, board prototyping and initial tests are presented below.

I. Overview of the Track Finder Hardware

The CSC Track Finder is being built in a single customized Wiener 6023 9U crate [5] that comprises the J1 part of the 21-slot VME64x backplane and custom 21-slot 6U backplane for all required communication between TF modules. Slot 1 is reserved for the VME controller that performs the control and monitoring functions. All the TF boards are VME A24D16 slaves capable to recognize the geographical address pins according to VME64x standard. We are using the SBS model 620 [6] PCI-VME bus adapter to test our prototypes. The MS is located on slot 14, next to Clock and Control Board (CCB) [7] that is an interface to LHC Trigger, Timing and Control System [8]. There are six SP modules on the left of the MS and CCB and six on the right. In addition, for testing purposes, there are slots for three Muon Port Cards (MPC) [4] and one Detector Dependent Unit (DDU) [9]. These MPC boards may produce test patterns representing data from up to three CSC sectors. One DDU board may be used for testing of the optical link to Data Acquisition System. The SP, custom backplane and a mezzanine card with the Virtex-2 FPGA are designed and built by the collaboration of the University of Florida (Gainesville, FL, USA) and Petersburg Nuclear Physics Institute (Gatchina, Russia). The DDU board is built at the Ohio State University (Columbus, OH, USA).

II. Muon Sorter Functionality

The MS block diagram is shown on Figure 1. It consists of the processing logic (mezzanine FPGA) and interfaces to CCB, SP, VME, and GMT. The most recent version of the MS specification can be found in [10]. All the main functions are performed by the Xilinx XC2V4000-5FG1152C FPGA residing on a mezzanine card. The FPGA performs sorting "4 patterns out of 36" and further LUT conversion in accordance with the GMT proposal [11].

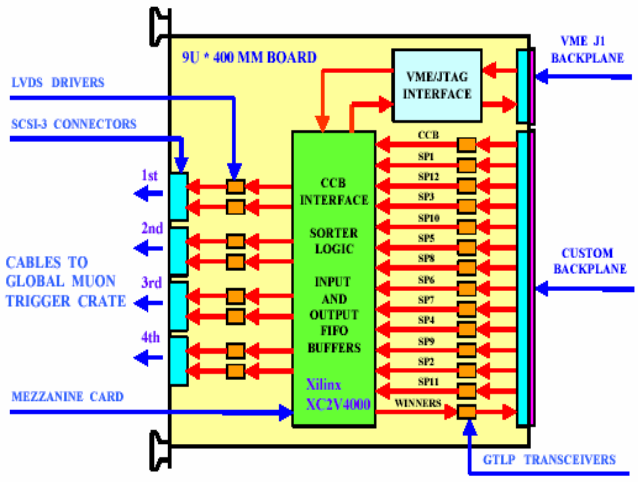

Figure 1: Muon Sorter Block Diagram

A. Interface to CCB and VME

The main 40.08MHz clock is distributed from the CCB over custom backplane using LVDS lines individually to every slot in the TF crate. All the rest signals are transmitted using GTLP logic with "negative" active levels. The MS decodes the TTC broadcast commands from the ccb_cmd[5..0] and ccb_cmb_strobe lines. A full list of these signals can be found in the specification [10].

The MS recognizes the logical A24 and geographical addresses. Geographical mode utilizes the geographical pins GA[4..0] available on VME64x backplane. In this mode the MS decodes its addresses when the code on A[23..19] lines is equal to 5-bit geographical address of its slot.

There are two methods of accessing the FPGA and its EPROM's residing on a mezzanine card. One option is based on Xilinx Parallel Cable IV [12]. Another option is to load/configure programmable devices using Fairchild SCANPSC100F boundary scan controller [13] under VME control. A small Xilinx XCR3128 PLD is being used to implement the VME access to Fairchild JTAG controller. This PLD can be programmed over separate connector using Xilinx Parallel Cable IV. The same approach is being used for the FPGA/EPROM access on an SP boards.

B. Interface to Sector Processors

Each SP may send to MS up to three muons every 25 ns. The list of signals is given in a Table 1. 64 bits of data corresponding to three muons are sent in two frames at 80 MHz, so the total number of physical backplane lines between MS and each SP is limited to 32.

Table 1: Sector Processor to Muon Sorter Interface

Inputs from each Sector Processor		
Signal	Bits per one muon	Bits per three muons
Eta Coordinate	5	15
Phi Coordinate	5	15
Rank	7	21
C (Charge, or Sign)	1	3
VC (Valid Charge)	1	3
Bunch Crossing ID	-	1
HL (Halo Muon Trigger)	1	3
BC0 (Bunch Crossing Zero)	-	1
SE (Synchronization Error)	-	1
SP (Spare Bit)	-	1
Total	20	64
Outputs to Sector Processor		
Winner Bits	-	2

If a particular muon from the SP has been accepted by the MS after sorting, then a "winner" bit is sent from the MS back to corresponding SP. The total number of feedback "winner" lines is 24, or two lines per each SP. The "winner" bits are sent in two 80MHz frames. Each SP may insert its "winner" bits into data stream to DDU for further monitoring. The Texas Instruments SN74GTLPH16912 transceivers are used for communication between the MS and SP. All lines are terminated on the receiver ends (56 Ohm to 1.5V). Having 408 lines between MS and 12 SP, we were able to use four industry standard 5-row 125-pin metric connectors on MS station for all required communications between MS, CCB and 12 SP's and fit the MS into a single VME slot.

C. Sorting Logic

The MS sorter accepts 36 7-bit patterns called Rank[6..0] that represent the "quality" of each muon (the larger the rank, the better the muon for sorting purposes). The sorter outputs four 36-bit binary addresses of the first, second, third and fourth largest patterns. These 144 bits are used for pattern merging onto the sorter outputs. If several selected patterns appear to have the same rank, then the pattern from the source with a largest physical address in the crate will be chosen as a 1st best, the pattern from the source with the second largest physical address will be chosen as a 2nd best and so on. It is assumed that if there are no valid muons selected by the SP, then each SP sends the Rank[6..0]=0.

Four groups of FIFO buffers (FIFO_A, FIFO_B, FIFO_C, and FIFO_D) are implemented in the main FPGA in order to test the MS internal functionality and its communications with the SP and GMT. All buffers are 511-bit deep and available from VME for read and write. FIFO_A may be used to simulate the SP inputs. FIFO_C buffers keep a copy of four selected muons immediately after sorting. FIFO_B buffers keep the copy of four selected muons after LUT conversion. FIFO_D buffer is described below in section D.

D. Interface to Global Muon Trigger

An interface to GMT is based on proposal [11]. The signals are listed in Table 2. All signals representing one muon are transmitted over twisted pair cable in LVDS logic levels. Four 68-pin SCSI-3 connectors are placed on the front panel of the MS. All four selected muons are transmitted in ranked order, with connector 1 assigned for the 1st best muon, connector 2 for the 2nd best muon and so on. The Texas Instruments 16-bit SN75LVDS387/LVDT386 chipset is being used. The MS has also one receiving connector for testing purposes. In the absence of the GMT receiver, the LVDS cable can be looped back into this connector and the data that was sent to GMT can be read back from FIFO_D buffer over VME.

Table 2: Muon Sorter Outputs to Global Muon Trigger

Signal	Bits per one muon	Bits per four muons
Eta Coordinate	6	24
Phi Coordinate	8	32
Quality + Pt Momentum	3+5	32
C (Charge, or Sign)	1	4
VC (Valid Charge)	1	4
Bunch Crossing ID	3	12
HL (Halo Muon Trigger)	1	4
BC0 (Bunch Crossing Zero)	1	4
SE (Synchronization Error)	1	4
40.08 MHz clock	1	4
Total	31	124

Look-up Table RAM's are embedded into an FPGA and provide data conversion into format acceptable for the GMT. 7-bit Rank is converted into 3-bit Quality and 5-bit Pt. 5-bit Phi and 5-bit Eta coordinates of each selected muon are converted into 6-bit Phi and 6-bit Eta patterns that take into account a respective endcap region.

III. Results of Prototyping and Initial Tests

Four MS boards were built and assembled and one of them was extensively tested in spring and summer of 2003. A picture of the MS board is shown on Figure 2. Software for testing of the sorter logic was developed. The data patterns corresponding to SP data can be loaded into FIFO_A[12..1], sent out at 80MHz through the sorter and results can be checked from FIFO_B[4..1] and FIFO_C[4..1]. Connection to GMT receiver board (that was not available yet) was tested using loop-back option and FIFO_D buffer. The MS, CCB and SBS 620 controller under tests in a 9U VME crate are shown on Figure 3. Based on results of simulation, the total latency of the FPGA logic is estimated to be 125 ns, or five bunch crossings of LHC frequency.

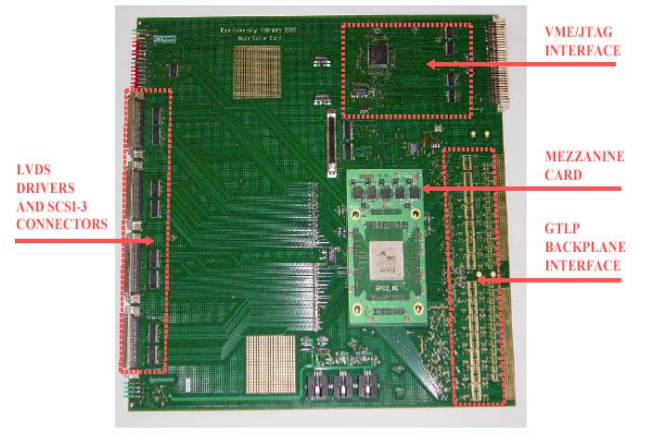

Figure 2: Muon Sorter Board

With the SCANPSC100F controller running at 10 MHz, we were able to program four XC18V04 EPROM's over VME for ~1 min, or four times faster than through the Xilinx Parallel Cable IV.

Figure 3: Track Finder crate under tests at Rice University

IV. Conclusion

We have built a prototype of the Muon Sorter board for the endcap CSC system at CMS. The board receives up to 36 muon patterns from 12 Sector Processors, selects four best ones and transmits them in ranked order to the Global Muon Trigger of the CMS experiment. Initial tests of the sorting logic were done and more integration tests with the Sector Processors and GMT are planned in 2003-2004.

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