A Multi-Level Boundary Scan Environment Used in the CMS ECAL Data Acquisition and Trigger System

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Abstract

This paper describes the implementation of boundary scan test (BST) architecture [1] and the corresponding software tools designed to manage the test application.

Tests performed in a prototype of the boundary scan system, to be included in the data acquisition and trigger system of the CMS electromagnetic calorimeter, being built at CERN, show that the same test/programming vectors used at board level can be re-used for system test or for reprogramming electronic devices during system operation. A final version of this BST system is being prototyped for the ECAL VME64x crates and will enable the application of BST and programming operations within the crate [2].

I. INTRODUCTION

A system architecture based in a backplane boundary scan bus is described in this contribution [3]. The system has connected several boards under test. The interface between the backplane bus and the local scan chains, located in each board under test is performed by a Scan Bridge device [4, 5]. The control of the backplane bus is done by a FPGA (Field Programmable Gate Array) that manages the application of the test and programming vectors.

A dedicated software tool – *Boundary Scan Connect* - translates the vectors generated to test each board, using the Serial Vector Format (SVF) [6], into a new set of vectors oriented to the system architecture. A straightforward modification, in the SVF data and instruction scan commands, is sufficient to re-apply the same test/programming vectors to the new system layout.

II. HARDWARE ARCHITECTURE

The system considered here is based in a VME64x Backplane Bus, an extension of the ANSI/VITA 1-1994 VME64 Standard [7], frequently used in academic and physics applications. The system boards are organized in card racks sharing a common backplane bus. A typical VME architecture includes the system boards, or slave boards and a master board managing the data transfers in the bus.

To perform the testing and the programming operations in the system, it was added some components, which are shown in figure 1:

- At Board Level: a *Scan Bridge* device is used to connect to the test bus. This device is operated using 1149.1 protocol, which is supported by available software (JTAG Technologies).
- At Crate Level: the *MTM bus* lines of the VME64x backplane are usedas standard 1149.1 boundary scan lines.
- A dedicated hardware controller is responsible for application of the test/programming vectors to the crate - *Boundary Scan Controller*.
- A software tool - *Boundary Scan Connect* - is used to translate the boundary scan test and programming vectors generated by commercial software.

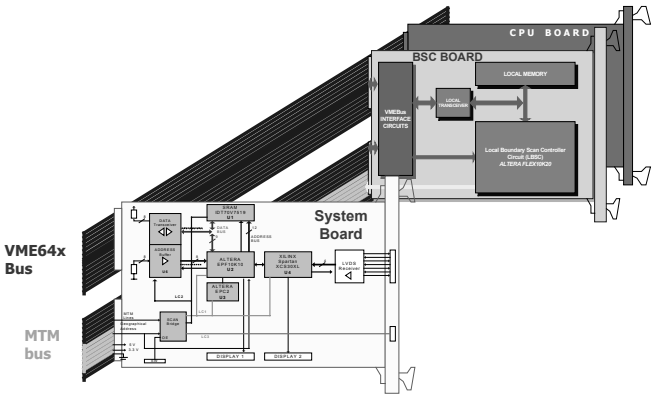

Figure 1: Hardware architecture

The VME64x bus specification dedicates a group of five lines, to accommodate the Module Test and Maintenance (MTM) bus, originally designed to support the IEEE Std 1149.5-1995 protocol. However, due to almost inexistent support of MTM at hardware and software level, the decision of using these lines as a 1149.1 backplane test bus was set.

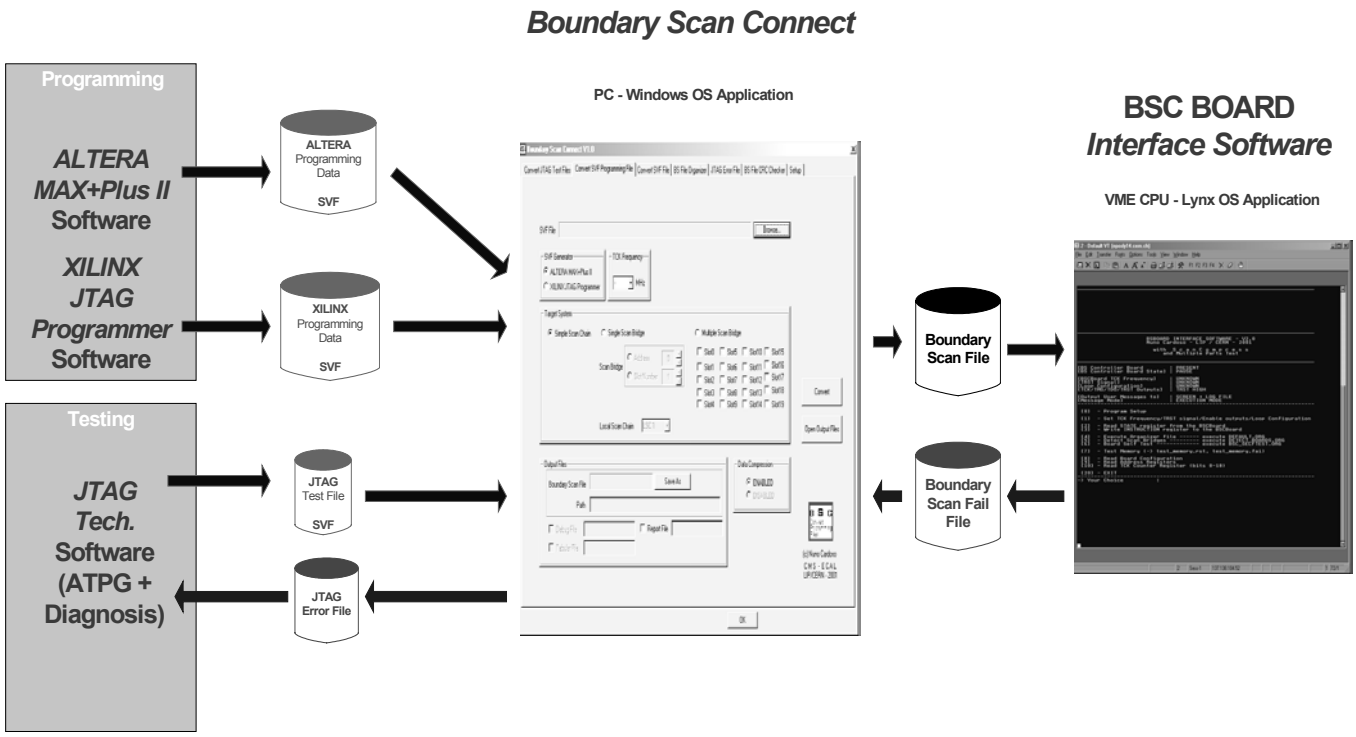

Figure 2: Software architecture

III. SOFTWARE ARCHITECTURE

The *Boundary Scan Connect* software takes the test/programming vectors generated by an ATPG or by a PLD/FPGA development station - figure 2. Most of these tools generate proprietary formats to describe their vectors. However, the Serial Vector Format (SVF) is, in some extent, supported by the majority of these tools. SVF employs ASCII characters to specify the input and response vectors and the mask patterns to be applied in each set of vectors. The SVF test/programming files contain scan data commands and scan instruction commands to load data into the target data register(s) and target instruction register(s) respectively.

A. JTAG Tech. Boundary Scan Tools

The software tools provided by JTAG Technologies include a Test Development Package. This package possesses an Automatic Test Pattern Generator (VIP Manager) for testing the BS infrastructure and the board interconnections. The generator tool takes the board netlist and the BSDL files to generate the test programs (.GEN and .APL files). Hierarchical structure in .CON file describes the local chain connections to the scan bridge. Tools for diagnosing the infrastructure and interconnection faults (shorts, stuck-at faults) are also available

B. Conversion of JTAG Tech. Test Files

The developed software allows the translation of the JTAG Tech. test files (interconnection and infrastructure) into a single boundary scan file containing all the information to apply the test and evaluate the results - figure 3. A temporary diagnosis file is created for later evaluation of test results.

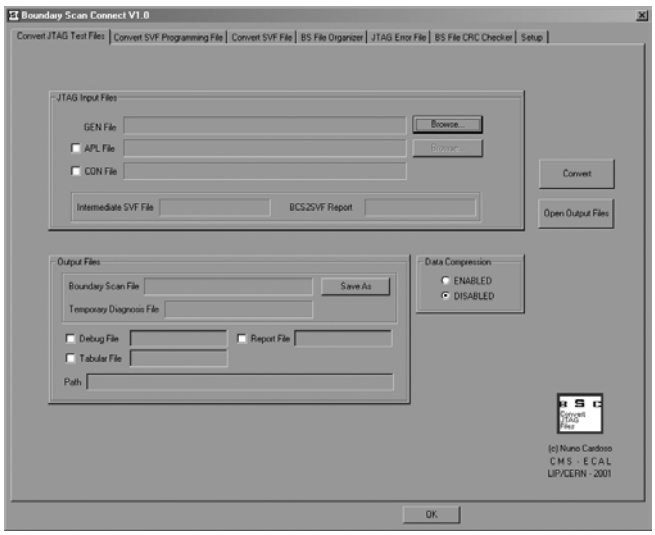

Figure 3: Conversion of JTAG Tech. test files.

A JTAG Error File allows the visual presentation of the test results and the diagnosis of the errors by the JTAG Tech. Software, figure 4.

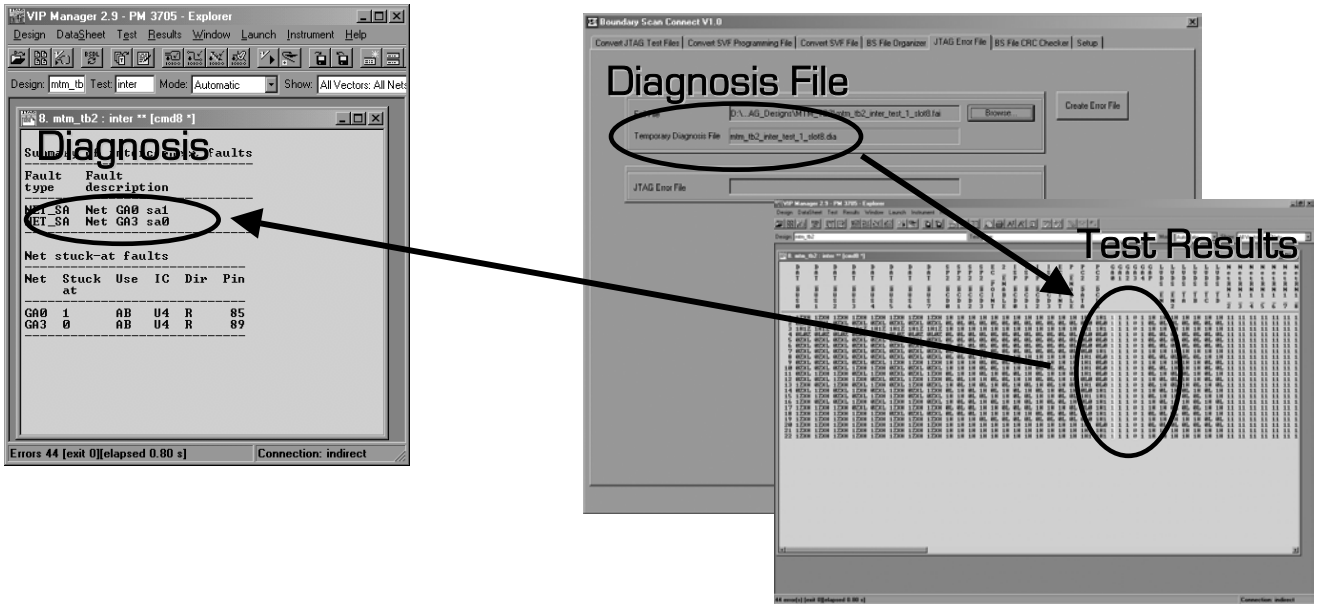

Figure 4: Test results and diagnosis.

C. *Generation of Programming Files*

When the system is used for in-circuit programming of re-configurable devices like FPGAs and Programmable Logic Devices (PLDs), the SVF file contains the scan operations to load the programming instructions into the device through their boundary scan interface port. The SVF file generated by these tools includes information specific to the board scan chain characteristics, i.e., the device organization and the dimension of the Instruction Registers and Boundary Scan Registers, but usually, it does not provide a mean to include an interface device in the scan chain – figure 5.

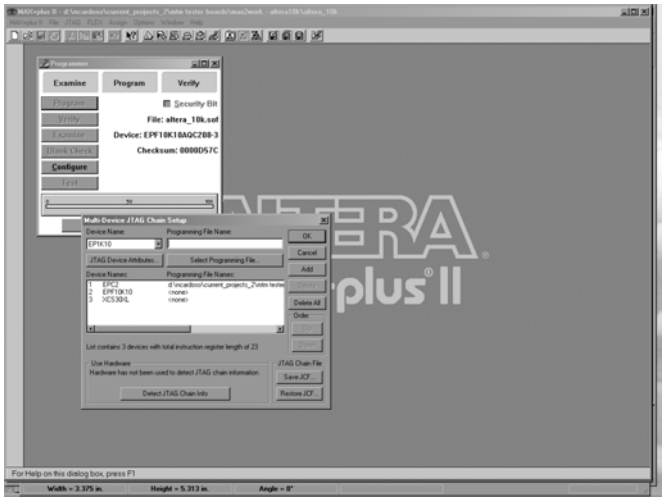

Figure 5: Generation of programming files (ALTERA).

The *Boundary Scan Connect* software processes the SVF commands and introduces the additional bit patterns to include the Scan Bridge registers and pad bits - figure 6.

The processing is performed in two steps:

- Modification of the SVF Data Scan commands. The data scan commands are modified accordingly with the local scan port configuration. The bit patterns corresponding to the Scan Bridge data registers and additional pad bits are inserted into the data scan chain.
- Modification of the SVF Instruction Scan commands. The instruction scans are modified in order to include the Scan Bridge instruction register, the board instruction scan chain and the pad bit.

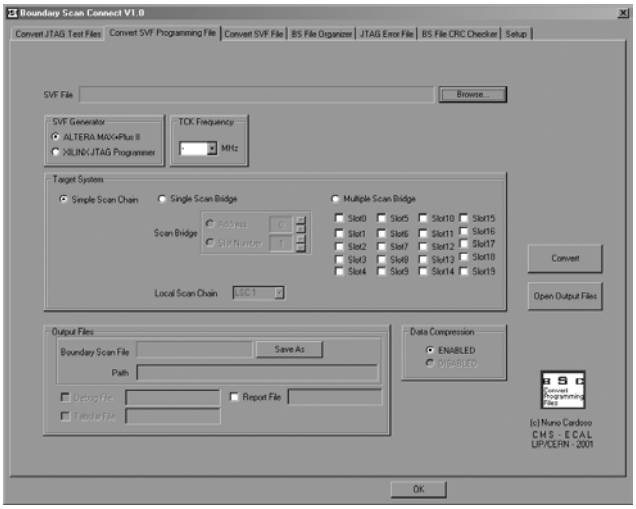

Figure 6: Conversion of programming files.

IV. VALIDATION OF THE ARCHITECTURE

Two demonstration boards, MTM-TB1 and MTM-TB2, with the boundary scan architecture presented in this paper were designed and manufactured. Each board contains 2 local

scan chains connected to a Scan Bridge. Typical boundary scan circuits like FPGAs, PLDs, memories and transceivers, were included in the design. A switch in the demonstration boards provided direct access to the local chains, bypassing the Scan Bridge, before inserting the boards in the VME64x system. A disable control signal in the Scan Bridge allows the control of the local scan chains by the test/programming controller – figure 7.

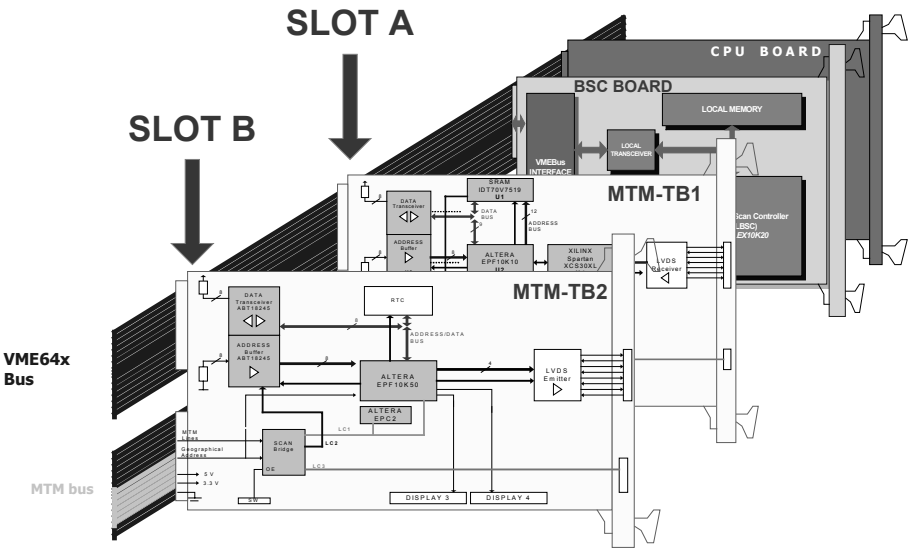

Figure 7: Validation of the test architecture.

V. RESULTS

For testing and programming the demonstration boards, it was used commercial tools available and Personal Computer (PC) based controllers provided by JTAG Technologies. In a later phase the *Boundary Scan Connect* software was used to translate the boundary scan SVF test and programming files, in order to include the information for selecting the Scan Bridge address and the active local scan ports. A general test/programming file, in a proprietary format, containing both, the test and the programming vectors, was applied through an embedded Boundary Scan Controller, implemented in a FPGA, via the 1149.1 backplane bus. The results obtained verified the correct operation of the system and, in particular, of the translation software.

The translation software is limited to the selection of a single Scan Bridge in the backplane bus. This limitation does not permit to test the backplane interconnection and the inter-board testing which require the simultaneous selection of multiple scan bridges. Therefore, testing performed outside the board boundaries cannot be done at the moment. However, this possibility is foreseen by the Scan Bridge architecture, which allows multiple broadcast addresses. Interconnect and inter-board testing would require a further description of the connections and the generation of additional test vectors.

VI. REFERENCES

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