CMOS Monolithic Active Pixel Sensors (MAPS) for scientific applications

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Abstract

CMOS Monolithic Active Pixel Sensors (MAPS) were invented or possibly re-invented in the early '90s. Their great potential as imaging devices was immediately recognised and since then the number of applications has been steadily growing. At the end of the same decade, MAPS were also proposed and demonstrated as detectors for particle physics experiments.

This talk will review the state-of-art of MAPS as imaging sensors, both for the consumer market and for scientific applications. Emphasis will be given to those aspects, e.g. radiation damage, charge collection efficiency, …, of particular interest for the particle physics community. The talk will conclude on the perspective of MAPS for future scientific instruments.

I. INTRODUCTION

Silicon devices have been used since the 60s for the detection of radiation [1]. The interest of MOS devices was immediately recognised and arrays were designed. However, when Charge-Coupled Devices were invented at Bell Laboratory in 1970 [2], they immediately became the main imaging devices, both in the consumer and in the scientific imaging market. About 10 years after their invention, CCDs were proposed as sensors for a vertex detector [3]. In the meanwhile, MOS and CMOS sensors were still being developed, mainly as focal plane infrared sensors [4, 5, 6, 7].

Towards the end of the '80s, helped by the reduction of CMOS transistors, Passive Pixel Sensors (PPS) were actively developed. In PPS, each pixel features one photodiode and one transistor for the selection of the pixel. The radiation-generated charge is dumped through the selection switch into the readout lines and read by a charge amplifier. PPS have good fill factor because but were still suffering from relatively low noise and speed.

The big push for the development of CMOS sensors came from the introduction of Active Pixel Sensors (APS) in the early '90s [8, 9, 10]. It was immediately recognised that CMOS APS, or Monolithic Active Pixel Sensors, MAPS [1], have several advantages.

- MAPS are made in CMOS technology, and can then take advantage of the world-wide developments in this field, in particular for the reduction of minimum feature size (MFS).
- Being monolithic, MAPS avoid the problems related to bump-bonding or other types of connections.
- Because of the shrinking size of transistor, pixels can be made very small or more functionality can be integrated in the same pixels [12 13, 14].
- MAPS can have a very low power consumption [15].
- Deep submicron CMOS is radiation resistant.
- Several functionalities can be integrated on the same chip together with the sensor arrays. This brings simplification at the system level and hence reduction of costs.Pixels can be accessed randomly, trading off resolution or array size with readout speed or making possible to track objects at very high speed [16].
- The readout and analogue-to-digital conversion is always massively parallel, being normally column-parallel, but in some cases even pixel-parallel [12 13, 14].
- They can be made very easy to use, limiting the readout system requirements to digital I/Os.

II. CMOS SENSORS IN INDUSTRIAL APPLICATIONS

In sensors developed for commercial applications, we can distinguish two phases of operation: i) integration or exposure ii) and readout (fig .1).

The integration can normally performed in two ways, either in *rolling shutter* mode or in *snapshot* mode. The former is the most common. All the pixels in a row are reset and start the integration at the same time. Pixels in different rows integrate for the same duration of time but not exactly at the same time. In the snapshot mode, all the pixels integrate during the same period of time. The snapshot way is closer to the way one would normally operate a sensor but normally requires more than 3 transistors to operate correctly [17]. The readout is always done row by row.

[1] The terms MAPS is used to distinguish CMOS APS from hybrid detectors (also called Hybrid Active Pixel Sensors or HAPS) in which the sensor and the readout electronics are on two different substrates, normally connected by bump-bonding. HAPS were proposed for high-energy physics [11] and they are also of interest in Infra-Red focal plane.

Most of the sensors used for commercial applications have either 3 or 4 transistors. Also, all the pixels in a column share a common output bus. This architecture is fast because is column-parallel, but an even higher increase in speed could be achieved by having all the pixels operating independently in the same time. Pixel-parallel sensors were proposed and developed by the Stanford University. In this case, the analogue-to-digital conversion is done inside the pixels. Several architectures for the data conversion were proposed [12, 13], with the most recent one being an in-pixel single ramp [14]. These pixel-parallel sensors achieve higher speed than conventional, column-parallel sensors, achieving rates o 10,000 frame/sec. The conversion tends however to be limited to 8 bit. The number of transistors in the pixel also tend to be higher thus limiting the fill factor (see the following section).

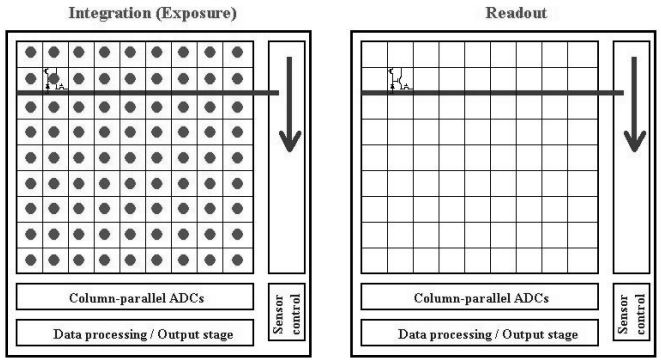

Figure 1. A commercial sensor normally operates in two sequential phase, the integration (on the left) and then the readout. While the integration can be done either in the rolling shutter mode (row by row) or in the snapshot mode (all pixels at the same time, the readout is always done row by row.

III. SENSORS IN CMOS

A schematic cross-section of a CMOS circuit fabricated in a twin-well technology is given in figure 2. Since every junction, either metallurgical or field-induced, can potentially be used for radiation detection, there are several ways to create a detector in a CMOS circuit. As indicated in figure 2, junction can be created directly in the wells or also between the wells and the substrate. This latter tends to be P-type and often manufactured as a thin epitaxial layer on a thick substrate, also of P type, and whose presence is to guarantee mechanical stability during wafer handling. The thick substrate tends to be heavily doped, while the epitaxial layer is less doped, with a resistivity of the order of 1 – 10 Ohm cm.

For visible light, or generally photon, detection, it is important to consider the absorption length of the radiation, which is a function of the wavelength. The energy gap for silicon being 1.1 eV, this translates into a cut-off wavelength of 1.1 μm, i.e. in the near infra-red. The absorption length is very long at this wavelength and tends to decrease with increasing wavelength, up to the UV band. In the visible region of the spectrum, the absorption length spans from a few microns at the red end down to fraction of a micron in the blue area. This is a rather fortunate coincidence, since it matches well with the thickness of substrates used in the microelectronic industry. Given the dependence of the absorption length from the wavelength, it becomes that shallow junctions, like the P+/N-well or the N+/P-well, tends to be more effective in the blue than in the green or the red, while deeper junctions, like the N-well/P-epi tends to be more effective for these colours. It has to be stressed that efficient green detection is particularly important for colour cameras, since the green is the wavelength to which the eye is more sensible. This is also the reason why the most common colour filtering pattern is the Bayer RGB pattern, which features two green and one red and one blue pixel every set of four.

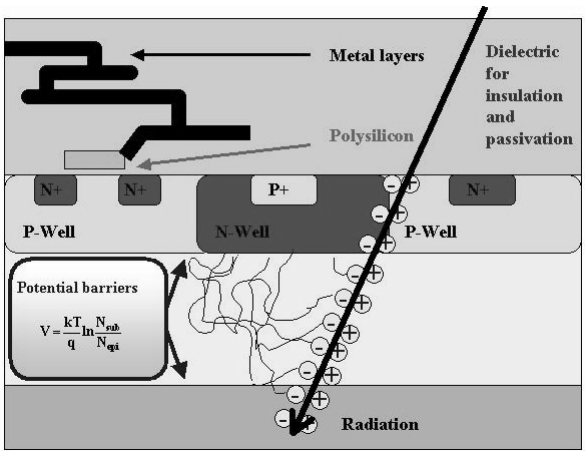

Figure 2. Schematic view of the cross-section of a CMOS process.

The N-well/P-epi junction has also another important characteristics, which is also illustrated in figure 2. The doping of this layer is lower than that of the P-wells above and of the P substrate below. At the boundary of the P epitaxial layer, there exists then a potential barrier whose height is

$$\frac{kT}{q}\ln\frac{N_P}{N_{epi}}$$

where N_P is the doping of either the P-wells or the P-substrate and N_{epi} is the doping of the epitaxial layer. The other quantities k, T and q have the usual meaning of the Boltzmann's constant, the absolute temperature and the charge of the electron respectively.

Electrons induced by the radiation in the P epitaxial layer are minority carriers in this free-field region. The potential barriers at the boundaries keep the electrons inside this region. When they approach the depletion area around the N-well, they experience a field that will attract them to the anode where they are finally collected. This means that the entire epitaxial layer can be used as a sensitive layer for radiation.

The use of the potential barriers generated by the doping layers to confine electrons in the epitaxial layer was well known to the CCD community (see for example [18]). In the CMOS field, it was first proposed for the detection of light [10] and successively proposed for the detection of charged particles [19]. For the detection of visible light, the detection

efficiency will still be limited by the material existing on top of the silicon surface, i.e. insulating dielectrics and metals for interconnect. While dielectric material can be fairly transparent, metals are opaque and constitute the main limitation to the detection efficiency. This is not the case for high-energy charged particles, since the metal layers are only a few micron thick. In this case, the N-well/p-epi diode achieve effectively 100% detection efficiency as demonstrated in [20, 21, 22].

IV. CMOS TECHNOLOGY FOR SENSORS

So far, the big push to the development of CMOS sensors has come from industrial applications. This has also brought improvements in the technology since foundries have recognised the commercial interest. Today, aside the traditional 'flavours' of logic and mixed-mode, or analogue RF, many foundries propose a new flavour, named CMOS Image Sensors or CIS [23, 24, 25, 26]. In these CIS processes, modules are added to improve the quality of the images. In these developments the main guidelines are:

- reduction of the average leakage current
- reduction of 'white spots', i.e. of pixels with very high leakage current
- increasing the dynamic range
- improving the quantum efficiency.

For an example of how the first two points are tackled by industry see for example [27]. For the third one, foundries tend to exploit the already existing feature of having multiple power supplies, for example 2.5 and 3.3 V in a 0.25 µm process, and multiple Vt transistors.

The last point deserves a few more lines since it is of particular interest for the detection of charged particles. As mentioned in the previous paragraph, for good quantum efficiency in the green-red area of the spectrum, the sensitive volume has to be at least a few microns thick. Most of the foundries involved in the development of CIS processes adopt an epitaxial layer with a few micron thickness because of these. This choice of substrate is particularly interesting in view of the move of many microelectronics foundries towards SOI substrate, where the silicon layer would be too thin to be used as a useful substrate for detection. It should however be mentioned that SOI substrates have also received some interest for the detection of radiation [28]. In this case, the 'handle wafer' is used as a sensitive layer. This has not yet entered the production lines of main manufacturers, but it is very interesting in view of the fact that 'handle wafer' can be made much thicker and with higher resistivity than epitaxial layers, normally limited to 20 µm and about 100 Ohm cm respectively.

V. CMOS SENSORS FOR SCIENCE

The first proposal to use CMOS sensors for a scientific application is probably for a vertex detector in particle physics [19]. Since then, different technologies have been tested and the results proved the original idea that 100% efficiency for charged particle detection could be achieved with the N-well/P-substrate diode. Also, the radiation resistance of the sensors have been tested up to level [22] of interest for the future Linear Collider.

In CCLRC-RAL we are now working to expand the range of applications where CMOS sensors can be used. A list of the main sensors designed so far can be found in table 1.

Sensor	Format	Pitch (µm)	Area (mm*mm)	Pixel type / CDS	MOS per pixel	Techno	Readout
512x512 camera-on-a-chip	**525x525 / 0.27M pixels**	**25**	**13*13**	**3MOS**	**3**	**0.5µm CMOS**	**10-bit column-parallel ADC**
EUVAPS	**2880x4096 / 11.8M pixels**	**5**		**4MOS**	**4**	**0.25 µm CIS**	**Analogue**
LinCS	**1x4096 / 4K pixels**	**3**	**12**	**linear**	**n.a.**	**0.25 µm CIS**	**Analogue**
RAL_HEPAPS2	**384x256 / 0.1 M pixels**	**15 (20 for FAPS)**	**7*5**	**3MOS / 4MOS / CTIA / FAPS**	**3 / 4 / 3 / 38**	**0.25 µm CIS**	**Analogue**

Table 1. List of the main CMOS sensors designed by CCLRC-RAL.

The 512x512 was designed as a technology demonstrator [29]. It is a camera-on-a-chip. At the bottom of each column (right in the figure 3), one column amplifier and a 10-bit single-ramp ADC are integrated. The readout is digital on a 11-bit wide digital bus, one overflow bit sent out in parallel with the 10 data bits. An example of snapshot with visible light is shown in figure 4. The pixel has the simple 3 MOS structure and the diode is N-well / P-epi and features a high detection efficiency. It has been tested with a number of particles, including 140 keV electrons. An example of the tests performed with electrons can be seen in figure 5. In this case a focused beam was raster scanned over the sensor, and the average number of electrons per spot was about 2. The results show the excellent performances of the sensor for the detection of low-energy charged particles.

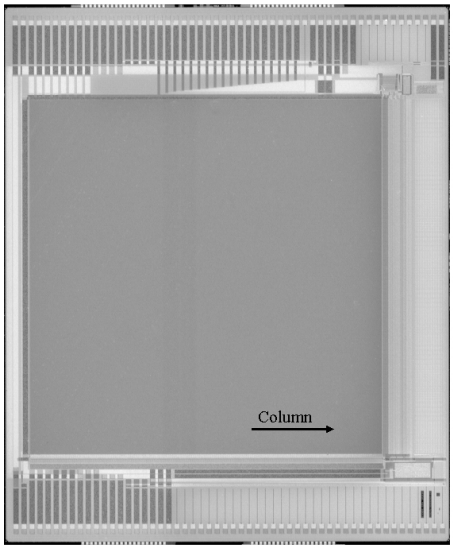

Figure 3. Photo of the 512x512 sensor. Columns are oriented horizontally in this picture. On the right, i.e. at the bottom of the columns, adjustable gain column amplifiers together with a 10-bit ADC per column.

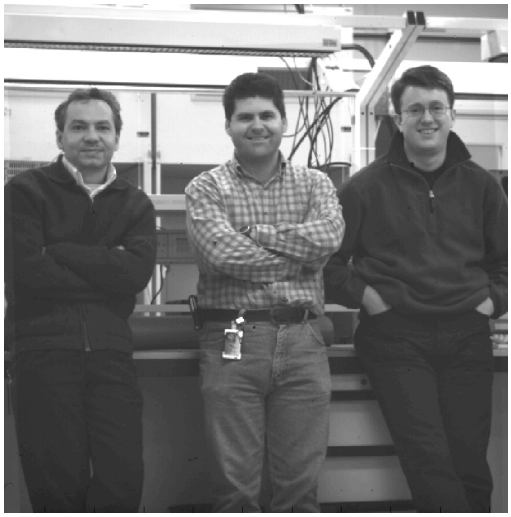

Figure 4. Snapshot taken with the 512x512 sensor.

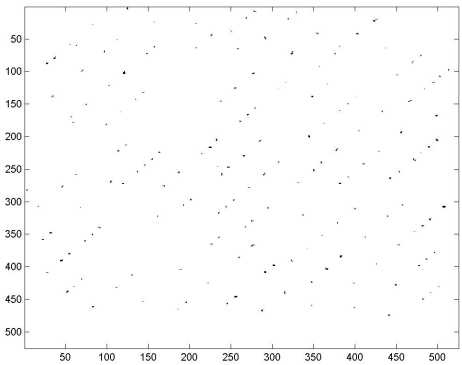

Figure 5. Raster scan with 140 keV electrons recorded with the 512x512 device. The beam was set so that each spot carried an average of 2 electrons per spot. Because of Poisson statistics, this means that some spots will have no electron. The distribution of electron per spots fits well with the expected Poisson distribution.

The other three sensors have been recently designed in a 0.25 µm CIS process. A photo of the 200 mm wafer with the three sensors is shown in figure 6. The first sensor is a 12M pixel sensor which is a prototype for 16M pixel for EUV observation of the Sun [30]. The driver application is the ESA's Solar Orbiter mission. The second one is a linear sensor, prototype of a sensor fro Earth Observation which could feature 3, 4 or even 5 arrays for colour and possibly infrared detection of the earth from Space with a very high resolution of 1 m [31].

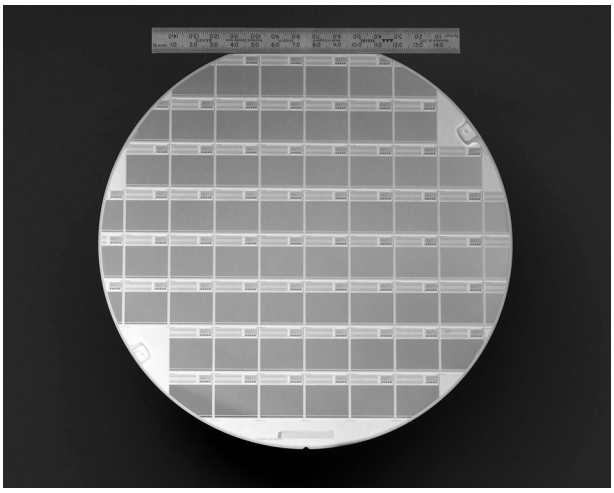

Figure 6. Photograph of the 200 mm wafer with the three sensors designed in a 0.25 µm CIS process. In each reticle, the large sensor is the 3k*4k sensor. On top of this, on the right is the linear sensor and of the left is the parametric test sensor.

The third one is a parametric sensor, i.e. a sensor where different designs are integrated in order to test different architectures. The floorplan of the sensor is shown in figure 7. Row and column decoders give random access to the single pixels. The layout is organised in 4 vertical stripes, each with a different type of design:

- 3 MOS
- 4 MOS
- Charge Preamplifier
- Flexible Active Pixel Sensor FAPS.

The last pixel is a special architecture designed with an internal analogue buffer in each pixel. The buffer consists of 10 memory cells. The pixel has also two amplifiers, one for writing and the other one for reading the cells. This pixel architecture has been chosen in view of the use of CMOS sensors for the next Future Collider. The design of the machine should allow to write data at the required speed (50 MHz for some designs) during the beam-on period and then read the sample out when the beam is off. More details about the architecture can be found in [32]. Tests are in progress at present.

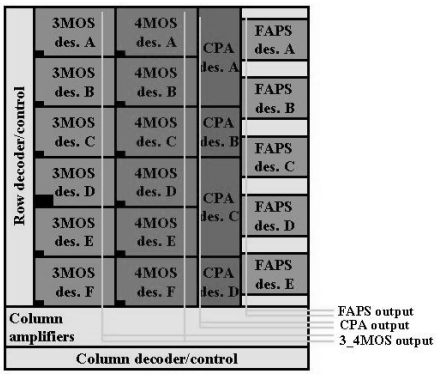

Figure 7. Floorplan of the parametric test sensor.

VI. CONCLUSIONS

In the last decade, CMOS sensors have been challenging the dominant role of Charge-Coupled Device in consumer and industrial applications. At present, CMOS sensors represent over 30% of the market and should go over 50% in a few years [33].

In scientific applications, CMOS sensors were first proposed as a vertex detector for particle physics, and because of the properties of the silicon substrate, CMOS sensors could be used for the detection of a wide spectrum of electromagnetic radiation, ranging from infrared to UV and low-energy X-rays, of charged particles, including low-energy electrons, and of neutrons [34].

For particle physics, we have also recently proposed a novel structure [35] which would allow to increase the electric field in the sensitive volume. The charge collection would then be speeded up, resulting also in an improved radiation resistance. A sensor with this type of architecture is now being currently designed and should be manufactured in the first half of next year (2004). This sensor could provide a solution to the design of CMOS Active Pixel Sensors for harsh radiation environment as the ones found in LHC.

CMOS sensors have only started to be used for scientific applications but their potential advantages over other solutions promise new exciting developments in the next years.

VII. ACKNOWLEDGEMENTS

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