A BiCMOS Synchronous Pulse Discriminator for the LHCb Calorimeter System.

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Abstract

A monolithic prototype for the analogue readout of the Scintillator Pad Detector (SPD) of the LHCb Calorimeter is presented. A low power version that works at 3.3 V has been designed using the 0.8 µm BiCMOS technology of AMS. It consists on a charge discriminator with a dual path structure formed by an integrator, a pile-up correction, a subtractor and a comparator. The chip also includes a DAC and serial digital control interface to program the threshold of the discriminator. Design, simulation and test results for different prototypes of the circuit will be presented and described.

I. INTRODUCTION.

The LHCb calorimetry [1] has four elements: a hadronic calorimeter (HCAL), an electromagnetic calorimeter (ECAL), a Preshower detector (PS) and a Scintillator Pad Detector (SPD). The system provides high energy hadrons, electron and photons candidates for the first level trigger.

The SPD is designed to distinguish electrons and photons for the LHCb first level trigger. This detector is a plastic scintillator layer, divided in about 6000 cells of different size in order to obtain better granularity near the beam [2]. Charged particles will produce, and photons will not, ionisation on the scintillator. This ionisation generates a light pulse that is collected by a WaveLength Shifting (WLS) fibre that is twisted inside the scintillator cell. The light is transmitted through a clear fibre to the readout system.

A block diagram is shown in figure 1. The signal of the scintillator pads is processed in a Very Front End (VFE) unit, which includes a photomultiplier (PMT) to convert the light pulse inro charge, the electronics to perform the discrimination between electron and photon signals, a bunch crossing clock receiver, a control unit and a LVDS serialiser to send the information to the PS Front End cards. For economical reasons a multianode (MA) PMT is chosen as photodetector, being the Hamamatsu R7600-M64 the baseline solution. Each VFE unit is implemented through a board containing 1 PMT. Therefore it will contain 64 discriminator channels. It is decided to install the analogue processing unit in the PMT base board to improve the SNR and to be able to simplify the interconnections and the PS FE boards by transmitting digital multiplexed information. The VFE boards will be located on top and bottom parts of the Scintillator layer, that means that a small space will be available to install

each unit and that power dissipation of the system must be considered (must be below 10W per board) Due to the high number of components and the complexity of the circuits the supply voltage is fixed to 3.3 V to fulfil this requirement.
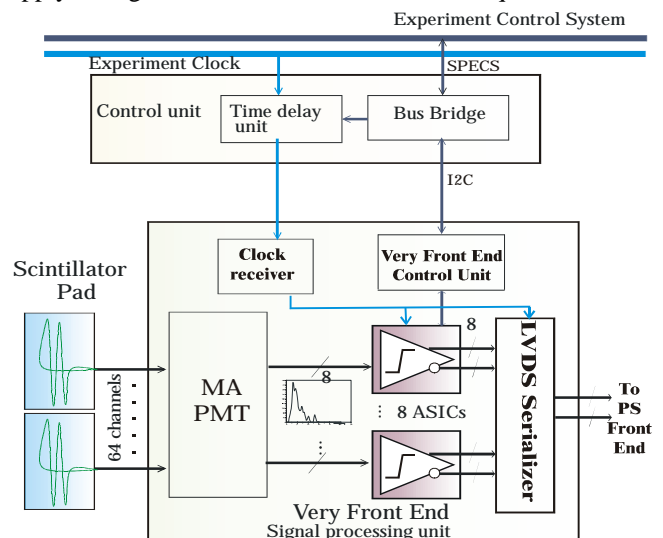

Figure 1: SPD readout system.

In order to optimise the space and power consumption the discriminator is implemented through ASIC, having 8 channels in its final version. The AMS 0.8µm BiCMOS technology is chosen because bipolar transistors will be needed for the analogue parts, specially to reduce offsets, and because MOS transistors will be used as switch elements and to reduce the power consumption in the digital parts. The analogue front end electronics of other elements of the LHCb calorimeter is also implemented in this technology.

II. REQUIREMENTS.

The SPD has to perform separation between photons and the charged particles. Ideally only charged particles would generate a signal (MIP signal). However, high energy photons can create an electron through secondary processes such as Compton effect or pair production. This phenomena produces an energy spectra with a maximum at 0 but with a small tail for high energies provoking that some photons are identified as electrons [3]. Applying a threshold at 1.4 MeV (≈0.7 MIP) is a good compromise to reject the photons with no too bad efficiency for the trigger. The resolution of the discriminator must be better than 0.05 MIP in order keep the energy resolution given by photostatistics in this threshold area. The

maximum average current that can be used to avoid a fast aging limits the gain of the PMT. For the cells with higher occupancy the MIP signal will be limited to 100fC.

The signal outing the SPD PMTs is rather unpredictable because of the low number of photostatistics, 20-30 photoelectrons per MIP, and the due to the response of the WLS fibre, which has a decay time of around 10 ns. This "slow" decay time means also that the signal spreads over more than clock period. According to present data about the 80% of the signal is in the first period. This fact causes another bothering trouble: the potential tail of a high amplitude event could cross the threshold and provoke a fake trigger. Thus, pile-up correction is needed. A range of at least 5 MIP is required to be able to perform this compensation.

Although the fibre response creates a pole at ≈30MHz, events with single photoelectron components can be observed due to the low photostatistics Thus the bandwidth of the system must be higher than the PMT one (about 100MHz). Temperature drifts must be take into account. A band gap current source is the base reference for all the blocks, to have good temperature stability. The linearity error must be smaller than 5%.

III.   SYSTEM ARCHITECTURE.

Figure 2 shows the functional architecture of each discriminator channel. The configuration is based on two interleaved processing units per channel to avoid any dead time and to be able to perform the pile-up compensation. This solution does not require external components such delay lines, which is important for room reasons. The bunch-crossing clock is divided and then used to multiplex by level the two paths of the channel each 25 ns. To prevent digital crosstalks on sensitive analogue parts, the latter are fully differential. This architecture is also implemented for the PS chip [4].
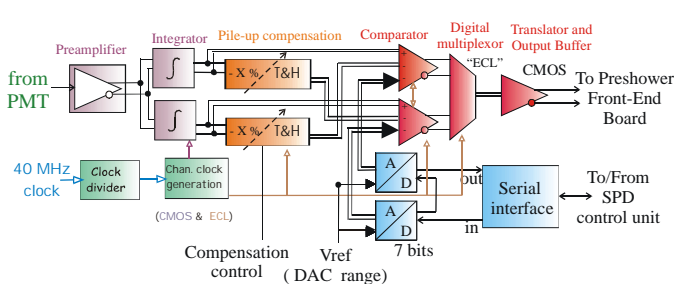

Figure 2: Functional diagram of a discriminator channel.

The PMT signal is single ended, it is preamplified and converted to differential by the first block of the discriminator. As explained in the previous section the signal is rather unpredictable and spreads over more than one clock period of 25 ns, thus, the only way to measure the energy deposition is to integrate. While one integrator is reset the other performs the integration and its output is continuously corrected and compared with a programmed threshold. The comparison is latched just before the end of the integration period. The pile-up compensation system takes a fraction of

the integrator output at this time (ideally the fraction that would appear in the next period) and stores it on a track and hold circuit. The fraction to subtract is tuneable through an analogue signal to be able to correct differences in the time response coming from differences in cell sizes, fibre lengths or radiation doses.

The comparison stage continuously subtracts from the integrator output the value stored in pile-up compensation block of the other path (that corresponds to the previous sample) and the threshold value set by a 7 bits DAC. A latched comparator, whose output would be validated and latched just before the end of the integration period, evaluates the sign of this subtraction. The output of the comparator is an ECL type signal, to reduce the pick-up noise. A multiplexor selects the comparator that it is in the latch state. An ECL to CMOS translator is needed to be able to drive the LVDS serialiser without adding external components. The output is differential to try to cancel the digital pick-up noise and to balance the supply currents.

Each path uses an independent DAC to be able to compensate the offsets due to process variations between different subchannels. It is a multiplying converter that uses a common differential external reference that can be changed for calibration and test purposes. The DACs are programmed through a serial interface to reduce the pin account. The memory elements of the digital part use redundancy mechanism to prevent the effect of single event phenomena.

Different internal clocks are needed to control the integrator, the track and hold, the comparator and the multiplexer. Special care is needed on its generation because the offset and the noise of the system is very sensitive to differences between the phases of the clock.

The required differential signal range for the analogue processing after integration would be ±1V, which is not easy to obtain with a supply voltage of only 3.3 V using a BiCMOS process (npn only). A MIP will be equivalent to 100-200 mV depending on the gain of the PMT.

IV.   DESIGN OF THE COMPONENTS.

A. Input stage.

The front-end preamplifier (see figure 3) consists on a bipolar pair with emitter degeneration. The gain is adjusted by the ratio between collector resistors and emitter resistors, and it is about a factor 6. The linearity is good enough for the level of input signals that must be processed; thus no compensation is needed. An emitter follower provides low impedance output, needed to decouple the effects of the switch on the integrators. The bandwidth of the block is higher than 200MHz for load capacitances smaller than 1pF according to Spectre simulations. The temperature coefficient (TC) of the block is quite small (TC<0.1%/C) thanks to the cancellation of the TC of the emitter and collector resistors (build with the same type of poly). This kind of open loop stage is widely used in other components because it allows to

have a high bandwidth, high input impedance, low TC, small area and to avoid stability troubles.
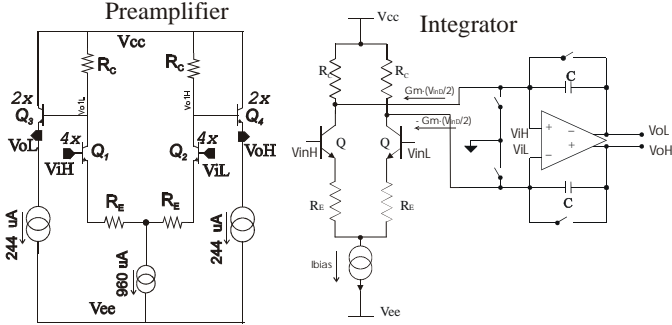

Figure 3: Input stage schematics: preamplifier and integrator.

In figure 3 is also shown the design of the integrator block. The input stage, which is also a bipolar pair with emitter degeneration (R_E), acts as a transconductor converting the input voltage to a differential current. This current is integrated by a fully-differential OpAmp with capacitive feedback (C), a detailed report on the design of the integrator and the OpAmp can be found in [5] (corresponds to the 5V version but the design is the same). For fast pulses almost all the differential current of the input pair flows through the feedback capacitors. The CMOS switches placed in parallel with these capacitors perform the reset and the ones connected to the input are intended to pull these nodes to zero during the reset phase. The integration time constant (τ_i) is given by $\tau_i = C \cdot R_E$.

The unity gain frequency of the OpAmp cause a pole in the integrator response, to fulfil the system bandwidth requirements the Gain bandwidth product (GBW) of the OpAmp must be higher than 100MHz. It is a fully balanced amplifier, having two stages and continuous common mode feedback (CMFB) circuit.

The noise and the offset of the discriminator are fixed by the input stage. A noise analysis must take into account the integration time ($\Delta T = 25$ ns). A small signal analysis of the main shot and thermal noise sources (for the preamplifier) in a continuous domain yields to equation (1) and (2), where $e_{n_O}^2$ is the power spectral density at the integrator output and $e_{n_I}^2$ is the power spectral density at the preamplifier input. Both are related through the amplifier gain (G) and the integrator transfer function ($H(j2\pi f)$). R_{LPMT} is an external resistor connected from each input pin to ground, r_b is the parasitic base resistance of the input pair and I is the bias current of this pair.

$$e_{n_O}^2(f) \approx 2 e_{n_i}^2 |G|^2 |H(j2\pi f)|^2 \qquad (1)$$

$$e_{n_i}^2 \approx 4KT\left(R_{LPMT} + r_b + R_E + \frac{R_C}{|G|^2} + 2q\frac{V_T}{I} \right) \qquad (2)$$

The main noise sources are the three first terms of equation (2), first order models are compatible with Spectre simulations where $e_{n_I}^2 \approx 100\ aV^2/Hz$. It can be shown that the Fourier transform of the impulse response ($H(j2\pi f)$) of a system that integrates a signal for ΔT follows expression (3):

$$H(j2\pi f) = \frac{1 - e^{-j2\pi f\Delta T}}{\tau_i\, 2\pi f} \qquad (3)$$

Equation (4) shows the noise voltage power $E_{n_O}^2$, a noise voltage of $E_{n_O} \approx 4\ mV\ r.m.s.$, within the required resolution.

$$E_{n_O}^2 = \frac{1}{2\pi}\int_0^\infty |G|^2 |H(j2\pi f)|^2 e_{n_i}^2 df = |G|^2 \frac{e_{n_i}^2}{\tau_i^2}\frac{\Delta t}{2} \qquad (4)$$

The offset of the discriminator depends on the matching of the resistors and bipolar transistors of the differential amplifier, the input referred voltage σ_{os} and current $\sigma_{i_{os}}$ offsets are shown in equations (5) and (6) respectively,

Statistical information is available from AMS to estimate

$$\sigma_{v_{os}} = V_T \sqrt{\left(\frac{\sigma_{R_C}}{R_C}\right)^2\left(1 + \frac{g_m R_E}{\alpha_F}\right)^2 + \left(\frac{\sigma_{I_S}}{I_S}\right)^2 + \left(\frac{g_m R_E}{\alpha_F}\right)^2\left(\left(\frac{\sigma_{\alpha_F}}{\alpha_F}\right)^2 + \left(\frac{\sigma_{R_E}}{R_E}\right)^2\right)} \quad (5)$$

$$\sigma_{i_{os}} = \frac{I}{\beta_F}\sqrt{\left(\frac{\sigma_{R_C}}{R_C}\right)^2 + \left(\frac{\sigma_{\beta_F}}{\beta_F}\right)^2} \qquad (6)$$

the value for the parameter tolerances for local variations, but it is not easy to estimate the effects of gradients in the die. Common centroid techniques, dummy devices and other layout strategies have been used to try to minimise both effects. The value of the integrator output for a zero input is called Output Zero Error (OZE), and can be related to input referred voltage and current offsets through equation (7) (it is an approximation of the transient response valid for t << 0.1 ms):

$$OZE \approx -v_{os} G\frac{t}{\tau_i} + 2i_{os} R_{LPMT} G\frac{t}{\tau_i} \qquad (7)$$
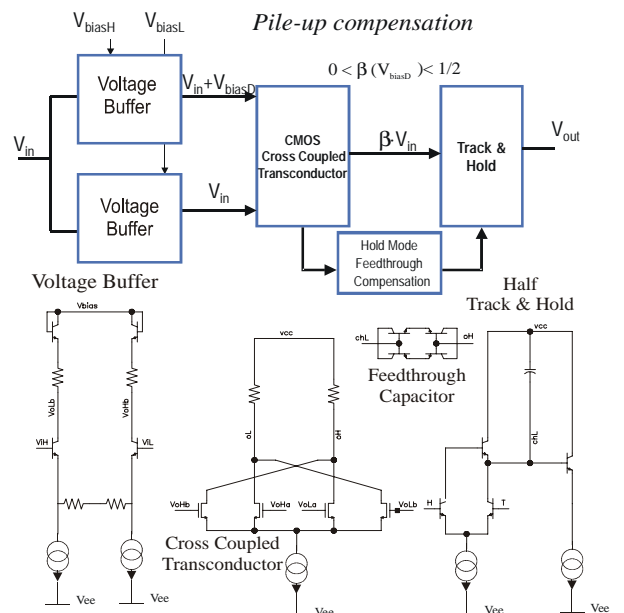
B. Pile-up compensation

Figure 4: Pile-up compensation block.

The functional diagram and the main parts of the pile-up compensation stage are shown in figure 4. The tunnable element is a voltage-controllable linear MOS transconductor based on the bias offset technique [6]. The inputs of this circuit are duplicated thanks to the cross coupled CMOS pair. If a shift ($V_{biasD}=V_{biasH}-V_{biasL}$) is created between the common mode of both inputs, if the differential mode is replicated and if the inputs are fully balanced, the output of the cross coupled transconductor (V_{Oxc}) is given by expression (8). Using the usual first order model for the MOS in saturation, the quadratic terms are cancelled and linear relation is obained. The transconductance is linear as long as all the transistor are in the active region, this condition requires a input range given in (9).

$$V_{Oxc} \cong 2K_N V_{biasD} V_{in} \qquad (8)$$

$$|V_{in}| < \sqrt{\frac{I_{bias}}{K_N} - \frac{3}{4}V_{biasD}^{\,2}} \qquad (9)$$

The shift in the common mode is created using two identical bipolar differential voltage buffers (fig. 4) with gain <1 to use the linear range given by (9). The positive rail of each buffer is controlled independently (V_{biasH} and V_{biasL}). A diode connected bipolar performs linearity compensation.

The circuit to store the value that will be subtracted to the next event is a derivation of a well known fully differential track and hold (T&H) [7]. Nevertheless, it is not possible to use the classical input stage (very similar to the bipolar voltage buffer described above) with a supply voltage of 3.3 V. The cross coupled transconductor plays this role, thus simplifying the T&H part but adding some requirements to the design of the pair itself. The T&H input is a follower that drives the hold capacitor and that is biased through a bipolar current switch controlled by the channel clock. Fig. 4 shows a half of the differential T&H and a circuit to compensate the hold mode feedthrough. The compensation is done connecting an output of the MOS transconductor with the hold node that corresponds to the complementary output through this circuit.

C. Comparison.

Three bipolar differential pairs with emitter degeneration are used to convert the outputs of the integrator, the DAC and the pile-up compensation stage to a differential current. Once this is done it is easy to subtract from the integrator signal the others. The result is converted to a voltage signal using a common collector resistor and linearity compensation.
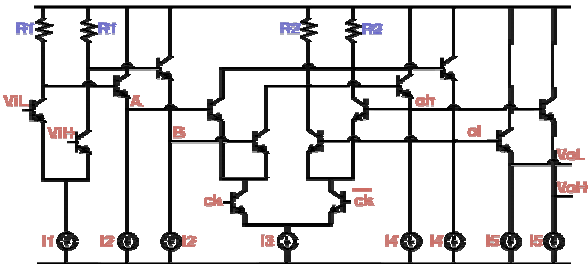

Figure 5: Latched comparator.

A latched comparator [8] evaluates the sign of the result of the previous operation. The comparator, shown in fig. 5, has two operation modes according to the clock level. In the acquisition phase amplifies the input signal while in the latch state it exploits positive feedback to reach the desired output levels.

D. DAC and digital control.

The DAC is a R-2R network that divides a floating reference voltage. Is a multiplying converter to have higher degree of freedom to calibrate and set the thresholds. It uses 1 bit to define the sign and 6 for the modulus. The layout use dummy switches and common centroid techniques to improve the linearity. The noise bandwidth is reduced to about 2 MHz using internal capacitors connected to ground.

Guard rings are widely used in all the components to prevent latch up, specially the Single Event Latch-up provoked by heavy ions. Another related problem is the Single Event Upset, to correct it all the memory elements of the digital part use a triple vote mechanism.

V. RESULTS.

No results on the 3.3 V version are currently available because it was sent to the foundry in May 2002. Previous prototypes of the chip have been designed before fixing the power requirements and they work at 5V, nevertheless the system architecture is equivalent and the principle of the majority of the blocks is the same.

The OpAmp and integrator experimental results are shown in table 1. The noise and OZE results are compatible with previous calculations and simulations done with the same procedure described in section 4.A.

Table 1: OpAmp and integrator results (measured for 10 samples).

OpAmp	
Input Offset	$<V_{io}>$ = + 1 mV σ_{Vio}=5 mV r.m.s.
GBW	$<GBW>$ = 180MHz σ_{GBW} = 4 MHz
CMRR	100 dB
Slew rate	90 V/μs
Common mode range	Vo= + 1.75 V to < -1.2 V Vi =+ 1.5 V to -1.5 V
Integrator	
OZE	$<OZE>$ = 38 mV σ_{OZE} = 70 mV r.m.s
E_{no}	< 1 mV r.m.s
τ_I	$<\tau_i> \approx$1ns with a tolerance <1 %
Bias current	2.5mA (including OpAmp)

A adjustable MOS cross coupled stage for the pile-up compensation was also tested. The input common mode range is from –1V to 0.8V and the differential input range is $|V_{in}| < 2V$. The linearity error for different transconductances (Gm) is <1%. The bandwidth is about 100MHz. The input offset voltage is $<V_{io}>$ = 5 mV σ_{Vio}=6 mV r.m.s. The noise voltage E_{no}< 1 mV r.m.s. Is important to know the matching between different channels in a chip because the control will be shared, figure 6 shows voltage gain of the block as function of the control voltage Vb for 10 circuits, the spread is

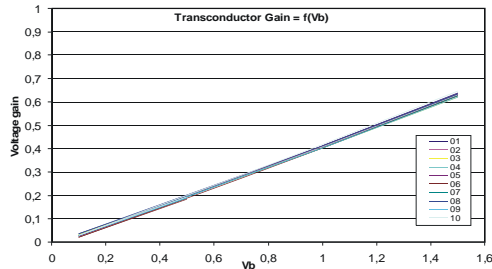always below 2%. The relationship between transconductance and Vb is quite linear as given in (8).

Figure 6: Voltage of variable Gm block (for 10 samples).

The DAC has been tested for different reference voltages between 100mV and 1V, having an INL error <0.5 LSB and a DNL <0.8 LSB. The settling time is about 110ns and the offset about 2 mV, a dependence on the sign was observed in the offset and has been corrected for the new version.

The test of about 10 circuits containing 4 channels confirm that noise and offset behaviour of the discriminator is fixed by the input stage (in this prototype no preamplifier was included, the integrator was the first stage). For the complete discriminator we have <OZE> = 35 mV and σ_{OZE} = 63 mV r.m.s. Differential signal range after integration is ±1 V (see fig. 7), the linearity error is <0.5% of full scale. A threshold sweep allows to study the noise of a complete channel (fig 7). It has been studied changing several conditions: different conditions for noise sources, i.e. other channels, (ECL and CMOS output pads, differential and single ended outputs) and using sockets or directly soldering on a PCB. A combination of pick-up and random noise effect has been found. In any case results range from 0.8 to 1.5 mV r.m.s, compatible with the noise study of the input stage, which clearly dominates above the others.
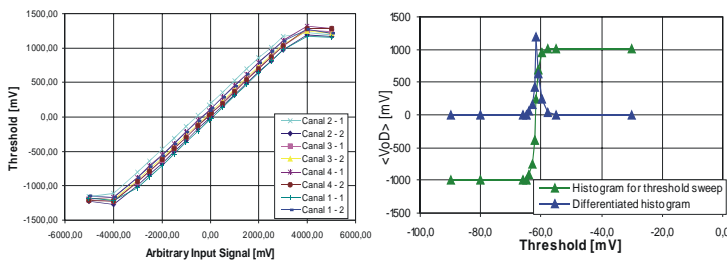

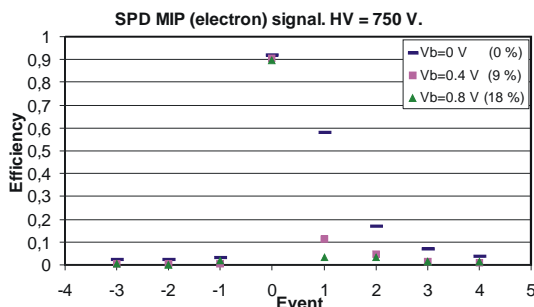Figure 7: Discriminator linearity (left) and noise (right).

Figure 8: SPD MIP signal for different pile-up corrections.

Figure 8 shows the response of a prototype of the system described in section 1 that was tested in a electron beam in CERN (July 2002). The efficiency of the discriminator output related to the calorimeter system trigger for different values of pile-up correction is plotted in a 8 sample time window around this trigger. The threshold was set only 3σ above the pedestal noise (<10mV, i.e. <0.1 MIP) in order to obtain a high sensitivity for the tails of the signal and to synchronise precisely the VFE clock with the trigger.

VI. CONCLUSIONS AND FUTURE WORK.

The design of a 3.3 V version of a full-custom synchronous discriminator is presented. The general architecture and some solutions are supported by the good results of previous prototypes working at 5 V. The power consumption will be reduced from 1.2 W to 0.6 W and the gain increased by a factor ≈3.

The next steps towards the 8 ch. prototype are to perform a complete functional and radiation tests. The study of the offset related to production tolerances is very important, since it could limit the dynamic range of the circuit because of the high multiplication factor shown in (7). Special care has been taken in layout design, but even local effects can be problematic. In case that it is needed, several solutions are under study: external offset cancellation (using the input bias current) and programmable offset trimming techniques.

VII. REFERENCES

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