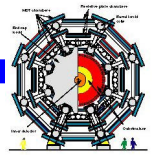


LECC Conference (LHC Electronics)

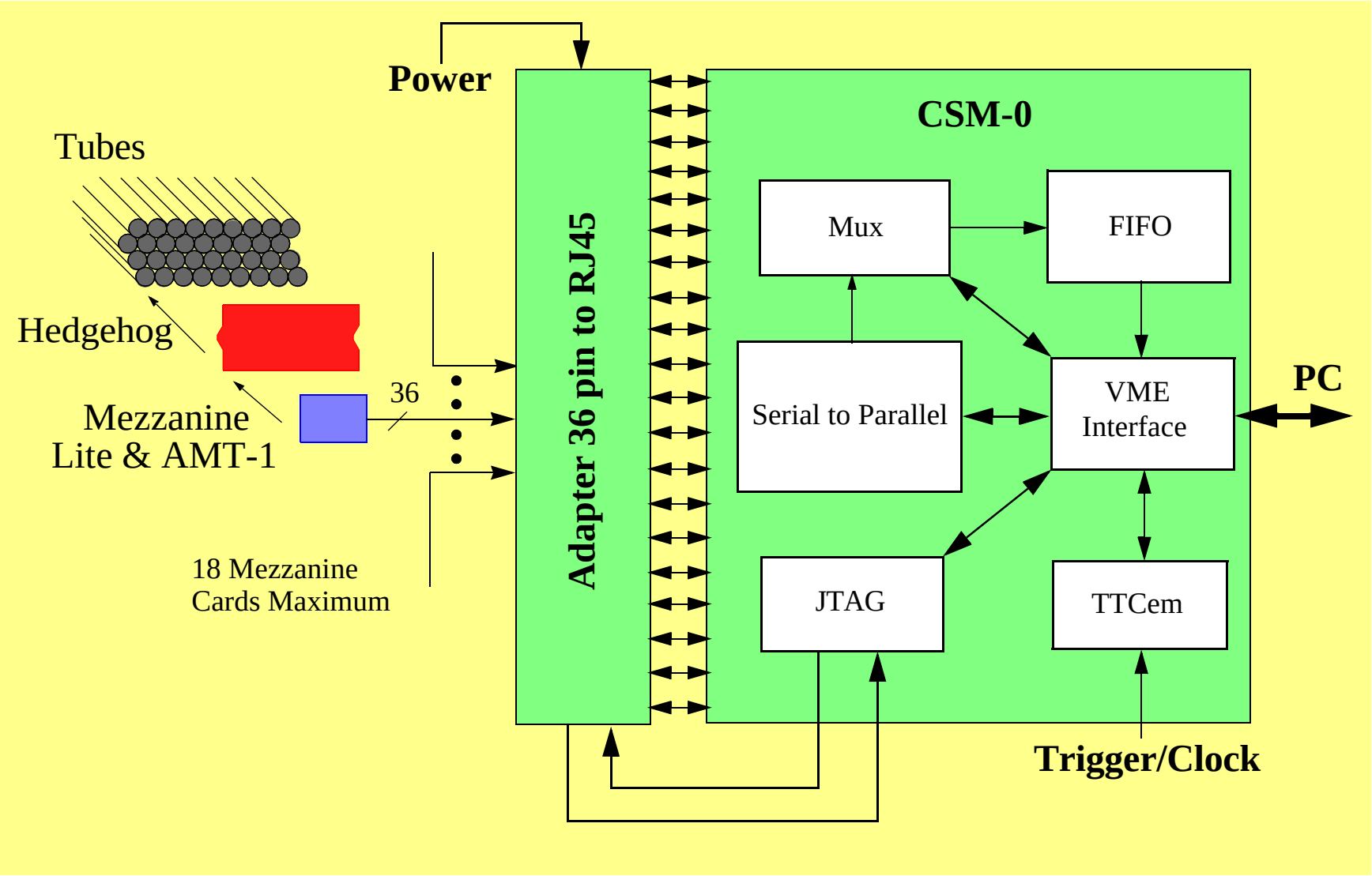
CSM module (Chamber Service Module) for MDT

P. Binchi - University of Michigan

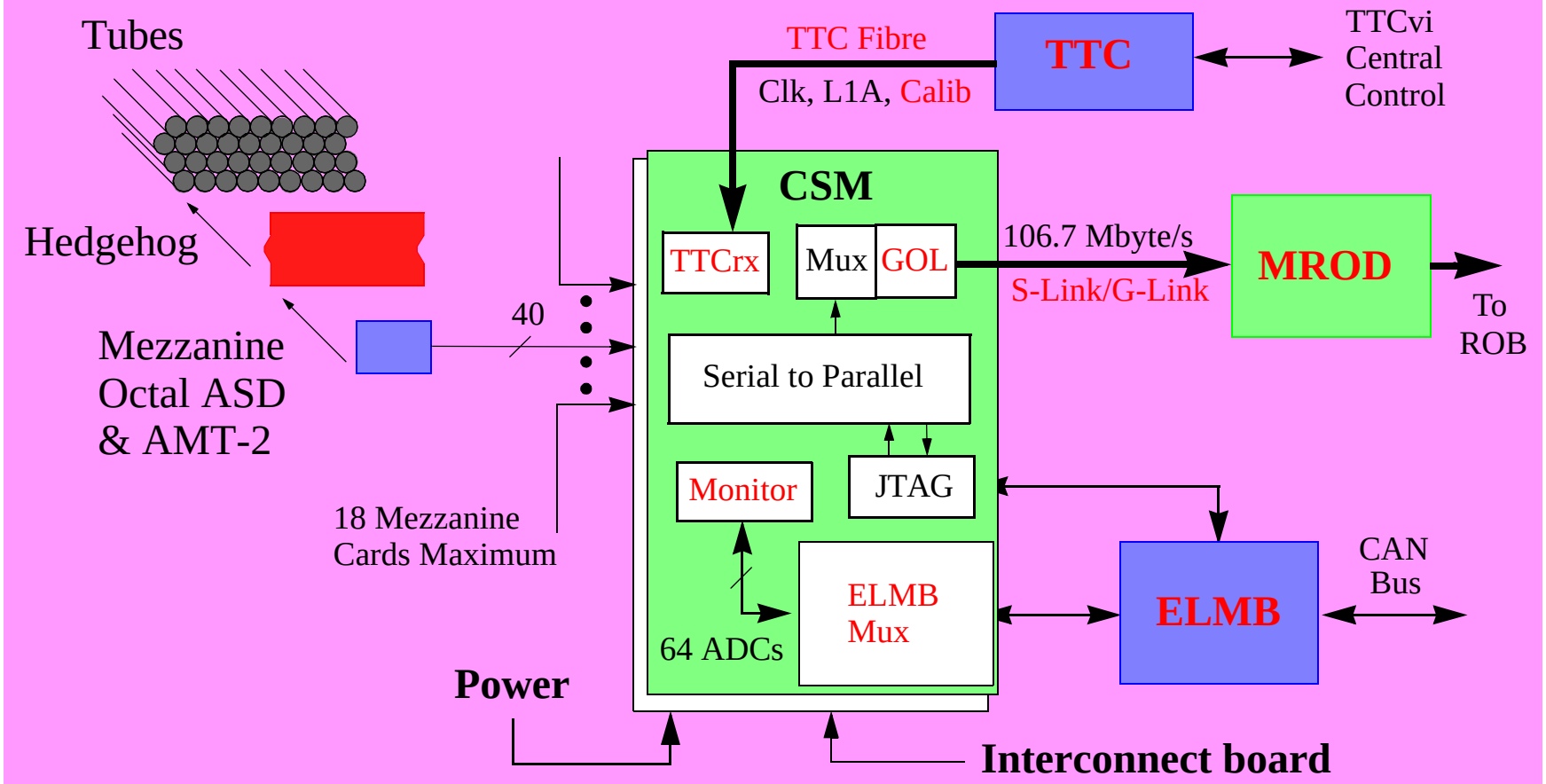
Colmar - September 12th, 2002

- Presentation Outline for CSM Status and Work Plan
  - Character and status of the prototype readout module & interconnect
  - Proposed final readout with comparison & contrast to the prototype
  - Major items & issues to be addressed in the final development
  - Responsibilities, work plan, & schedule for the final readout
- Priorities for multiplexer development (ordered first to last)
  - Passive card, cables, and connectors to complete the chamber assembly
  - Baseline CSM in FPGA (TDM & G-Link protocol via GOL)
  - Detailed costing for baseline FPGA & if possibly an ASIC version.

Previous Prototype (CSM-0)



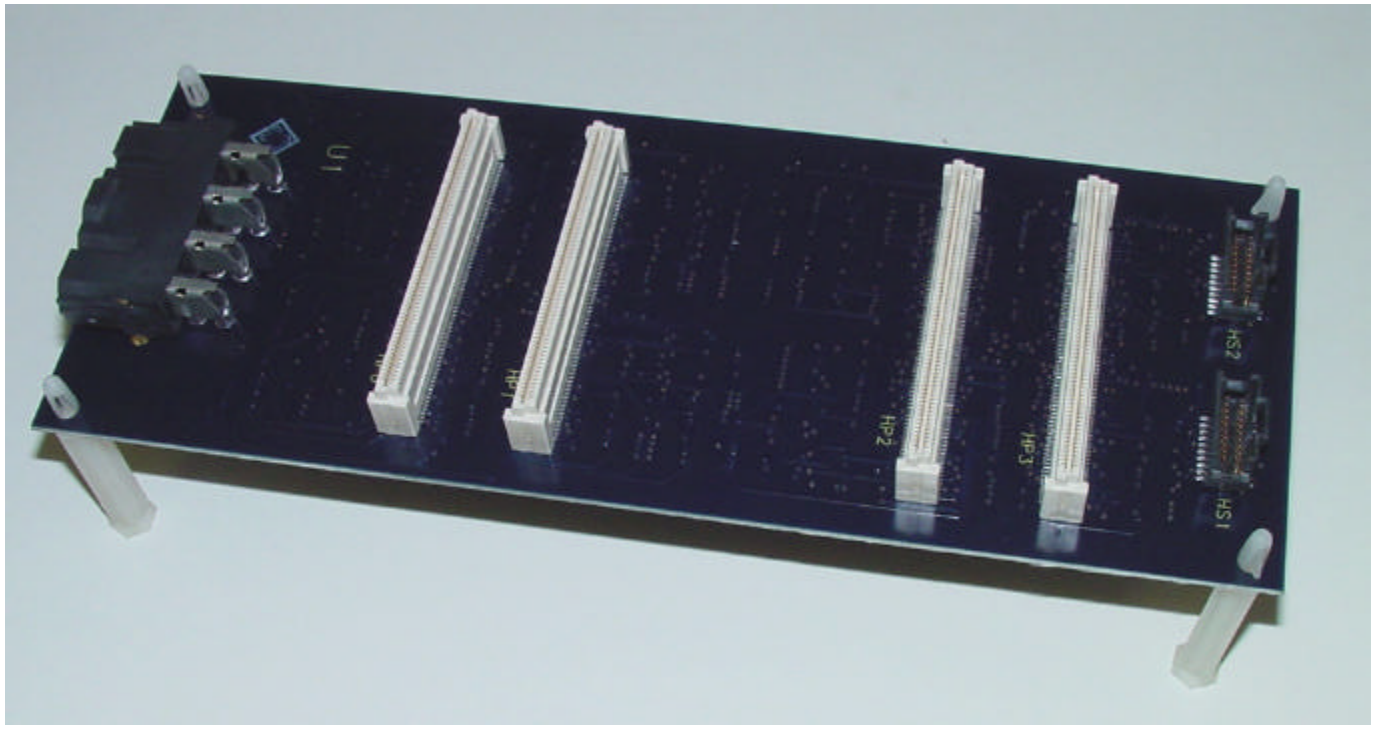
Proposed Chamber Service Module

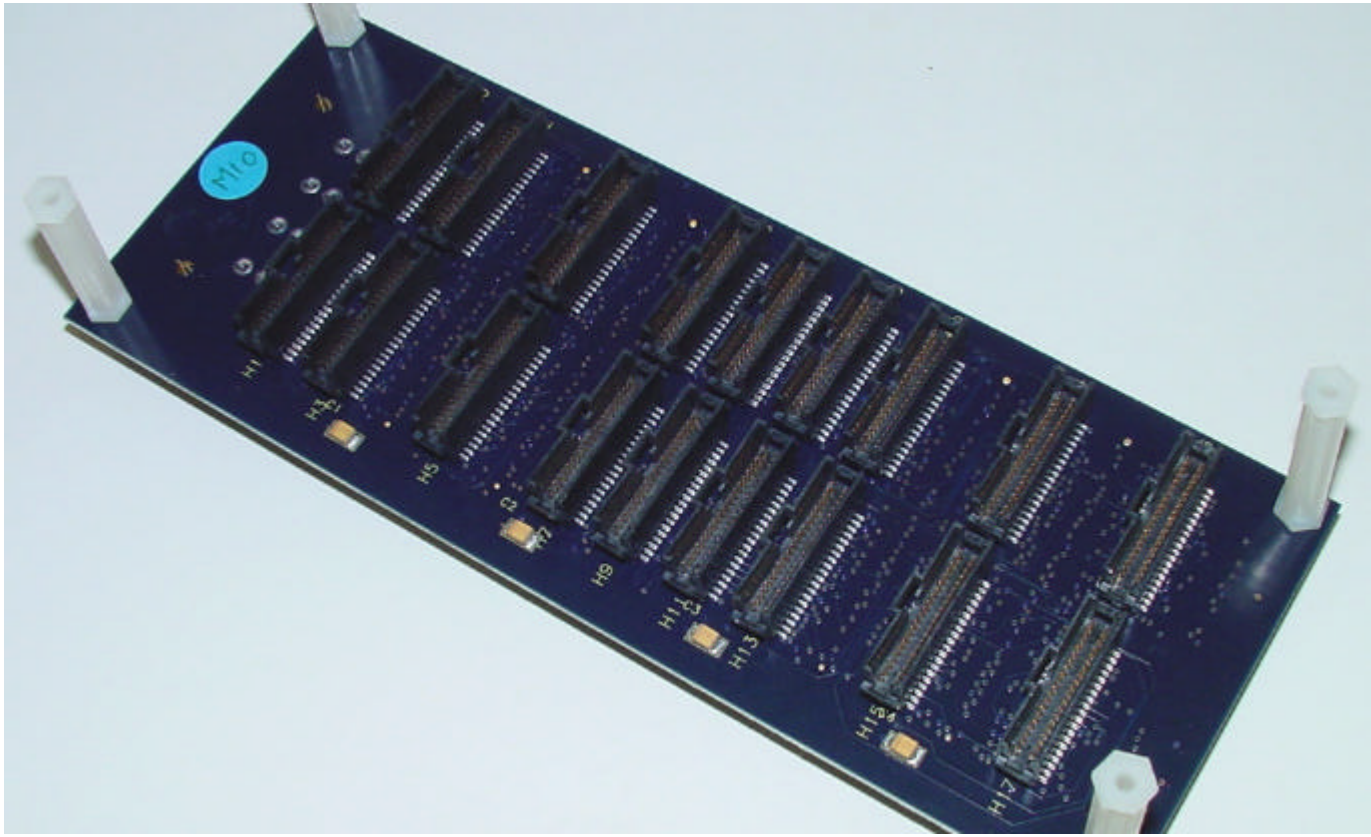


Note: All connections to the CSM are through a passive interconnect except the TTC and MROD systems

Passive Interconnect

A picture is shown below (top and bottom side):

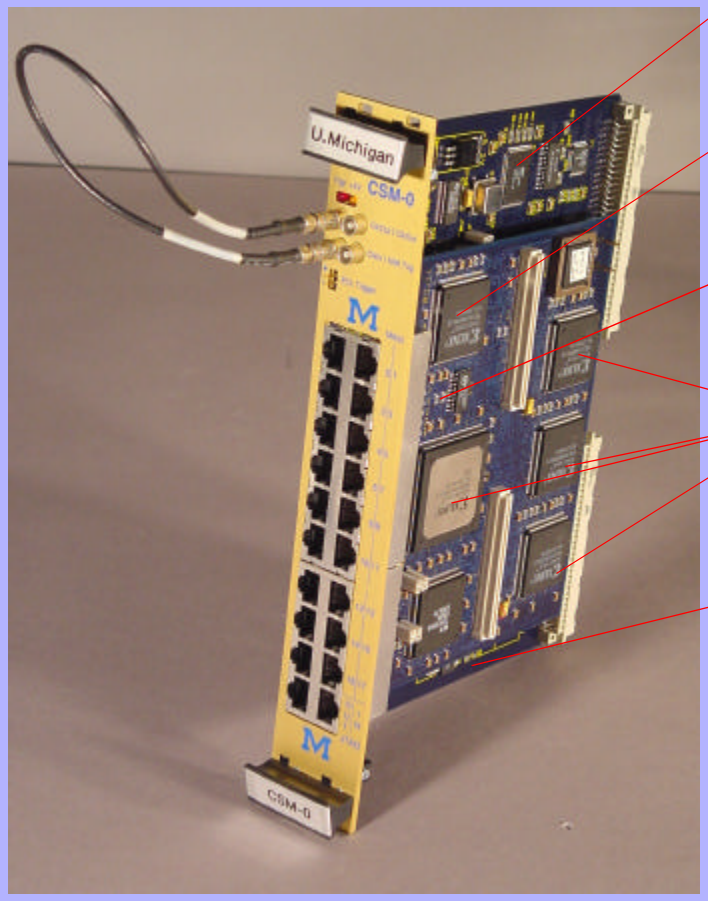




- **A small number has been pruduced so far. The first tests gave good results. Final production will be around 1200 units**
- **A short version is needed for chambers with 12 TDC**
- **A review & tests are needed to confirm the electrical & mechanical compatibility**
- **Prototypes are needed to build an example assembly**

What's Different from the Prototype?

Existing CSM-0 Module



FIFO → G-Link/S-Link to MROD

1 28mm FPGA → 1 10mm TTCrx + receiver

Clock Fanout → In FPGA DLL (DCM)

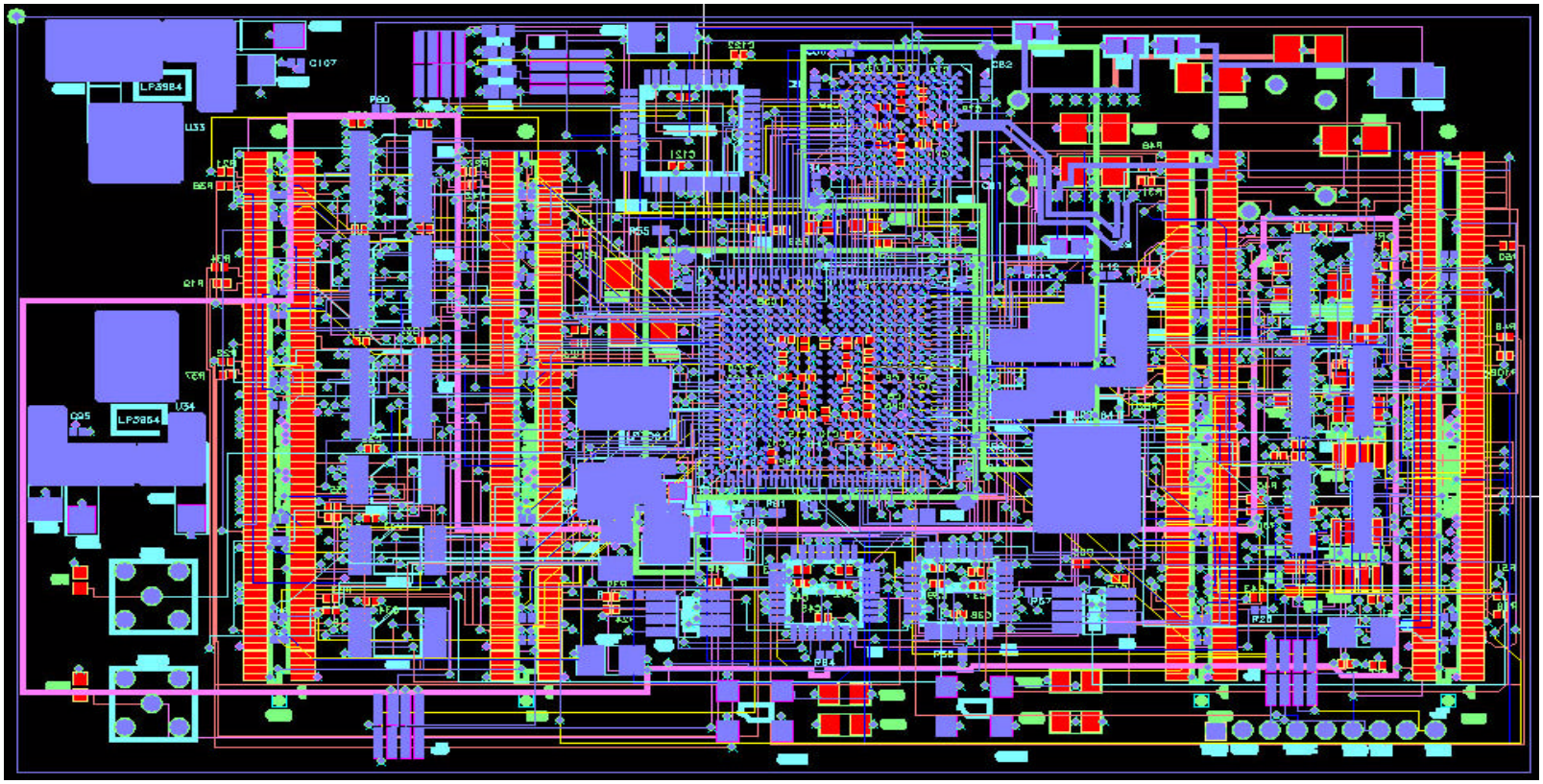
3 28mm FPGAs → 1 23mm FPGA &1 40mm FPGA

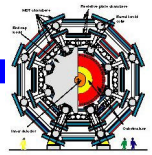
115 x 166mm board → 80 x 130mm

LVDS on VME → LVDS in FPGA

Event Building → Time Division Mux

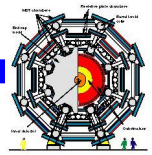
CSM-1 board





CSM1

- dimensions 80mm x 130mm;
- it is an intermediate board in order to test the new CSM structure focused on the functionality of the single bigger FPGA and on the S-Link fiber data transmission.
- TTCrx ASIC -> external TTL triggers from a connector and 40 MHz clock provided by a high precision oscillator (on discussion)
- G-Link optical comunication to MROD via GOL
- No ELMB multiplexing on it (DCS mux is to be copied later).
- JTAG communication with the user by opto-isolated connection to a PC.



ATLAS

- JTAG communication among all the internal (FPGA, Flash RAM) and external (TDC's) programmable units.
- 3 different voltages: 1.5V, 2.5V, 3.3V;
- connected to the motherboard through four 2mm spaced 140 pin connectors: all signals, JTAG chain, power supply come from them;
- 5 mils (0.127mm) traces with 5 mils clearance between traces and traces and vias in the board.
- 10-layer board: 7 signal layers and 3 power layers (input 4V power, 2.5V and 1.5V supplies share the same layer)

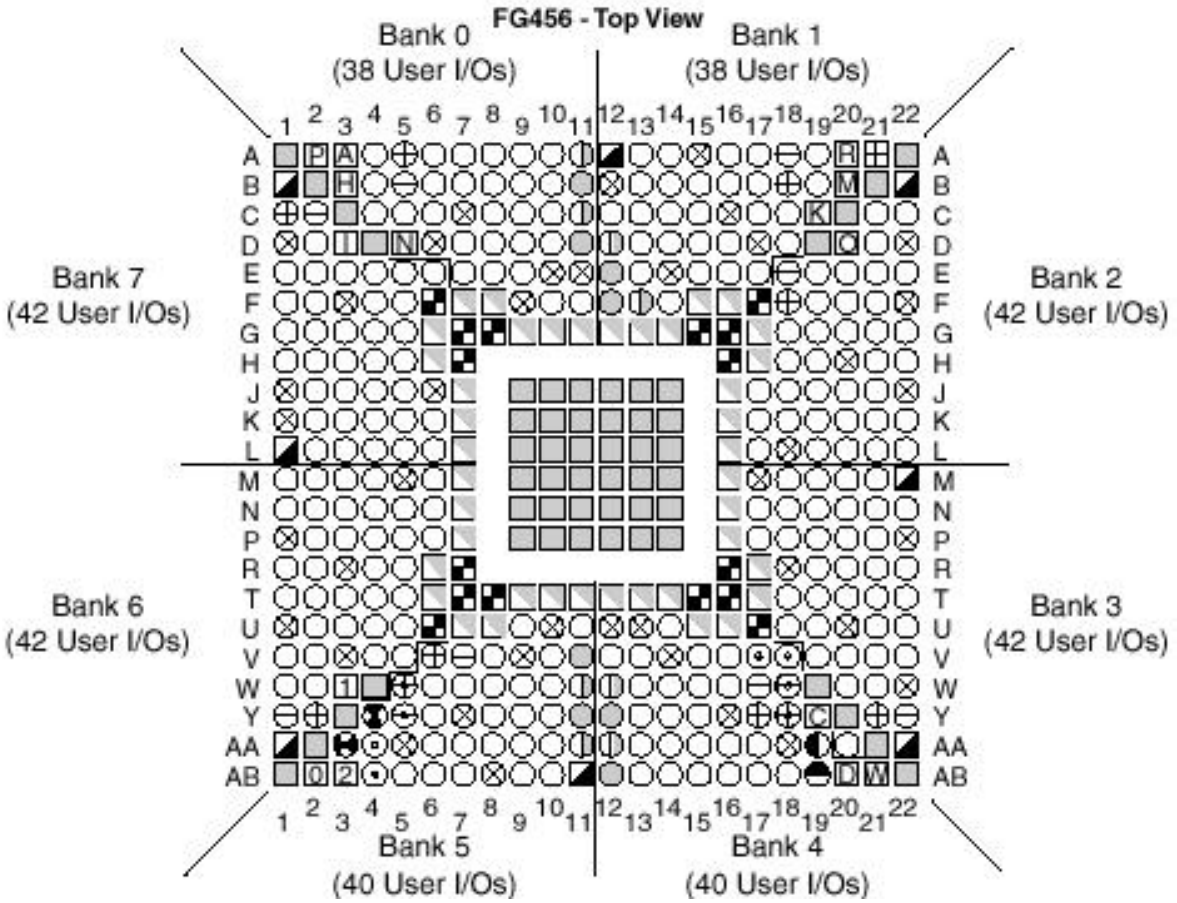
CSM-1 Prototype: technical view of its parts.

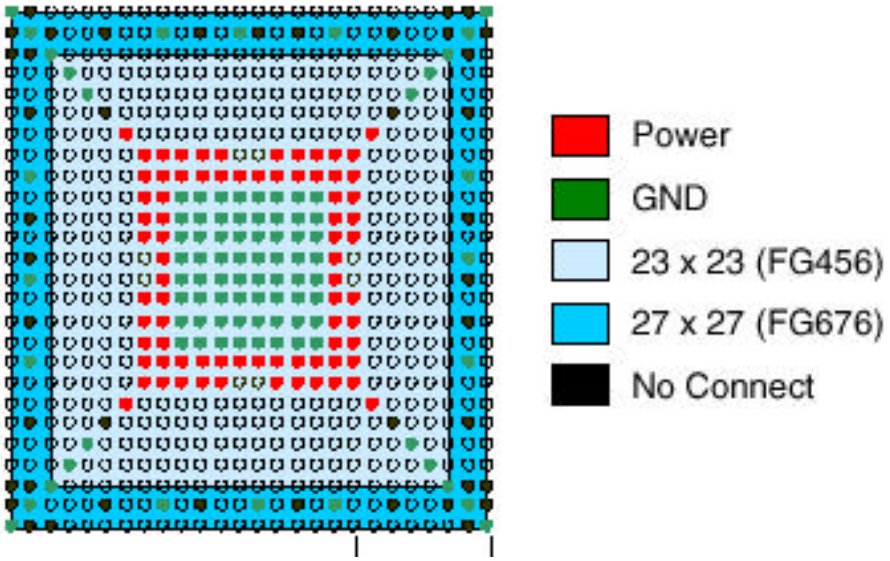
- **Xilinx Virtex II Field Programmable Gate Array (FPGA)** : it's the latest multifunctional version of FPGA. Used chip XC2V1000FG456.

Main Features:

- 1mm fine pitch ball grid array chip with 456 inputs/outputs (effective 324 IO pins available). Size: 23mmx23mm;
- 1 Million system gates
- Its pins are divided in 8 different blocks and they can be either LVTTL or LVDS (and other options) in all voltage values;
- 8 internally implemented DCM Units (digital clock manager) can originate clocks at the required frequences through numberous multiplications and divisions of the input clock (used for the internal clock phasing and for developing other clocks as needed for the optical data transmission);
- The functions of the four FPGA's in the CSM-0 will fit in just one VIRTEX FPGA if a mechanism to automatically synchronize the data coming from all 18 mezzanine cards to the local 40MHz clock is devised (and so it is).

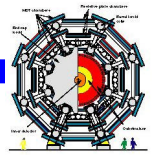
- 1.5V core power supply;





Xilinx XC18V00 Series PROM:

- it contains the bit code to program the FPGA;
- it is not really a PROM but more properly a flash RAM since its content can be erased and rewritten up to 20,000 times;
- its code is downloaded through boundary-scan (JTAG);



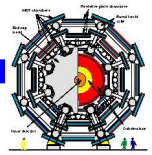
- it can program the FPGA both in master/serial mode and through JTAG;

- cheap and small in size.

- **Voltage regulators:** three are needed:

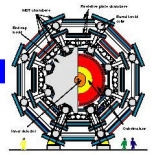
  - **1.5 V -** for the FPGA's core CMOS logic;
  - **2.5 V -** for the GOL chip power supply;
  - **3.3 V -** for the FPGA IO signals (both TTL and LVDS), the FPGA and all the remaining chips (optocouplers, fanouts, JTAG, transceiver....).

- **Optical isolators:** four signals are optically isolated for the JTAG transmission: three are inputs to the module (TDI, TCK, TCS) and one is output (TDO). Three Agilent HCPL063L chips are used (3.3V power supply).



ATLAS

- **Gigabit Optical Link chip (GOL)**: it is a multi-protocol high-speed transmitter ASIC.
  - designed with 0.25 um CMOS technology;
  - it sustains transmission of data as fast as 1.6GBit/sec;
  - it can transmit data both in Ethernet and G-Link mode, slow and fast transmission (800Mbit/sec vs. 1.6Gbit/sec);
  - Boundary scan (JTAG) compatible;
  - It is the interface between the master unit (FPGA) and the physical transmitting component.
- **Small Form Factor Infineon Transceiver**:
  - Part # V23818-K305-L57;
  - both receiver and transmitter, here only used as a transmitter;
  - single power supply (3.3V);
  - 1.5 Gbit Ethernet transmission;
  - 850 nm laser;



- connected to optical fiber for up to 550m transmission;
- it sends serial data to the MROD according to the SLINK protocol.

- **Clocks and signals multiplexers/fanouts**:
  - they create copies of signals in order to save IO pins coming out from the FPGA;
  - they fanout both LVDS and LVTTL signals.

Ball Grid Arrays (BGA) chips placement and routing

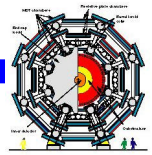
- both the VIRTEX 2 FPGA and the GOL chip have a fine pitch ball grid array layout (1mm spacing between IO pins);
- Ball Grid Arrays layout allows a much higher quantity of pin availability than regular “flat” chips for the same amount of space;
- on the other side each used I/O pin (except for the external ones) needs a via in order to have the possibility to route the signal connected to it and avoid crossing traces.

DATA TRANSMISSION

The board will send data information according to the S-Link protocol; it will send continously 18 data words from the 18 TDC's followed by a spacer word:

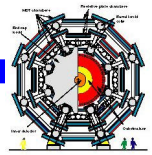
TDC 0 Data Word
TDC 1 Data Word
.....
TDC 17 data Word
Spacer
TDC 0 Data Word
.....

The spacer word will have a 4 bit code and 18 parity bits, one for each previous 18 data word.

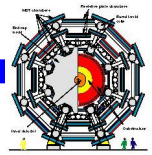


AUTOPHASE

- each data coming serially from the tubes through the TDC units is synchronized to its own 40MHz clock;
- all these clocks have indipendent phases from each other (depending from the cable length) and from the CSM1 clock (the frequency is the same);
- internal DCM units provide as default the four translated phases of the input clock (90-180-270 degrees): by using these outputs serial data from TDC's are analyzed on each phase and the most convenient one is chosen (with the most reliable data bit);
- DCM is also used as a DLL (delay locked loop) to synchronize the 25MHz clock with the parallel data to be sent to the GOL;
- below is shown how the DCM unit (it is a hardware unit!) is istanti-ated in VerilogHDL:

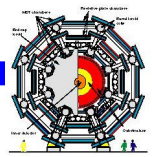



```
DCM dll (
  .CLKIN(CLKIN),
  .CLKFB(CLKFB),
  .RST(RESET),
  .DSSEN(),
  .PSINCDEC(),
  .PSEN(),
  .PSCLK(),
  .CLK0(CLK0_dll),
  .CLK90(),
  .CLK180(),
  .CLK270(),
  .CLK2X(),
  .CLK2X180(),
  .CLKFX(),
  .CLKFX180(),
  .STATUS(),
  .PSDONE(),
  .CLKDV(),
  .LOCKED(LOCKED));
```

JTAG CHAIN AND COMMUNICATION

- IEEE Std. 1149.Boundary Scan (better known as JTAG) provides both the configuration bitstreams to the programmable units and the communication (both ways) between the CSM1 module and the external units;
- JTAG is a protocol which uses 4 signals (3 inputs TDI, TCK, and TMS and 1 output TDO) to send and receive data streams serially and its standardization allows the possibility to put on a single chain all different kinds of component which support it and exchange data among all of them;
- JTAG chain in the CSM1 module contains the PROM, the FPGA, the 18 TDC's and the GOL chip;
- during setup the configuration bitstream is sent to the PROM which programs the FPGA which eventually sets the connected TDC's in the global JTAG chain;
- the FPGA can also be programmed directly but in this case the configuration will be volatile (reset at power-off)
- in the prototype 4 jumpers are used to include/exclude each single unit from the JTAG chain for testing purposes;

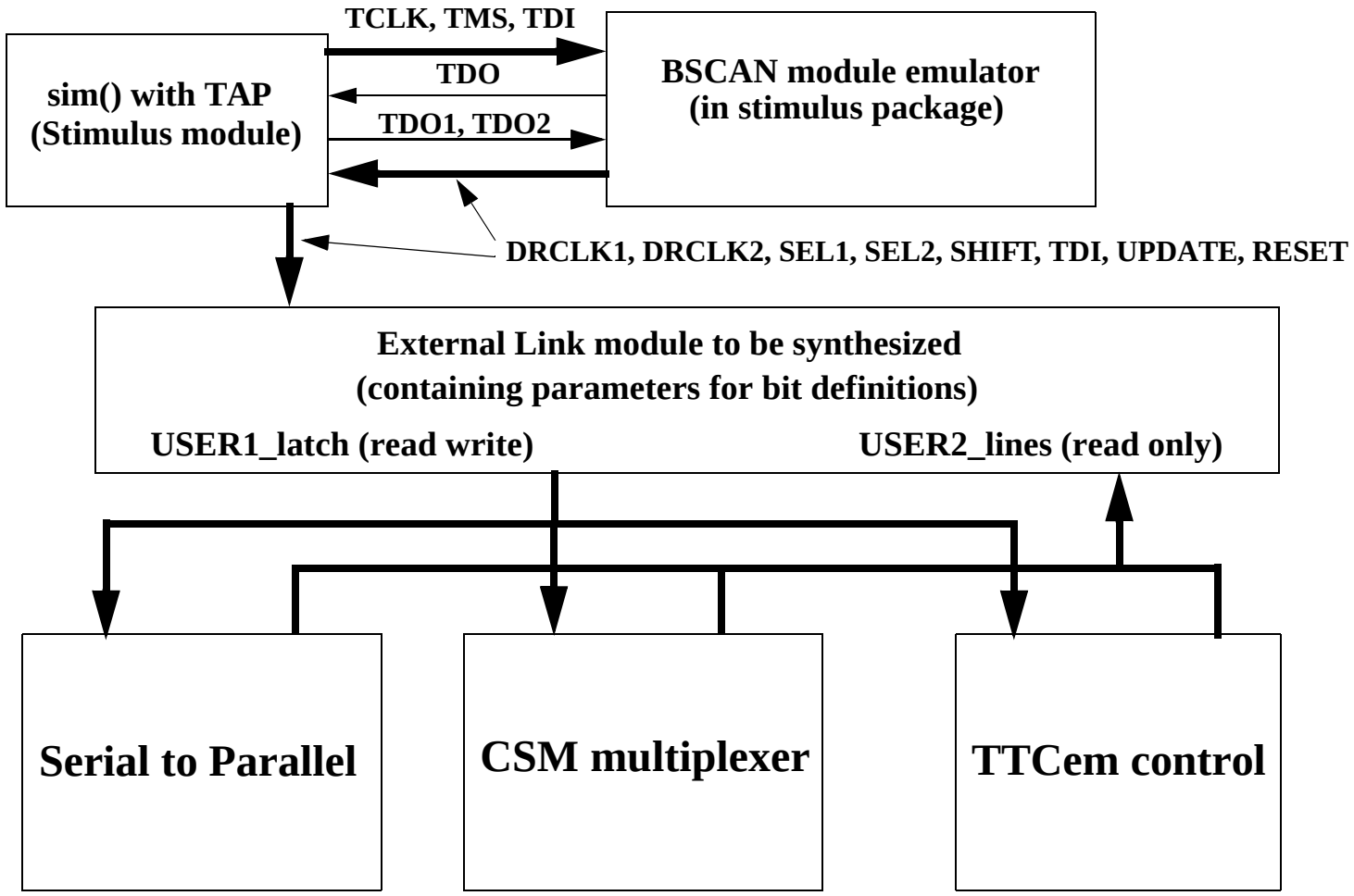


ATLAS

- An internal module called BSCAN Virtex2 allows the JTAG communication both ways through two registers called USER1 (read/write) and USER2 (read only);
- BSCAN_VIRTEX2 module instantiation in VerilogHDL (it is a predefined hardware module internal to the FPGA):

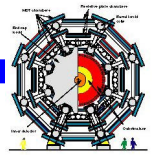
```
BSCAN_VIRTEX2 jtag(
  .TDO1(TDO1_OR),// USER1 register sequence out
  .TDO2(TDO2_OR),// USER2 register sequence out
  .DRCK1(DRCLK1),// Serial clock for USER1
  .DRCK2(DRCLK2),// Serial clock for USER2
  .RESET(JTAGRST),// JTAG reset (might use reset)
  .CAPTURE(CAPTURE),// capture register selected
  .SEL1(SEL1),// USER1 register selected
  .SEL2(SEL2),// USER2 register selected
  .SHIFT(SHIFT),// Shift data in/out of selected
  .TDI(TDI),// New data shifted in
  .UPDATE(UPDATE));
```


Scheme of the BSCAN_Virtex2 JTAG communication



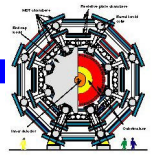
Main differences Prototype CSM-1 & Final CSM

- **TTC:** the TTCrx chip will be installed directly into the board and not emulated;
- **40 MHz Clock:** it will be provided by the on-board TTCrx chip;
- **JTAG:** JTAG programming will be mastered in the prototype board by a connection to a PC with an appropriate JTAG card. In the Final CSM this function will be provided by either the TTC or the DCS system.
- **ELMB multiplexer:** it will be mounted on the final prototype on the back side of the board (calibration and sensor settings).



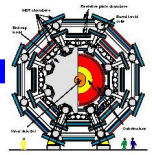
Major Items Addressed and to be Addressed

- Certification and integration of the passive interconnect
- Implementation of CSM in a single FPGA with LVDS I/O
  - A simplification since it removes external busses & pipeline steps
  - A simplification since event building is converted to time division multiplexing
  - Requires clock phase synchronization between 18 TDCs with different cables
- Installation of S-Link core in FPGA for fiber protocol
- Integration of TTCrx chip in place of TTCem in FPGA
- Radiation tolerance of all CSM components
  - Infineon optical transceiver, FPGA, & flash memory
  - Other components are same as used in DCS and will be certified in that context
- Design to sense and recover from SEU faults.



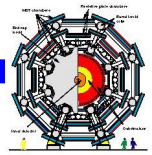
Responsibilities

- Passive interconnect - the first produced small stock is being tested, slight modification of the design before the final production (already quoted at around $150 each) - UoM
- CSM active board - UoM
  - FPGA code evolving to Time Division Multiplexing -
  - Integration of TTCrx - replacing TTCem - parts from CERN
  - Init of FPGA from Flash memory, JTAG routing to TDCs, & SEU detection
  - Layout of FPGA, TTCrx, fiber encoder, fiber transceiver, DCS mux/JTAG
  - Calibration fanout from TTCrx to Mezzanine cards
- Mezzanine cards & cables - Harvard/BU
- MROD - NIKHEF/Nijmegen
- TTCrx/ELMB/DCS - CERN



Work Plan

- Production and testing of the intermediate step CSM-1 (Single FPGA, ready for production)
  - Containing time division multiplexer with data in final format to MROD in standard S-Link mode through optical transmission.
  - Containing optical isolated JTAG from commercial driver
  - LATEST NEWS: upon availability of the TTCrx chip the CSM1 board will be equipped with it and it will not use the emulated TTC. The version will be much closer to the final prototype (good!) but it will delay slightly the production of the first stock of CSM1 boards (~2weeks).
- Final CSM with DCS/Mux/JTAG/TTCrx/G-Link core
  - Requires: stabilized design, radiation certified parts, & verified S-Link core
  - GOAL: working and available final CSM units for the Summer 2003 Test Beam at CERN.



Team

- J. Chapman - faculty (coordination/documentation)
- Tiesheng Dai - researcher (Board testing/Software development)
- Pietro Binchi - engineer (CSM-1 board design)
- Jeff Gregory - student (MiniDaq updates/Octal ASD code/ MDT chamber readout)
- Tuan Bui - student (CSM-0 certification/FPGA synthesis)