CALIBRATION BOARDS FOR THE ATLAS LAr CALORIMETERS

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Abstract

In order to calibrate the ATLAS Liquid Argon (LAr) calorimeters to an accuracy better than 1%, over 16 bit dynamic range, chips have been designed in DMILL technology. The design and performance of a 16 bit DAC, a static low offset operational amplifier and a digital chip to control the calibration boards are presented.

A 8 channels board using these chips has also been realised and carefully measured as this module will be replicated 16 times to design the final 128 channels calibration board.

I. INTRODUCTION

The LAr calibration boards, which are located right on the cryostat in dedicated front-end crates [1], house 128 pulsers which generate accurate pulses to simulate the detector signal over the full 16 bit dynamic range.

To equip module 0 calorimeter, 10 boards have been produced and extensively used in the test beam for the last three years. Their performance has met the requirements in particular in terms of uniformity [2]. However, they make use of many COTS.

Since then, several developments have been realised in order to design the "final" ATLAS calibration board, based on the same architecture but completely radiation tolerant, by migrating most of the COTS into DMILL ASICs , in particular a low offset operational amplifier, a 16 bit DAC and all the digital part.

The measurements of all these DMILL chips as well as their performance on a small 8 channels prototype are presented below.

II. REQUIREMENTS AND PRINCIPLE

A. Requirements

The calibration board is used to inter-calibrate the 200 000 readout channels and measures their three gains [7]. Thus, each calibration channel must generate accurate pulses to simulate the detector signal over the full 16 bit dynamic range. It is based upon 128 0.1% precision DC current sources and HF switches which transform the DC current into fast pulses (Rise time below 1ns) with a 400 ns exponential decay. To keep the constant term better than 0.7%, the accuracy of the calibration must be good and so the integral non linearity lower than 0.1% and the non uniformity between channels better than 0.25 %.

The radiation levels anticipated at the LAr crate location is 50 Gy in 10 years and 1.6 10^{12} N/cm^2. Taking into account the safety factors required by the rad-tol policy [3] , they must be qualified up to 0.2-3 kGy (20-300 krad) and 1-5 10^{13} N/cm^2, depending on the process. For DMILL chips, the radiation tolerance criteria (RTC) are

- $RTC_{TID} = 3.5*1.5*2*50 = 500$ Gy
- $RTC_{NIEL} = 5*1*2*1.6 10^{12} = 1.6\ 10^{13}$ N/cm^2
- $RTC_{SEE} = 5*1*2*0.7 10^{11} = 7.7\ 10^{12} h_{>20MeV}$/cm^2

B. Pulser and 128 channels board principle

The fast output voltage pulse is obtained by interrupting a precise DC current that flows in the inductor. When a fast TTL command pulse is applied on the NPN transistor, the PMOS transistor is OFF and the current is diverted to ground. The magnetic energy stored in the inductor produces a voltage pulse with an exponential decay. The pair PMOS-NPN transistors is referred as the HF switch.

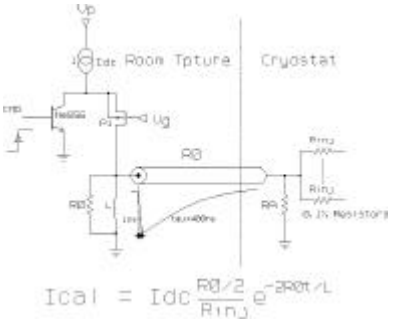

Figure 1: *Pulser principle*

To generate the precise DC current from 2 µA to 200mA, a *16 bit DAC* is necessary. The DAC voltage which varies from 16 µV to 1V is distributed to the 128 pulsers thanks to a *low offset operational amplifier* in voltage follower configuration. The voltage to current conversion is built upon a low offset op amp in voltage to current converter configuration and a precise 0.1% 5 Ω resistor.

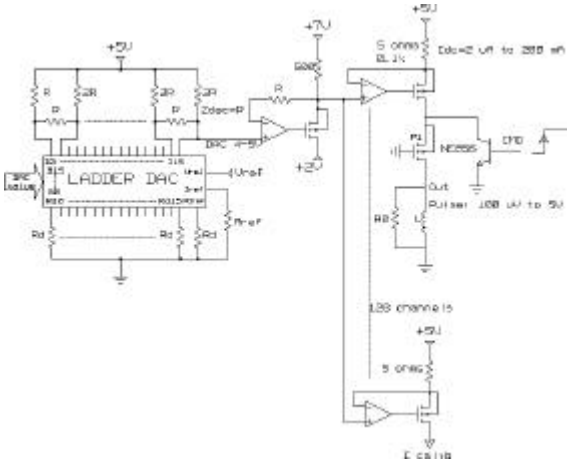

Figure 2: *Simplified schematics of the analog part of the 128 channels calibration board*

III. 16 BIT DAC

A. Requirements and design

A 16bit DAC with 10 bit accuracy is necessary to cover the full dynamic range of ATLAS and COTS did not provide adequate radiation tolerance. Therefore, a 16 bit R/2R ladder DAC has been designed in DMILL technology.

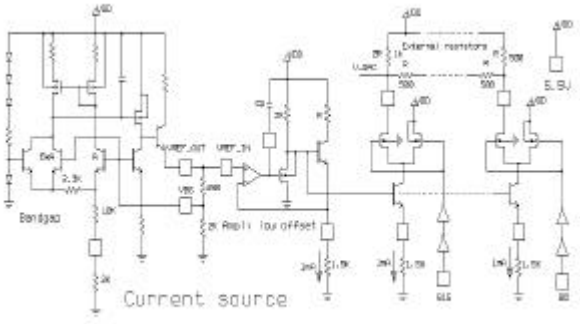

Figure 3*: Schematics diagram of the 16 bit DAC (V2)*

This DAC (Figure 3) is an array of 16 identical switched current sources driven by a common reference source. To reduce the sensitivity to V_{BE} mismatch and variations with temperature the emitters of the current sources are strongly degenerated (1mA in 1.5 kΩ ⇒ 1.5 V) with precision resistors (0.1%) which are external. Each digital input is connected to two complementary MOS transistors (switches) which feed the collector current in the R/2R ladder.

The second DMILL version (DACV2) is identical to the first one (DAC V1) except for the *reference source* in which a current mirror was causing a slight degradation under gamma irradiation. Thus, the DAC V2 integrates an improved reference source: a band gap reference has been incorporated and the current mirror has been replaced by a reference source built around a low-offset op amp as described below and mounted in current source configuration. The 1.5 V reference input voltage is converted into a reference current with the same external 1.5 kΩ precision external resistor. The base voltage is then distributed to all the identical NPNs forming the 16 current sources.

B. Performance

123 DACs V2 were received in May 02.

The performance measured is 0.01% integral non linearity over the 3 shaper gains, 1,10,100, as shown in Figure 4. The temperature stability has been measured on 10 chips between 20°C and 65°C and the slope is +0.01%/K.

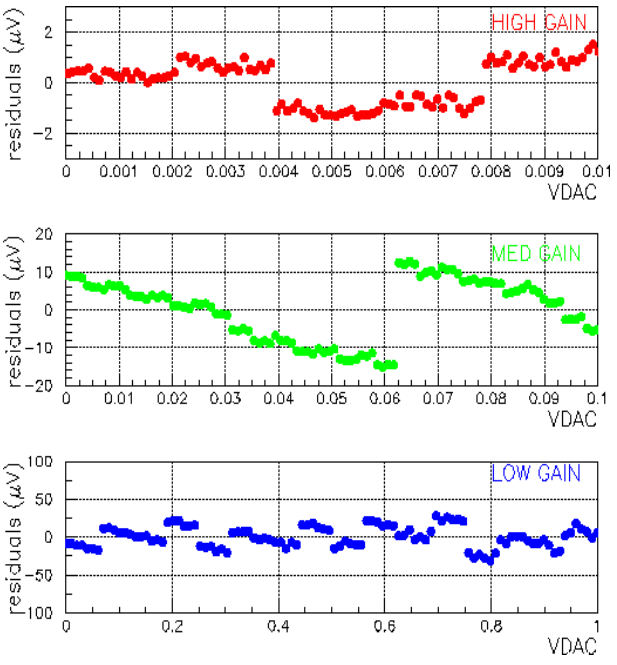

Figure 4*: Residuals of a linear fit over the 3 shaper gains*

C. Irradiation tests

10 DACs V1 chips have been irradiated up to 9. 10^{13} N/cm^2 at CERI in Orleans (20 MeV) and to 2 kGy ^{60}Co in Saclay and measured on line. Results have been detailed at the LEB7 in Stockohlm [4] and indicate good

tolerance to Neutrons. A 0.1% overall shift was observed under gammas irradiation and has been traced down to a change in the reference current built around a current mirror, as explained above. Although acceptable it has been corrected in the second DMILL iteration and 10 DACs V2 will be irradiated under gammas next December to check the tolerance with the new current reference.

IV. LOW OFFSET OP. AMP.

A. Requirements and design

The low offset op amp is the key element to build the precision DC current sources and also to distribute the DAC voltage to the 128 channels.

Thus, the op amp offset should be smaller than the DAC LSB=16µV. More than the offset value itself, its stability in time and with temperature is important. It must be independent of the input DAC value. The integral non linearity of the DC output current must be smaller than 0.1%. Again COTS as the OP497 used on the module 0 boards did not provide adequate radiation tolerance. After prototyping in AMS, the static low offset op amp has been translated into DMILL technology.

As shown in Figure 5, the circuit is built around a bipolar differential pair and external precision collector resistors (150 kΩ 0.1%). The transistors are 10*1.2 NPN, mounted in centroid configuration. A larger transistor size would in principle further reduce the offset, but would decrease the radiation hardness due to a too low current density. This input stage provides a gain of 127, enough to disregard the second stage offset.

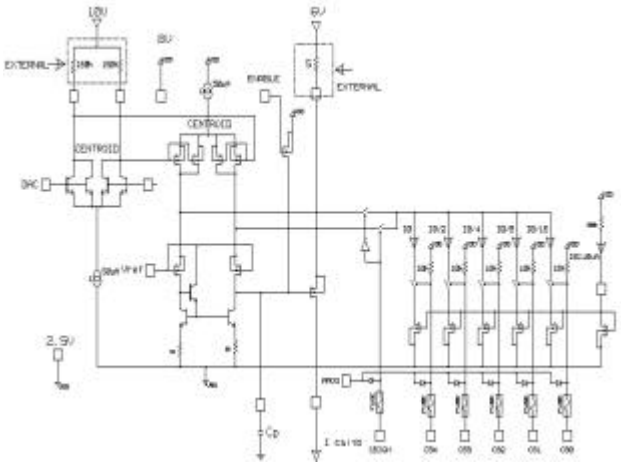

Figure 5: *Schematics diagram of the low offset op amp*

The second stage is built around a cascoded PMOS differential pair, again in a centroid configuration. A bank of 5 binary scaled current sources allows to add or remove up to 20% of the static current and allows further trimming down to ± 10µV. Only op amps with initial offset lower than ± 200µV will be trimmed. The output stage is a large (20,000/0.8) PMOS in order to drive the large maximum output current (200 mA).

B. Performance

40 chips of the first DMILL version (V1) have been received in march 2001: 37 were fully functional, giving a functional yield of 94% for a chip area of 2 mm^2.

A final version V2 has been realised to integrate the HF switch. The op amp is exactly the same as the one integrated in V1 version. 593 3mm^2 chips in plastic package PQFP44 were received in November 01 and 574 were functional. As anticipated, the offset is dominated by the input pair and 364 chips were found between ± 200µV, giving a final yield of 63%.

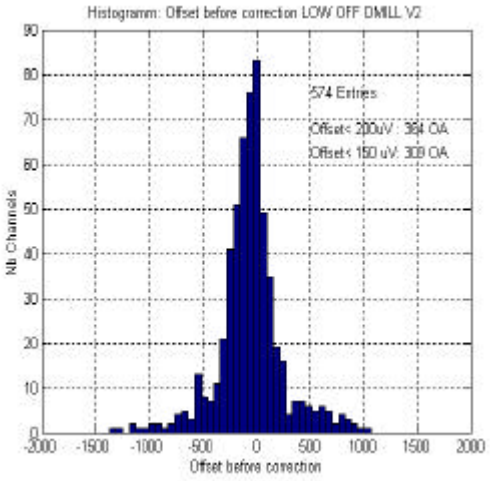

Figure 6: *Offset distribution before trimming*

The offset stability in time has been measured on 10 op amps by monitoring the output DC current along 90 minutes and was found better than 10 µV.

The temperature stability was measured on 10 chips before trimming and was better than 2 µV/°C. Op amps with initial large offset showed the largest variation. 10 op amps previously trimmed down to a few µV have been kept at 87° during 4 days. The stability of the offset has been found better than 2 µV over this period. This measurement also demonstrates the robustness of the fuses.

The sensitivity of the Op amp offset to the DAC input has been studied by measuring the DC current linearity at the PMOS output. The non linearity over each shaper gain is presented in Figure 6: The largest residuals in the high gain range (which covers 0→10 mV), less than 2 µV, can be interpreted as an upper limit of the sensitivity of the op amp offset to the DAC input voltage. The small non linearity of the two other ranges is mainly due to the voltage source itself and the PMOS switch performance.

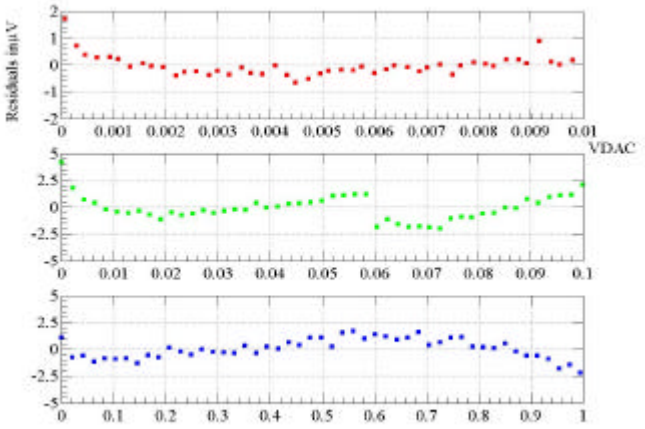

Figure 6: *Residuals of a linear fit on the DC output current over the 3 shaper ranges*

C. Irradiation tests

Concomitantly to the DAC, 10 op amps, not previously trimmed, have been irradiated to photons and neutrons. The offset has remained stable inside 15 µV.

These measurements were detailed at the LEB7 last year and show adequate radiation resistance [4].

D. Production and tests

28000 op amps will be produced before the end of this year. They will be tested and the selected ones trimmed down to a few µV with a robot located in Grenoble [ISN Grenoble].

V. DIGITAL PART

The calibration boards used on module 0 were controlled by an elaborate digital circuitry which allowed to load on board a full calibration sequence (ramping the DAC, changing patterns…)[2]. Although practical and very time efficient this circuitry was based on memories and numerous FPGAs which would not operate reliably in the high radiation environment.

It has thus been decided to simplify the control logic (Figure 7) and load through the SPAC serial bus [5] the run parameters (DAC value, delays, pulsing patterns).

These parameters are decoded from I^2C local bus and stored in registers, which have again been designed in DMILL technology (Calogic chip).

The Calogic chip (Figure 8) covers an area of 16 mm^2 and 39 chips have been received in march 2001, which were all functional.

4 chips have been subsequently tested for SEU at Louvain with 60 MeV protons. No SEE (90 flip flops tested) has been observed up to a fluence of 8.3 10^{12} p^+/cm^2 (8 hours / 30 10^6 I2C accesses).

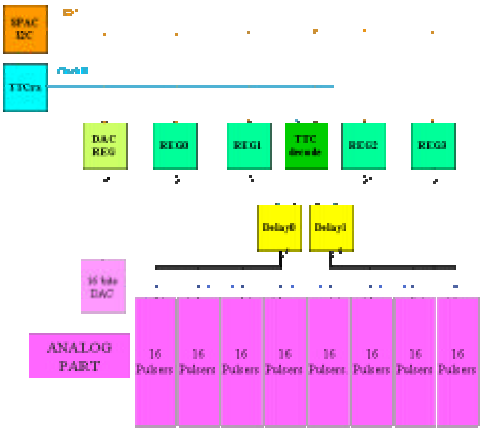

Figure 7: *Schematics diagram of the digital part*

2 delay chips per board are necessary to align in time physics and calibration signals. These chips designed in DMILL technology by CERN [6], contain 4 delay lines that generate delays from 0 to 24 ns, with 1ns step. Their linearity was measured and residuals are within ± 60ps. The jitter is 25 ps.

SEE tests were performed in Louvain on 4 chips. One error occurred and it was cleared by power reset.

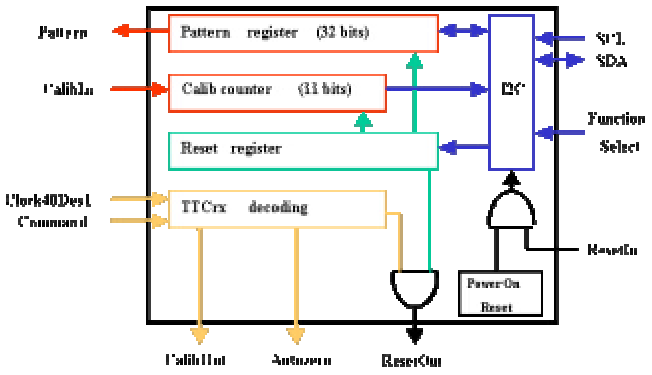

Figure 8: *Schematics diagram of the CALOGIC chip*

VI. EIGHT CHANNEL BOARD

The 8 channel board (Figure 9) has been designed to be 1/16th of the final board. Due to the size of the Op amps package, the layout is very different from the radiation soft board used in module 0 tests. In particular, on the previous board, all the outputs were aligned in a single row, on both sides of the board, with a pitch of 6 mm [2].

The new op amp PQFP44 package exhibits a foot print of 14x14 mm^2 which forces the channels to be staged in the board depth. Consequently, the large command signal (CMD) which fires the pulses can no longer be well separated from the sensitive output signals and results in a ground bounce problem. Most of the problems experienced on the new prototype stem from this new layout and were not seen on the single channel test boards.

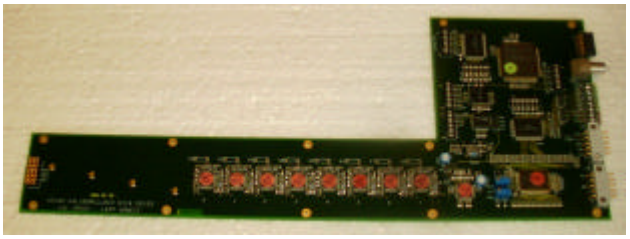

Figure 9: *8 channels prototype picture*

E. Parasitic injected charge

The figure 10 shows the pulse before shaping for a full DAC range.

The rise time is smaller than 2 ns and its variation with the DAC value is very small.

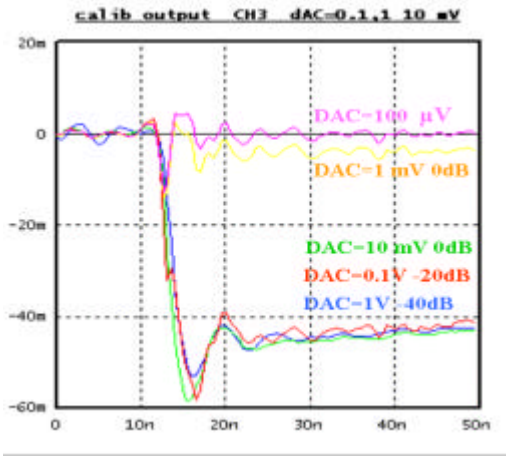

Figure 10: *Pulser output for a full DAC range*

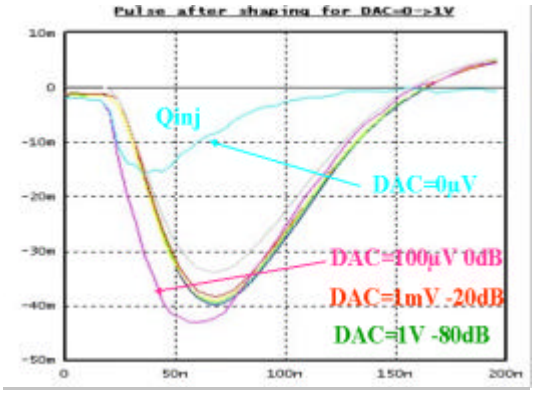

Figure 11: *After CRRC2 shaper (tp=50 ns)*

The undershoot visible on the waveform is a direct consequence of the modifications applied to reduce the ground bounce explained above and solved by moving the switch termination resistor towards the output connector. Consequently, the impedance of the line between the switch output and this termination resistor will have to match 25 Ω instead of 50 Ω.

The HF ringings seen at small DAC values are a residual of the ground bounce and are related to the high frequency switch which is made of a large (10000/0.8 µm) PMOS and an external fast switching NPN (NE 856) bipolar transistor. The small signal obtained when setting DAC=0 (or close to zero) is referred to as "Parasitic Injected Charge" (PIC). This parasitic charge injection is due to the parasitic inductance between the PMOS located inside the op amp package and the external NE856 which makes a resonant circuit with the gate-source capacitance (C_{GS} ~20 pF).

After shaping (Figure 11), the PIC contribution is very small: it is equivalent at its peak to a DAC setting of 30 µV and at the maximum of the signal, to a DAC setting of 15 µV (1 LSB). It is more than a 10 times improvement compared to module 0. Thus the dynamic range of the calibration output pulses is 60000 or 5V/ 75 µV.

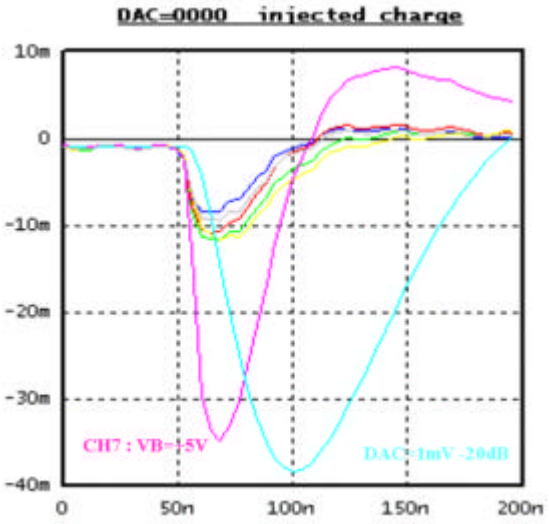

Figure 12: *Parasitic Injected Charge Improvement*

Actually, quite a lot of work was necessary to improve the PIC. For example, a significant improvement (Figure 12) has been obtained in lowering V_{GS} at a given current by reducing the effective threshold voltage V_T through the bulk voltage biasing scheme. It was previously tied to VP6 to minimize body effects (Ch7) and tying it (other channels) in DC to the source reduces V_{GS} from 1.2V to 0.6V typically, bringing a factor of 2 improvement to the PIC .

F. Linearity

DC and dynamic linearity has been measured over the 3 gains of the shaper (Figure 13).

Pulse linearity has been measured after shaping and with a 12 bits ADC sampling the signal at the peak . For the medium and high gains, residuals are within ± 0.05 %.

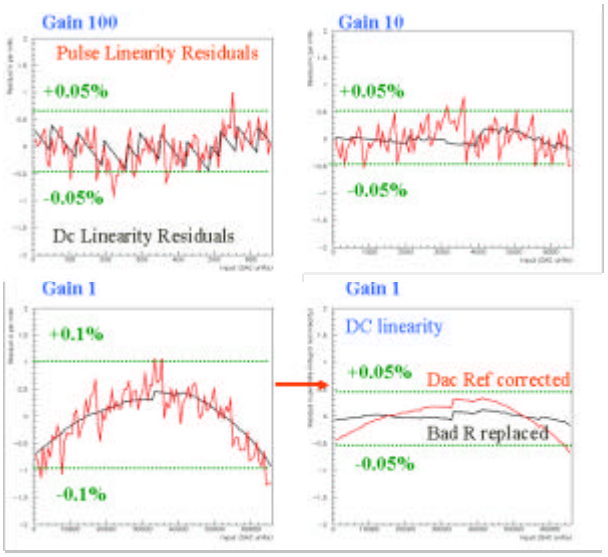

Figure 13: *Residuals of the linear fits of the DC and dynamic linearity over the 3 shaper gains*

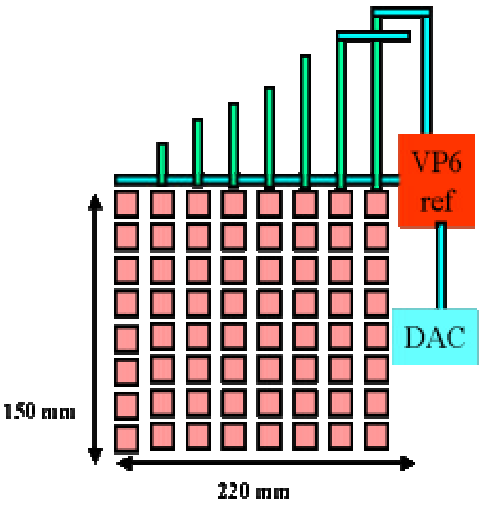

Figure 14: *VP6 star distribution*

For the low gain, *i.e.* for DAC values going up to 1 V and so output DC currents going up to 200 mA, the residuals of both DC and dynamic linearity are within ± 0.1% which is slightly worse than expected. This has been traced to two small imperfections: First the DAC which was referenced to the same VP6 as the current sources decreased slightly when the maximum current was drawn (up to 200 mA per channel). Once this reference corrected, residuals were within ±0.5%. The remaining effect was due to a bad brand of 5 Ω resistors with a too high temperature coefficient leading to a significant change at 200 mA maximum current setting. Using a good resistor brand give residuals within ±0.01 %.

These linearity measurements also show that the dynamic performance is at the level of the DC performance.

VII. FINAL 128 CHANNEL BOARD

The large board is supposed to be a simple replication of the 8 channel module.

However, the correct star distribution of the DAC with respect to the VP6 requires careful attention. In particular, all the lines connecting the 5 Ω resistors to the reference VP6 taken for the DAC should be equalized in resistance and cannot be shared between channels and a DAC variation with the number of enabled channels is to be avoided. 5 layers are necessary to route this VP6 with equalized length (Figure 14).

Many tricky PCB layout details were also necessary to avoid coupling between digital and sensitive analog signals at the level of 100 µV.

VIII. CONCLUSION

The DMILL chips designed for the calibration board exhibit good performance and fulfill the calorimeter requirements. Their design is now final and they are ready for production.

2 prototypes of 128 channels calibration boards using these chips will be available next October. The call for tenders for the production of 130 boards for ATLAS will be done in 2003.

IX. REFERENCES

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