A low-power high dynamic range front-end ASIC for imaging calorimeters

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Abstract

High granularity calorimeters with shower imaging capabilities require dedicated front-end electronics. The *ICON_4CH* and *VA4_PMT* chip-set is suitable for very high dynamic range systems with strict noise requirements.

The *ICON-4CH* is a 4 channel input, 12 channel output ASIC designed for use in a multi-anode photomultiplier system with very large dynamic range and low-noise requirements. Each of the four input signals to the ASIC is split equally into three branches by a current conveyor. Each of the three branches is scaled differently: 1:1, 1:8 and 1:80.

The signal is read out by a 12 channel low noise / low power high dynamic range charge sensitive preamplifier-shaper circuit (*VA4-PMT* chip), with simultaneous sample-and-hold, multiplexed analog read-out, calibration facilities. Tests performed in our lab with a PMT are reported in terms of linearity, dynamic range and cross-talk of the system.

I. INTRODUCTION

Imaging calorimetry takes advantage of the fine granularity of the detector to allow for the reconstruction of the lateral and longitudinal development of electromagnetic and hadronic showers. This feature is a powerful tool to achieve good electron / hadron discrimination. An important requirement for an imaging calorimeter, designed for very high energy measurements, is the dynamic range of the front-end electronics.

In this paper, we focus on a particular implementation of imaging calorimeters with multi-anode photomultipliers (MAPMTs) read-out. Given the high gain of the photodetector at operating conditions, the front-end electronics has to deal with integrated charge values ranging from a few tens of fC (for minimum ionizing particles) to several hundreds of pC (for high energy showers). Our group developed a prototype of front-end electronics where the very large dynamic range was split in three contiguous sub-ranges, at the expense of multiplying by three the total number of read-out channels. This concept was first implemented in a functional unit, consisting of a two-chip structure, and later integrated into a specifically designed hybrid board, as described in the following.

II. FUNCTIONAL PRINCIPLES

A hybrid board (see photo in fig.1) which houses 12 chip-sets was developed by Ideas ASA (Norway) as a joint project with the University of Siena and INFN. Each chip-set consists of two chips (known as *ICON_4CH* and *VA4_PMT* respectively) and has the capability to read-out four anodes of a MAPMT. The hybrid is also designed for housing TA-chips (based on the TA32CG architecture, Ideas ASA, Norway) to give trigger capability to the system.

Figure 1: Hybrid which houses 12 chipsets consisting of two chips (known as *ICON_4CH* and *VA4_PMT* respectively)

The *ICON* chip works as a current conveyor for the pulses coming from the PMT's. Each input signal is split into three equal signals with a current conveyer, and each of the branches mirrors the input signal with different scaling (one branch with 1/1, one with 1/8 and one with 1/80 ratio). In this manner, each of the four input signals is split in three, with different dynamic range, each having its own output pad. Therefore, the number of outputs from the ICON is 12.

The outputs from the *ICON* are AC-coupled to the 12 *VA4_PMT* inputs. This is a chip of the VA family modified in the front-end section while the calibration and read-out functionalities are the standard ones. Instead of the usual shift_in / shift_out daisy-chain, there is one *shift_in_b* which goes into all VA chips and one separate clock to each one. However, the hybrid has been designed so that it is possible to use the shift_in /shift_out daisy chain can still be used instead.

The principle of the two-chip structure is summarized in figure 2, which shows one channel of the current conveyor and its three corresponding channels in the VA chip; the large external capacitors (tipical value ~ 1nF) used for AC-coupling are shown in the middle.

ICON_4CH input signals is split equally into 3 differently scaled branches by a current conveyer. The output stage consists of a current source and an on-chip resistor (10 KΩ). Since the output DC voltage level of the ICON is not compatible with the input bias voltage of the VA, the two chips are AC-coupled by means of an external capacitor; so the signal can be read-out by a VA-chip, e.g. the *VA4_PMT*.

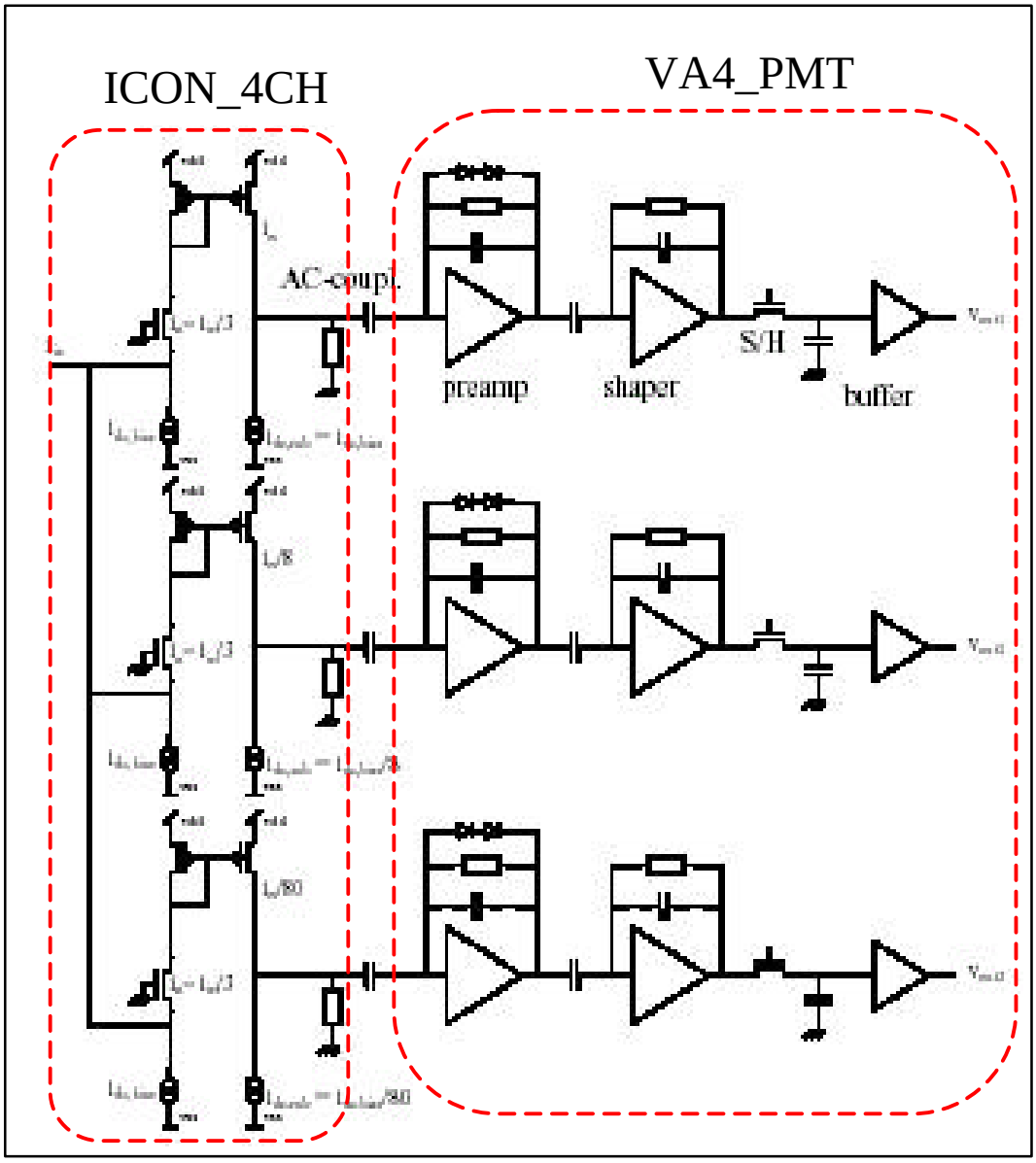

Figure 2: Principle of the two-chip structure

The read-out system consists of a board with standard VME interface. The hybrid is implemented as a piggyback board placed on top of the VME-board by means of 100mil pitch double-row header connectors.

A. *ICON_4CH description*

The *ICON_4CH* (see fig.3 for chip layout) is a 4-channel-input, 12-channel-output ASIC designed for a system with very high dynamic range (up to 10^5) and low-noise demands. In order to achieve both requirements, each of the four

B. *VA4_PMT description*

The *VA4_PMT* (see fig.4 for its layout) is a 12 channel low noise/ low power high dynamic range charge sensitive preamplifier-shaper circuit, with simultaneous sample-and-hold, multiplexed analog readout, calibration facilities. The ASIC also features programmable gain in the preamplifiers, giving adjustable DNR/noise performance. It has been derived by a standard VA eliminating the front-end saturation effects, giving an excellent cross-talk performance.

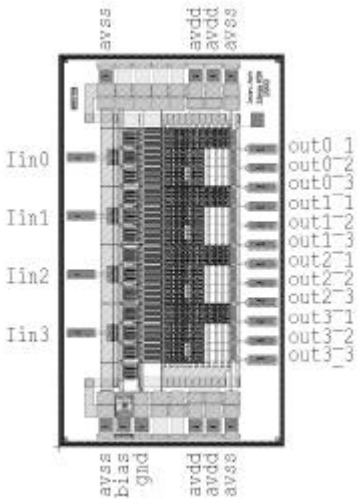

Figure 3: *ICON_4CH* chip layout

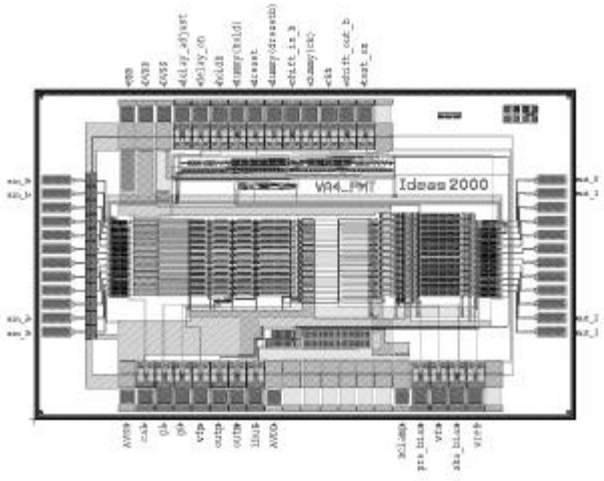

Figure 4: *VA4_PMT* chip layout

III. HYBRID FEATURES

The ASIC design was driven by its possible use in experiments with Sci-Fi calorimeters for energy measurements up to the TeV scale (as, for instance, AMS-02 [3], CALET [4]) or the multi-TeV scale (e.g.: CREAM [5]). Balloon-borne or space-based experiments impose strict requirements on low power consumption, while rad-hardness is a minor issue (order 10 krad dose) compared to LHC experiments.

The main features of the hybrid are:

- LOW POWER: each chip-set has about 38 mW power consumption and this means about 450mW for the hybrid;
- HIGH DYNAMIC RANGE: the ASIC features a 10^5 dynamic range;
- MINIMAL CROSS-TALK: 0.1% up to 100 pC input charge values, 0.1-0.3% above;
- BOARD-PMT DISTANCE: the hybrid is connected to the PMT anodes through standard 50 ohm coaxial cables: in this way the electronics crates can be located far away from the PMT;
- FAULT TOLERANCE: chip control lines are separated and a daisy-chain has been avoided;
- POSSIBLE ADDITIONAL FEATURES: to give trigger capability to the system, a modified TA chip (from TA32CG architecture) has been specified to:
  - provide an analog output signal proportional to the number of input channels above a programmable threshold;
  - provide an analog output signal proportional to the sum of 4 analog inputs (they can be chosen among the available 12 channels from the Icon chip when the die is mounted on the hybrid: this allows additional flexibility in the choice of the dynamic sub-range to be used for triggering purposes).

IV. LAB TESTS

A. Measurement setup

To test the hybrid board, we used an experimental setup that could be tuned to provide input signals similar to those generated by a scintillator based detector (e.g.: Sci-Fi calorimeter, scintillator hodoscope, …).

We used a pulse generator to produce a trigger signal to the board. Using the same signal, we flashed a LED coupled to a PMT (both enclosed in a light-tight box). The output of the PMT was used as an input for the hybrid board.

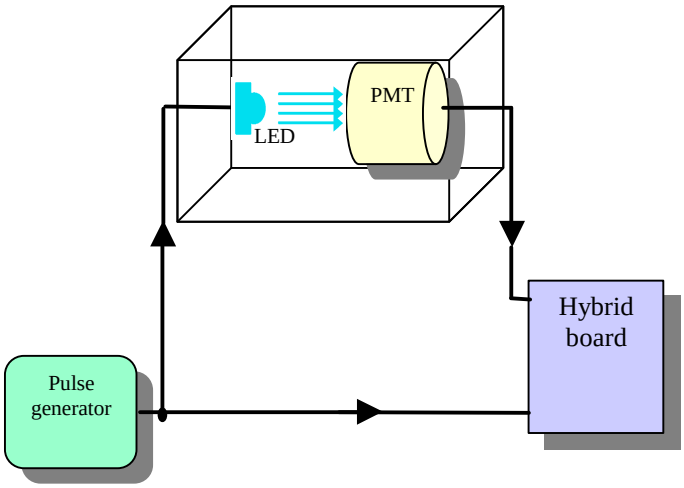

Figure 5: Measurement setup

B. Test results

Tests performed in our laboratory with a multi-anode photomultiplier R7600-00-M4 showed linear behavior for

input charge values up to 8000 pC, rms noise under 50 fC and cross-talk under 4 per mill.

Figures 6 to 8 show test results for chip linearity:

- channel 0 (gain G =1) output has a linear behaviour for input charge values up to about 80 pC,
- channel 1 (G = 1/8) up to about 700 pC,
- channel 2 (G = 1/80) up to 8000 pC.

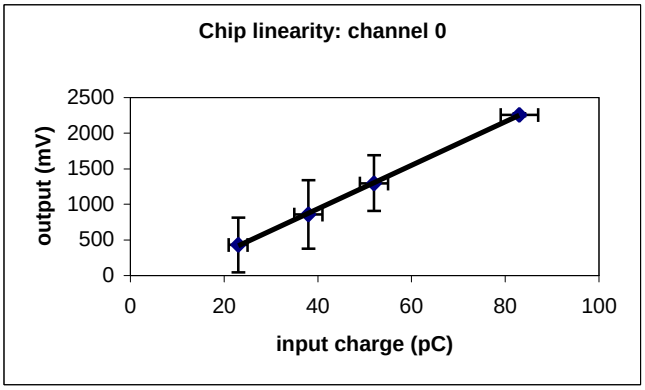

Figure 6: Channel 0 (G =1) linearity

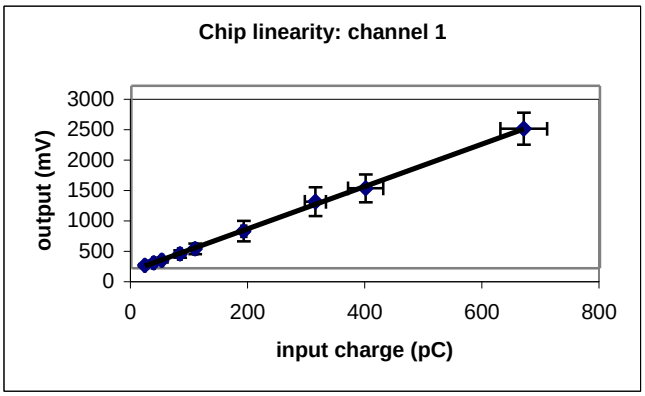

Figure 7: Channel 1 (G = 1/8) linearity

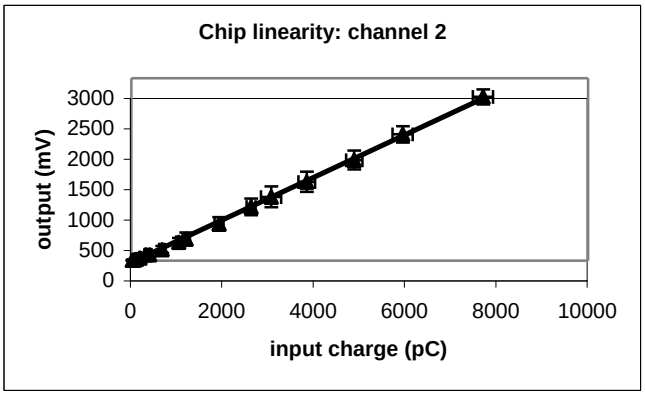

Figure 8: Channel 2 (G = 1/80) linearity

Measured gains for each channel are reported in table 1. Ratios between measured gains of different channels are in agreement with the expected ones.

Table 1: Measured gains

Channel	Expected gain ratio	Measured gain (mV/pC)	Measured gain ratio
0	1 : 1	30	1
1	1 : 8	3.5	0.12
2	1 : 80	0.35	0.012

Figure 9 shows the test result for cross-talk measurements: cross-talk becomes significant with respect to the rms noise for input charge values above 100 pC; for input charge values above 1000 pC, the cross-talk reaches a plateau at 4 pC approximately.

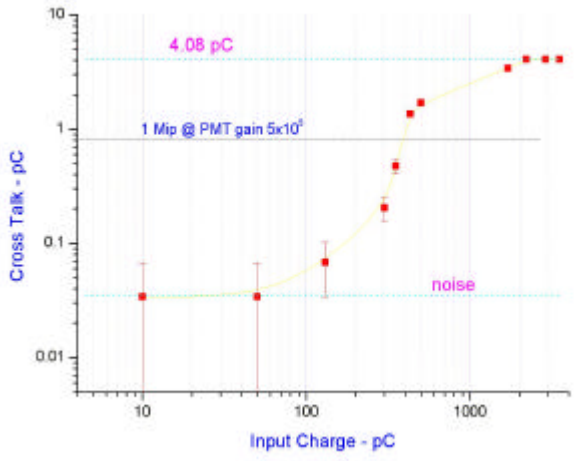

Figure 9: Cross-talk between channels

V. CONCLUSIONS

Calorimeters designed to operate at very high energy require dedicated front-end electronics with a very large dynamic range. Our group developed an ASIC where this dynamic range is split in three contiguous sub-ranges, at the expense of multiplying by three the total number of read-out channels. Tests performed in our laboratory showed linear behavior for input charge up to 8000 pC, rms noise under 50 fC and cross-talk under 4 per mill.

References

[1] Ideas ASA, Norway – *ICON_4CH* and *VA4_PMT* documentation .

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