Front-end Electronics for the LHCb preshower.

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Abstract

The LHCb preshower detector (PS) is both used to reject the high background of charged pions (part of L0 trigger) and to measure particle energy (part of the electromagnetic calorimeter).

The digital part of the 40 MHz fully synchronous solution developed for the LHCb preshower detector front-end electronics is described including digitisation. The general design and the main features of the front-end board are recalled. Emphasis is put on the trigger and data processing functionalities. The PS front-end board handles 64 channels. The raw data dynamic range corresponds to 10 bits, coding energy from 0.1 MIP (1 ADC count) to 100 MIPs while the trigger threshold is set around 5 MIPs.

I. The Preshower

A. The detector

The preshower is located immediately upstream from the electromagnetic calorimeter (ECAL), with one-to-one correspondence between ECAL towers and preshower cells. It is made of a 12 mm thick lead ($2\ X_0$) followed by a detection plane of 15 mm thick scintillator pads. A description can be found in reference [1]. Around 6000 cells constitute this plane, it is subdivided into inner, middle and outer sections with approximatively 4*4, 6*6 and 12*12 cm^2 cell dimensions. The scintillation light is collected with helicoidal wavelength shifting fluorescent fibre held in a groove in the scintillator. The both fibre ends are connected to long clear fibres which send the light to photomultiplier tubes (MAPMT) with 64 channels that are located above or below the detector. The main characteristics of the light at the output of a phototube are described in reference [2] as well as the preshower requested performances. On average, about 25 photoelectrons in response to a minimum ionising particle (MIP) are provided and about 85% of the charge is obtained in 25 ns.

The deposited energy in the preshower is measured. First, the comparison to a threshold allows to produce, every 25 ns, a Yes/No signal for the L0 calorimeter trigger system. Second, this energy is used to correct the energy measurements in ECAL. For that PS signals require digitisation over 10 bits.

It has therefore been decided to sub-divide the front-end electronics in two parts. The "very front-end", part described in reference [3], is placed the closest possible to the MAPMT, on its back, and it compensates the gain variation of the 64 channels by load resistances at the entrance of the amplifier which will be adjusted between 50 Ω and 200 Ω. It comprises amplification, integration and holding of the signal.

B. Raw signal

The raw signal at the MAPMT output does not have a constant shape due to statistical fluctuations of energy deposit and to the characteristics of electrons emission. In addition the output pulse spreads over more than one bunch period of 25 ns. In case of successive collisions the generated pulses are piling up. Statistical studies of the signal shape (test beam at CERN) show that the pile-up can be corrected considering only two 25 ns periods according to the required precision. A factor, α, denotes the ratio between the integral of the signal within the second 25 ns period over the integral within the first period.

As there are very large fluctuations in the signal pulse shape, it is important to integrate the signal over a time as long as possible within the 25 ns limitation.

C. Very front-end electronics

This is performed by alternating two integrators and reseting one integrator when the other is active. It allows a continuous integration of the signal on 25 ns periods without deadtime. Then the signal is sampled by track-and-hold circuits and the output of the active integrator is chosen by a multiplexor.

A dedicated ASIC has been designed for this purpose with a 10-bit dynamic range. All circuits elements are functioning in differential mode to improve stability and pickup-noise rejection. 8 channels per chip are implemented, so a board contains 8 chips.

The analog signal is then sent with twisted-pair cables, between 10 and 20 meter length according to their location, to the front-end board located in racks above the detector. In this board, the signal is digitised with a 10-bit ADC and stored in a FIFO pipeline until level 0 and level 1 trigger decision.

II. Front-end Electronics

The PS front-end board handles 64 channels. It receives the analog signals coming from the PS very-front-end board and 64 bits, one per channel, coming from the

scintillator pad detector (SPD). SPD is made of a detection plane of scintillator pads placed just before the PS lead. It has the same granularity and structure than PS and allows to identify charged particles for L0 calorimeter trigger. It provides one bit per cell, coming from a sample discriminator telling whether a cell has been hit.

The front-end part of the preshower electronic system has the following functionalities :

- A synchronization signal is provided to the very front-end electronics;
- The analog signals from the very front-end chips are digitized and processed in order to produce the preshower data;
- The preshower trigger data are computed;
- The SPD data are collected;
- It receives at 40 MHz, from ECAL cards, the address of the ECAL candidates;
- The neighbourhood of each cell is searched through all preshower and SPD data;
- Preshower and SPD data are sent synchronously to the ECAL validation boards for trigger purpose;
- The needed data are stored waiting for L0 and L1 trigger signals (DAQ).

Each process implemented on the front-end board is done without any dead time with a pipe-line architecture (fully synchronously).

A. Mixed electronics part

The very front-end chip output signal has always the same sign. Its amplitude reaches 2 volt in differential mode , with a common mode voltage of -0.6 volt. 20 m long cables link very front-end and front-end boards. A both end cable adaptation with pole zero correction is used to allow the use of simple, cheap Ethernet cable up to 20 meters without reflection. The signal amplitude is divided by a factor 2 due to the cable adaptation.

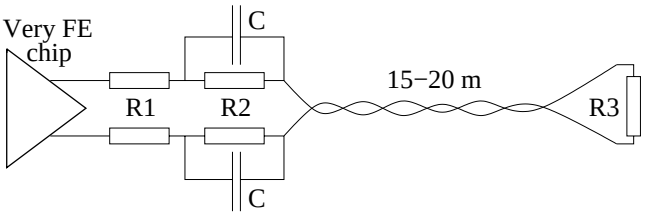

Figure 1: Cable adaptation

For the digitisation we plan to use the AD9203 ADC from Analog Devices: this ADC has differential inputs, a small package and is low power (3.3 V, 78 mW). Its inputs are bipolar with a common mode voltage of +0.5 volt and a dynamic range from –0.5 to 0.5 V.

The AD8138 (or a new cheaper version AD8132), which is a differential input and output Op. Amp. with a separate common mode feedback is then used to adapt the signal specifications from the very front-end chip and the cable to the AD9203 ADC inputs characteristics.

As shown on figure 2 a balanced differential offset is used to shift the dynamic range of the input signal from 1 volt to ±0.5 volt, and the common mode feedback loop used to fix the common mode voltage at the AD9203 reference value (+0.5 V), as proposed by the analog device application note.

A differential anti-aliasing filter connects the Op. Amp. and the ADC. It is based on a simple basic RC network. The cut off frequency is about 40 MHz. The filter mainly aims to limit the noise instead of avoiding aliasing phenomenon (the very-front end signal is held when digitized).

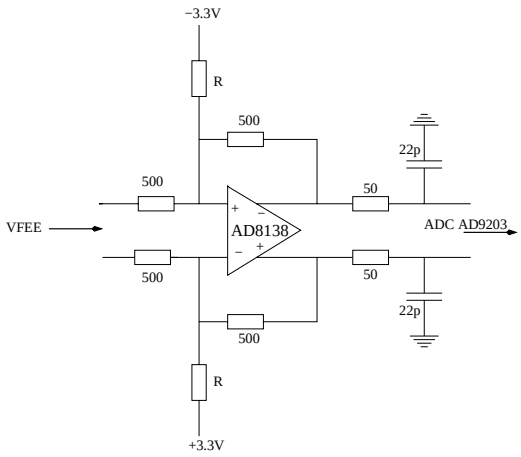

Figure 2: Signal adaptation with AD8138

The ADC has been carefully tested, to be sure that it was possible to use it with an unipolar signal shifted by a constant offset without extra noise.

The ADC clock needs a little more care, due to the fact that it is no differential TTL level. As we do not plan to carry TTL 40 MHz clock on the 64 channel board, we decide to carry it with LVDS levels and to convert it channel by channel as near as possible of the ADC's. In addition we take care to reduce the size of a full channel to avoid the risk of clock digital noise.

As the planned format for the front-end board is a 9U size, using both sides, only 1 cm in height is allowed for 1 channel. Thus, the components have to be placed in a compact way without debasing the noise immunity and cross-talk between adjacent channels.

B. Data processing part

Since the very front-end chip is made of two half channels, the corrections for each half channel are necessary. Thus one front-end board manage 128 half channels.

First of all, the pedestal scattering has to be compensated. It is predominantly due to the offset variation between very front-end channels and half-channels. To ensure that the pedestal has always the same sign, an additional differential offset is applied (about 50 mV) at the input of the Op. Amp. (resistive bridge).

Then a gain correction is applied.

Then previous sample residue multiplied by the factor α is subtracted to the current data.

Finally the corrected 10 bits data are coded into a 8 bits floating format to decrease the amount of bits sent to the DAQ system. The coding process does not degrade the overall precision along the dynamic.

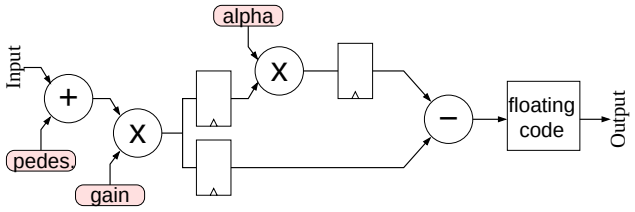

Figure 3: Data processing scheme

C. *Trigger part*

The preshower trigger data are computed from data by a single comparison with a threshold to determine if the signal corresponds to an electromagnetic candidate (electron or photon). This threshold value will be typically around of 5 MIPs, i.e. 50 ADC count. This is the main trigger function of the front end-board.

In addition, the preshower front-end electronics produces some data destined for the ECAL trigger process.

64 SPD data bits are received from the SPD front-end boards (same detector cells granularity), they have a similar meaning than the preshower trigger data. The front-end board has to count the number of active bits (SPD multiplicity). A 7 bit number from 0 to 64 is issued and sent to the ECAL trigger processor with a bunch identifier.

The ECAL trigger needs preshower and SPD trigger information [6]. To avoid the transmission of 64 trigger data bits between one preshower half front-end board and one ECAL front-end board, only the strictly necessary data are sent.

For each local maximum, in a 4*8 ECAL cells block, the ECAL trigger system sends an address to the preshower front-end (5 bits for the local maximum address and 4 BCID bits). Then the front-end board transmits the neighbourhood of the corresponding preshower cell to the validation board. The BCID is added to allow the ECAL trigger system to cross-check time consistency.

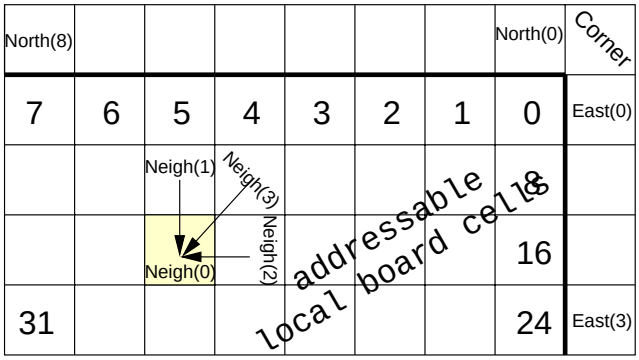

Figure 4: neighbours search algorithm

What is called "neighbourhood" is the trigger information corresponding to the addressed cell, its northern neighbouring cell, its eastern neighbour and its north-eastern neighbouring cell. When a bordering cell is addressed, one may need information from another front-end board. That's why front end boards are linked together and transmit each others the useful data in a synchronous way. A synchronisation process compensates the various latency according to the data source before the neighbour search process starts.

As the ECAL trigger electronics is organized in 32 channel board, each 64 channels PS Front-end board is seen by the trigger system as two 32 channels half boards, each receiving its own request address. The address commands selection inputs of multiplexors that fetch and output the neighbours.

III. PROTOTYPES

A. *Mixed part optimisation*

A preliminary prototype of the mixed electronic part (Op. Amp. and ADC) was designed in order to validate the choice of the components. The components of this first prototype was poorly placed and routed since the front-end board constraints were not established at the time of the design. The preliminary version lead us to evaluate, in the worst case conditions, the intrinsic noise of the circuitry. The way to design the differential offset part and the anti-aliasing filter was determined according to its influence on the noise.

Despite the lack of maturity of the design the noise measurements were acceptable: the maximum noise reached a value of 0.8 mV along the dynamic that is to say less than one quatization step (1 LSB is 1 mV).

In a second iteration, a final version was designed tacking into account the front-end board spacing constraints and some EMC specifications. All the components of the design are placed into a 1 cm by 4 cm rectangle area that allows the 64 channels to be fitted in the board.

The following layout arrangements were done :

- A ground plane is covering all the surface filled by the components ;
- The decoupling capacitors are placed as close as possible of the power pins ;
- A local carried upward ground plane is added under the ADC in order to avoid the numerical signals influence on the analog part ;
- The ADC reference voltage wire is routed near static power tracks and maintaining a sufficient distance from disrupting dynamic signals ;
- The small size of the layout avoids line effects to be bothering ;

- The clock is converted from LVDS electrical levels to TTL levels as close as possible of the ADC.

Due to these precautions the noise effects have been reduced to a comfortable range of 0.4 mV along the dynamic. The good results lead us to create a hierarchical library element for the PCB layout to ensure that every channel would be identical.

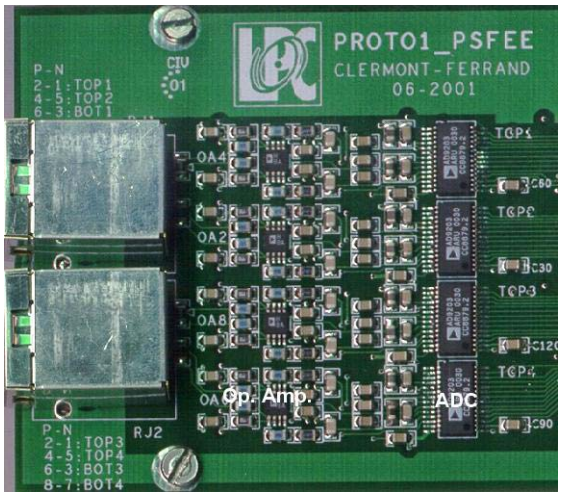

Figure 5: 8 channels hierarchical block (double side)

Finally a 8 channels prototype was designed to test the crosstalk. No significant crosstalk effects were measured.

B. Digital process prototype

An additional prototype aims, on the one hand, at validating the functional behaviour of the processing algorithm and on the other hand, at providing a simple data acquisition protocol to be used during test beam or at laboratory (automated tests, photomultiplier test bench, etc.).

A 16 channels (at 40 MHz) board was designed using the mixed part hierarchical element described before. The processing algorithm for 8 half-channels is fitted into one FPGA. It includes neither TTC functions nor ECS interface and is not foreseen to take into account radiation hardness constraints.

The board is driven by a computer through a VME bus. The computer runs under a Linux operating system. The software is written in C++ language (a LabView version also exists and is used for debugging purpose). An additional FPGA interfaces the VME bus and an internal bus connecting every FPGA on the board.

The internal bus is made up of one 40 bits data bus, one 10 bits address bus and one 8 bits control bus. Thus one can acquires the 10 bits raw data for 4 channels (1 FPGA). Due to the FPGA technology several kind of algorithm can be programmed according to the use of the board (algorithm tests, test beam, photomultiplier test bench).

The algorithm tested at laboratory is given by figure 3. In order to take into account the half-channel structure of the very front-end chip both the pedestal and the gain register are doubled. They are flipped each clock cycle.

In addition to the data processing algorithm each data processing FPGA includes 4 very simple DAQ channel using internal memory blocks. A DAQ channel is formed by an adjustable length L0 pipe-line (up to 256 words) followed by a dual-port RAM accessible through the internal bus. The selected events are stored into the RAM when a positive L0 trigger occurs. Many additional features are provided: programmable delay on the trigger signal, maximum number of event to acquire, etc.

In particular a temporal mode allows a programmable length sequence of successive events to be stored in case of trigger. The position of the trigger along the sequence can be set. This mode is very useful to give an access to the successive values of the 25 ns period integrals of the pulse caused by a particle.

Up to 1024 8 bits data words can be acquired per run. It takes about 0.1 s to download the whole board to the PC (limitation due to the PCI-VME interface speed). Hence the board is fully compatible with test beam data acquisition constraints.

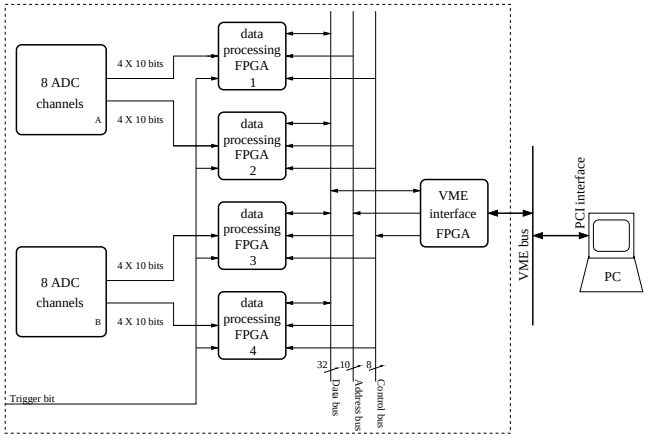

Figure 6: Prototype architecture

To meet radiation tolerance constraints (10 krad over 10 years) we tried to synthesizes the data processing algorithm into an ACTEL 54SX technology. A maximum of 2 channels can be fitted in a 54SX32 chip. It includes triple voting structures for configuration registers. The estimated working frequency is about 60 MHz after place and route step.

Another prototype dedicated to the trigger algorithm was designed. It has being tested successfully.

C. ASIC prototype

In order to estimate the cost and the feasibility of an ASIC solution a 4 channels circuit has been designed. It includes a parameters downloading serial interface with parity check and triple voting (configuration registers) for radiation tolerance. The total number of configuration bits is 220. Configuration data can be loaded without disrupting the data processing.

The chosen technology is AMS 0.35 µm (CMOS). It realizes a good compromise between cost and performance. The prototyping cost is also reduced due to CMP multi-project fabrication runs.

The die size, including 88 input/output pads and the core, is 3 by 3 mm^2. With the package (CQFP100), the total surface use including the package is 2 by 2 cm^2. The working frequency reaches 250 MHz. Hence less pipe-line steps can be used therefore reducing the latency.

IV. CONCLUSION

The preshower mixed electronics part and the digital data processing algorithms are validated thanks to prototypes boards.

A technological study leads us to compare classical FPGA, ACTEL and ASIC based solutions. While classical FPGA does not fulfil the radiation hardness requirement, the ASIC version is better than ACTEL in term of occupied PCB surface, working frequency, latency and cost (see table 1).

Even if engineering, production and testing time could be rather uncertain the ASIC solution appears as the most relevant according to the cost and PCB usable space (32 cm for 64 channels) due to the smaller QFP100 package (QFP208 for FPGA).

Table 1: Technologies comparison

Technology	Number of channels	Cost per channel
Altera ACEX	4 (max 6)	10 EUR
ACTEL 54SX32	2	18 EUR
AMS 0.35 µm	4	12 EUR

AMS technology cost includes 30% of spare chips (the total number of chips is 2000). FPGA costs are for 1000 chips.

V. REFERENCES

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