# The Design of the Coincidence Matrix ASIC of the ATLAS Barrel Level-1 Muon Trigger

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*Abstract*

The ATLAS level-1 muon trigger in the barrel region identifies candidate muon tracks within a programmable transverse momentum range. A system of seven Resistive Plate Chamber detector concentric layers provides the hit information in the bending and non-bending projection. A coincidence of hit in the detector layers within a programmable road is required to generate a trigger signal. The width of the track road in the detector is used to select the transverse momentum cut to be applied.

The Coincidence Matrix ASIC provides the core logic of the trigger on-detector electronics. Both the trigger algorithm and the detector readout logic are implemented in this chip. Each CMA is able to process 192 RPC signals coming from up to four different detector layers. Most of the CMA logic works at an internal frequency of 320 MHz.

The design and the tested performance of the ASIC are presented.

## I. The ATLAS Barrel Level-1 Muon Trigger

The ATLAS muon spectrometer in the barrel, which covers a pseudorapidity region equal to $|\eta| < 1.05$, makes use of the Multi Drift Tube detectors for particle track precise measurement, and the Resistive Plate Chamber detectors for triggering.

The barrel first level muon trigger has to process the full granularity data (about 350.000 channels) of the trigger chambers [1]. The latency time is fixed and less then 2.5 μs. The maximum data output frequency to the higher-level triggers is 100 kHz.

Level-1 trigger main functions are:

- identification of the bunch crossing corresponding to the event of interest;
- discrimination of the muon transverse momentum $p_T$;
- fast and coarse muon tracking, used for higher-level trigger processors;
- second coordinate measurement in the non-bending projection with a resolution of ~1 cm.

The level-1 trigger is able to operate with two different transverse momentum selections, providing a low-$p_T$ trigger ($p_T$ ~ 5.5 GeV), and a high-$p_T$ trigger ($p_T$ ~ 20 GeV). To reduce the rate of accidental triggers, due to the low energy background particles in the ATLAS cavern, the algorithm is performed in both η and ϕ, for both low-$p_T$ and high-$p_T$ triggers. Barrel precision MDT chambers can only measure the bending coordinate, thus the ϕ projection is used to give to the experiment the non-bending muon coordinate with a resolution of ~1 cm. The measured non-bending coordinate is used in addition with the data coming from MDT detectors for precise particle track reconstruction.

A section view of the trigger system is represented in Figure 1, showing where the three RPC stations are located inside the ATLAS Muon Spectrometer. The ATLAS muon trigger system is composed by three RPC stations. The RPC detectors are mounted on the MDT chambers.

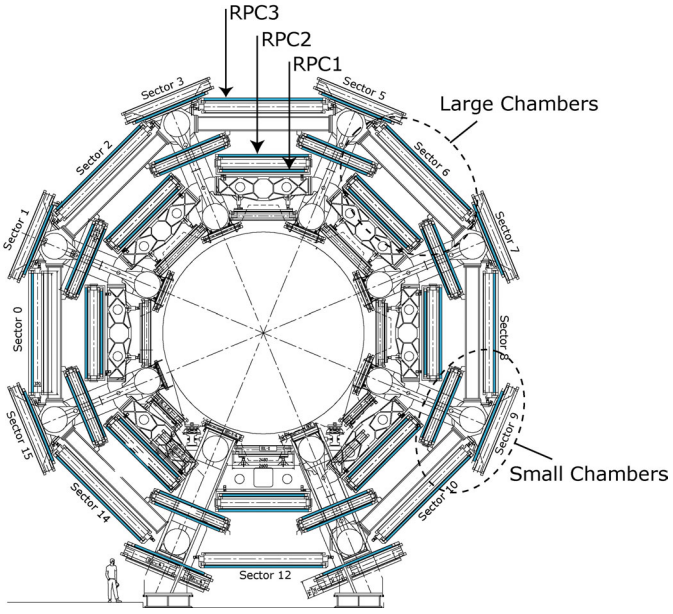


Figure 1: The ATLAS Muon Spectrometer Layout

Each RPC chamber is readout by two planes of orthogonal strips. The η strips give the bending projection, while the ϕ strips give the non-bending one.

Muon $p_T$ selection is performed by a fast coincidence between strips of different RPC planes. The number of planes in the whole trigger system has been chosen in order to minimise accidental coincidences and to optimise efficiency. For accidental counting reduction, the trigger operates in both bending and non-bending projection.

Figure 2 shows the trigger scheme. The low-$p_T$ algorithm makes use of information generated from the two Barrel Middle stations RPC1 and RPC2. The first stage of the algorithm is performed separately and independently in the two η and ϕ projections. If a track hit is generated in the RPC2 doublet (pivot plane), a search for the same track is made in the RPC1 doublet, within a window whose centre is defined by an infinite momentum track coming from the

interaction point. The width of the window is programmable and selects the desired cut on $p_T$ (the smaller the window, the higher the cut on $p_T$). Three programmable $p_T$ thresholds in each projection can be applied simultaneously. To cope with the background from low energy particles in the cavern, a majority coincidence of the four hits of the two doublets in each projection is required.

The high-$p_T$ algorithm makes use of the result of the low-$p_T$ trigger system and the hits available in the RPC3 station. A coincidence between the 1/2 majority of the RPC3 doublet and the low-$p_T$ trigger pattern is required.

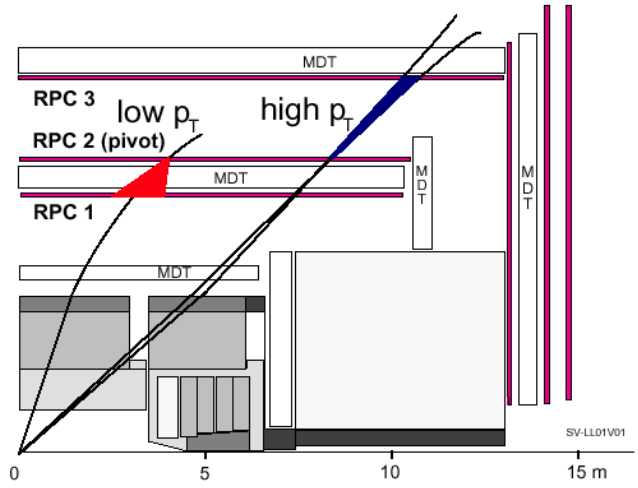


Figure 2: The ATLAS Barrel Level-1 Muon Trigger

Figure 3 shows the trigger slice scheme. Front-end signals coming from RPC2 pivot and RPC1 detectors first go to the splitter boards, which are used for splitting signals going to more than one CMA. Four CMAs are hosted in one PAD board, in which data coming from the ASICs are collected from the PAD logic chip, which formats outputs the low $p_T$ trigger algorithm data. RPC3 outer detector signals and data coming from the low $p_T$ board are sent to the high $p_T$ PAD board, hosting four CMAs, which performs the high $p_T$ trigger algorithm and sends results data off-detector via an optical transmitter.

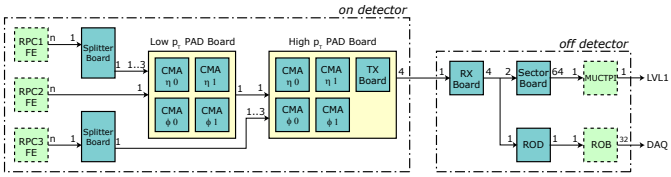


Figure 3: The ATLAS Barrel Level1 Muon Trigger slice scheme

## II. Coincidence Matrix ASIC

The CMA is the core of the barrel level-1 muon trigger logic, its main functions are:

- incoming RPC front-end signals timing alignment and digital shaping;
- input and output signal masking;
- de-clustering and majority logic algorithm execution;
- execution of the trigger algorithm, local muon track candidates identification and $p_T$ classification;
- RPC hit time measurement with 3.125 LSB (1/8 of the Bunch Crossing period);
- readout data storing during level-1 latency;
- readout data formatting and serial transmitting.

### A. CMA functionality

The CMA can be programmed to perform either the low-$p_T$ or the high-$p_T$ trigger algorithm. The chip can be used as a η CMA, covering a region $\Delta\eta\times\Delta\phi \sim 0.2\times0.1$, or as a ϕ CMA, covering a region of $\Delta\eta\times\Delta\phi \sim 0.1\times0.2$.

The chip has 2×32 + 2×64 inputs for the front-end signals [2]. In the low-$p_T$ CMAs the 2×32 inputs are connected to the front-end signals, either η strips or ϕ strips, coming from a doublet of the RPC2 pivot plane, while the 2×64 inputs are connected to the signals coming from the RPC1 doublet. For the high-$p_T$ CMAs the first 32 inputs are connected to the output trigger signals coming from the low-$p_T$ PAD board, the second 32 inputs are not used, while the 2×64 inputs are connected to the signals coming from the RPC3 doublet.

The CMA aligns in time the input signals in step of one-eight of a bunch crossing period. For this reason the chip internal working frequency is 320 MHz, eight times the 40 MHz bunch crossing frequency. Input signals can be masked to the zero logic in order to be able to suppress noisy channels and to handle unconnected input signals [3].

RPC average cluster size is ~1.4, hence input signals are pre-processed and de-clustered in order to sharpen the $p_T$ cut. The maximum cluster size to be processed in the de-clustering logic is programmable.

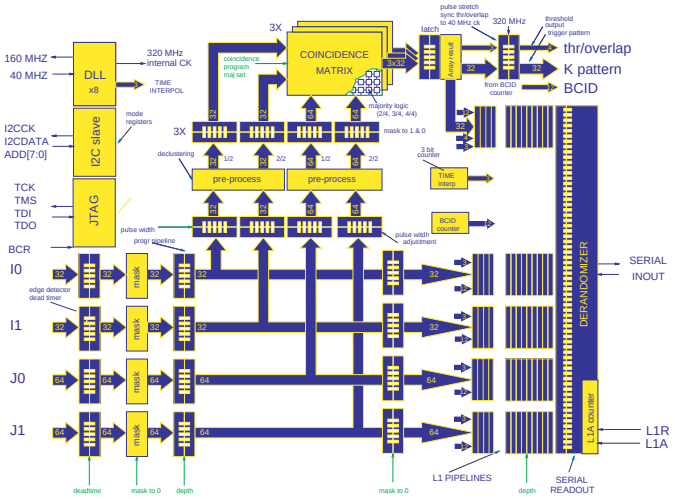


Figure 4: CMA block scheme

Processed input signals are sent to the coincidence logic, which performs the coincidence algorithm. The logic is repeated three times, so that three different coincidence windows can be simultaneously applied inside the chip. The three coincidence windows can be independently programmed, thus providing three different muon $p_T$ cuts. Coincidence logic inputs can be masked to "one" logic, to

simulate unconnected inputs. A programmable majority logic can be applied to the coincidence algorithm, choosing a 1/4, 2/4, 3/4 or 4/4 plane confirmation. The 32-bit trigger output pattern is then sent to the chip outputs.

The CMA readout logic collects chip input data and trigger output data in a latency memory, used to store events during level-1 latency period. Data corresponding to one event are accepted according to the Level-1 Accept signal arrival time and to the programmed acceptance window time. All other hits are discarded, while level-1 validated data are formatted and sent to de-randomising buffers for the serial readout.

### *B. CMA radiation environment*

Table 1 shows the simulated radiation levels [4] for the RPC stations in the barrel region. The RPC electronics will be mounted on the Barrel Middle (BM) and Barrel Outer (BO) stations. The table show the different radiation levels in case of a Footer, Large or Small station.

Table 1: ATLAS RPC Simulated Radiation Levels

| | $SRL_{tid}$ [$Gy \cdot 10y^{-1}$] | $SRL_{see}$ [$h \cdot cm^{-2} \cdot 10y^{-1}$] (E > 20 MeV) |
|---|---|---|
| BMF | 3.02 | $4.69 \cdot 10^9$ |
| BML | 2.04 | $5.65 \cdot 10^9$ |
| BMS | 3.03 | $4.73 \cdot 10^9$ |
| BOF | 1.19 | $4.08 \cdot 10^9$ |
| BOL | 1.33 | $4.21 \cdot 10^9$ |
| BOS | 1.26 | $4.10 \cdot 10^9$ |

For the Total Ionising Dose effect, considering the worst case $SRL_{tid}$ value, with the appropriate safety factors, we obtain a radiation tolerance criteria less then 8 krad, to be used as the integrated maximum total dose a CMA has to tolerate in ten years of ATLAS working operation.

The CMA chip has ~ 300 internal registers used for ASIC configuration, programmable via $I^2C$ bus. Single Event Upset has been taken into account during ASIC development. SEU detection logic has been implemented for all chip registers, so that eventual presence of SEU can be monitored during run. Triple redundancy logic has been implemented for critical control registers, in order to drastically reduce the possibility of having upsets in those register and so to assure CMA correct operation during run under radiation.

### *C. CMA architecture*

CMA design has been realized with a 0.18 µm CMOS technology. Standard cell design approach has been used. A PLL is used for 40 MHz external clock frequency multiplication, providing the 320 MHz internal clock. 24 double-port RAMs are used as FIFOs for the readout memory logic. Chip area is 4.5×4.5 $mm^2$, containing ~430.000 gates. Core power supply is 1.8 V, I/O pads power supply is 3.3 V. The ASIC has been packaged in a 352 pin BGA package. Figure 5 shows the chip layout.

The ASIC receives 2×32 input signals coming from the pivot RPC front-end electronics, and 2×64 input signals coming from the non-pivot planes. Level 1 Accept and Reset signals, as well as 40 MHz clock, are distributed by the TTCrx mounted on the PAD board.

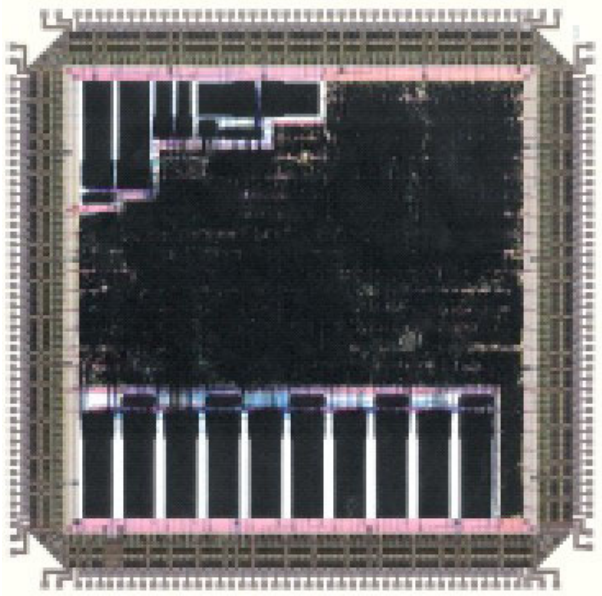

Figure 5: CMA layout

All chip internal registers are accessible as shift registers via an $I^2C$ slave interface implemented into the ASIC. At initialization time, the CMA can be programmed using this serial interface. A 24 bit Control Register is used to store chip main functionality. During initialization all registers are driven by the 40 MHz external clock, and the PLL is disabled. During run mode the PLL is enabled, provides the 320 MHz clock, and feeds a 160 MHz clock generator. 160 MHz clock is used in part of the readout logic, while 320 MHz clock is used for the rest of the logic.

CMA front-end inputs signals are first sent to an input pipeline block, which synchronizes the input signal to the 320 MHz clock, contains the masking to 0 logic, performs signal digital shaping in the range 1÷1/8 of bunch crossing period, and delays signals in the range 3/8÷3 BC periods. The pipeline block is used for input signal time alignment, and can be employed for preloading input patterns for test purposes. Front-end signals dead time is programmable in the range 1÷4 BC periods, in steps of 1/8 BC period.

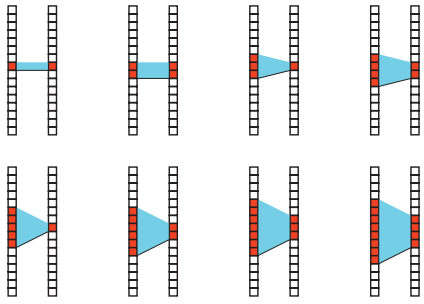

Figure 6: CMA de-clustering logic

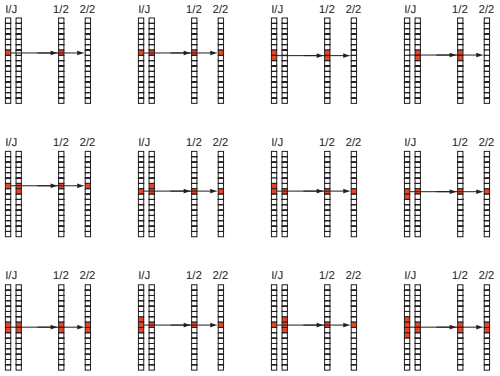


Figure 7: CMA pre-processing logic

Pipeline block output signals are sent to the readout block and to the trigger block. In the trigger block signals are first sent to the de-clustering and pre-processing logic and then to the logic performing the trigger algorithm. Maximum processed cluster size is programmable, up to ±3. Pre-processing logic correlates hits coming from two detector layers, favouring 2/2 hits over 1/2 hit. The logic can be programmed to work for positive and negative η values. Figure 6 and Figure 7 show logic functionality.

Coincidence logic is repeated three times in parallel, one for every programmed threshold. The majority logic can be 1/4, 2/4 (one hit per doublet), 3/4 and 4/4. The highest threshold trigger pattern which has non-zero information is shaped in time and then sent to the chip output. Trigger output pattern can be shaped in the range of 1/8±1 BC period. Trigger logic flags the number of the output threshold, and the eventual overlap between two adjacent regions.

The readout architecture has been studied with a high level simulation [5], which has determined the required buffer sizes and readout bandwidth. The requirements were to monitoring RPC signals with a resolution compatible with the detector time resolution of 1.5 ns [6]. Each group of 32 front-end signals has a dedicated readout path, up to the derandomizer buffer, where hits belonging to the same Level1 ID are assembled in data frame. Figure 8 shows a schematic view of the CMA readout logic.

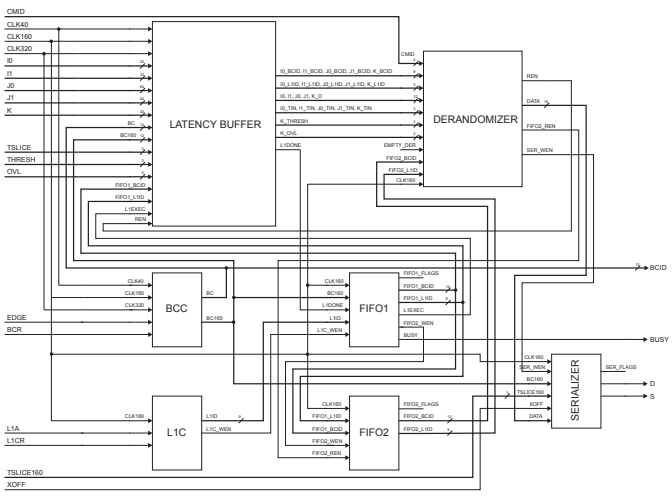


Figure 8: CMA readout block

All buffer memories are implemented with FIFOs. Each input FIFO buffer is written at the full 320 MHz speed and contains the hit pattern, BCID and time interpolator value. The readout part of this buffer, together with the rest of the readout logic works at 160 MHz. FIFO1 and FIFO2 contain a list of Level1 IDs and relative BCIDs respectively to be processed by the derandomizer and ready to be sent via the serializer. FIFO1 is read when hits belonging to a Level1 ID have been processed and sent to the derandomizer. FIFO2 is read when a full event has been sent to the serializer FIFO. Filling status of all FIFOs can be monitored during run [7].

The latency buffer stores hit patterns coming from the input FIFO until they get old, i.e. until the time difference between the running BCID counter and the BCID stored in the latency memory exceeds a programmable value contained in the latency register. Latency memory is 128 BCs maximum (3.2 ms). Latency buffer depth is 256 32-bit patterns (128 for trigger patterns). Each hit is associated a time slice and BC, if more than one are readout. Maximum readout window is 8 BCs. The hit pattern derandomizer FIFO stores hit pattern belonging to a time window flagged by a Level1 Accept, until the whole event gets assembled in the hit derandomizer FIFO. This last FIFO contains headers, sub-headers, footers and hit words, as described in the event data format chapter, ready to be serialized.

The serializer block attaches CRC codes to event fragments and ships the data out, following the DS-link protocol. The serializer block is able to output data at a programmable frequency of 10÷80 MHz. The effective bandwidth is less than 8-64 Mbit/s due to some overhead in the data transmission. A state machine with CRC recalculation and watchdog timer can assure data consistency on the receiving end.

Table 2 contains the full list of the CMA I/O signals. The showed chip signals can be grouped as front-end inputs, TTC inputs, trigger data pattern and flags outputs, readout serial data and flags outputs, $I^2C$ signals, ASIC device addresses, JTAG signals, scan and test signals, reset signal.

Table 2: CMA I/O signals

| | | | |
|---|---|---|---|
| I0[31:0] | positive pivot plane 0 / low pt k-pattern | XOFF | Transmit off input |
| I1[31:0] | pivot plane 1 | BUSY | ASIC busy signal |
| J0[63:0] | non-pivot plane 0 | SCL | I2C clock line |
| J1[63:0] | non-pivot plane 1 | SDA | I2C data line |
| L1ACCEPT | L1 Accept signal | DEVID[7:0] | Device identification input |
| L1CNTRES | L1 counter reset | TCK | TAP SCAN clock |
| BCNTRES | BCID counter reset | TMS | TAP SCAN MODE |
| CLK | 40 MHz | TRST | TAP SCAN RESET |
| TCLK | 10 MHz | TDI | TAP SCAN IN |
| K[31:0] | k-pattern output | TDO | Tristate TAP scan out |
| BCID[11:0] | Bunch crossing ID counter | SE | Scan enable signal |
| THR[1:0] | Threshold value | TST | Test enable signal |
| OVL[1:0] | Overlap value | CLKOUT | PLL clock tree output |
| SER_D | DS-link Data line | CLK160OUT | clk_160 tree output |
| SER_S | DS-link Strobe line | CLR_N | Asynchronous clear |

Design approach used for the project was to first build the VHDL RTL code for all CMA blocks, then build the VHDL

test benches for all blocks and for the full chip. Design synthesis and RTL code modification was then started. Finally scan chains, JTAG logic and I/O pads insertion was executed. At this point place & routing and clock tree building was performed, leading to the final layout.

### *D. CMA test*

Design for testability has been a relevant part in the ASIC development history.

The ASIC has 37 serial scan chains, 32 for core logic and 5 for RAMs. JTAG boundary scan and $I^2C$ slave capability have been implemented as well. All core CMA registers and all RAMs are accessible via scan chains. Register accessibility is fundamental during ASIC acceptance tests. Dedicated scan chains have been designed for RAM data, addresses and control signals, in order to be able to test the RAM cores. JTAG boundary scan can be used for board check during assembly tests. $I^2C$ interface can be employed for register accessibility and test pattern generation during functional tests. Finally, input pipelines can be preloaded via $I^2C$ with appropriate hit patterns, so that the chip can be run for a fixed programmed number of cycles for test purposes.

A CMA dedicated load-board was developed for industry tester. The board has been designed with additional connectors for PLL test and lab tests in Rome. Scan and functional tests were first performed on industry machine at 1 MHz and 40 MHz input clock frequency, at room and at 125°C temperatures. Test machine used test patterns provided by Rome. Industry test executed on the first 86 available CMA packages showed a yield of ~81%. Functional test at 40 MHz were then executed, again using Rome test vectors. No logic fail was detected on functional test.

The test board was then used for lab test in Rome. 160 MHz derived clock output has been used to check PLL stability and functionality. PLL has been characterized vs. voltage and vs. input frequency. Measured jitter is 25 ps rms, 150 ps pk-pk. PLL works according to specifications.

Trigger test was performed on a limited number of input channels, due to limitations on the laboratory setup. Minimum hit pulse width measurement was ~6 ns (it was 12 ns in specs). Dead timer, pulse shaping and pipeline delay logic are working according to specs. Trigger output latency was measured, giving the numbers showed in Table 3.

Table 3: CMA measured trigger output latency.

| | |
|---|---|
| Input to K-pattern delay | $T_{latkpat}$ = (59 ± 1) ns |
| Input to THR/OVL delay | $T_{latthr}$ = (63÷88 ± 1) ns |
| Skew between THR and OVL | $T_{outskew}$ = (2 ± 0.5) ns |

Readout tests were done at 40 Mbit/s using 10ns period sampling with waveform analyzer. A C++ deserializer program has been used to convert waveform vectors to readout data fragments. Readout logic works correctly. Figure 9 shows the measured readout latency time. Nominal point, corresponding to 1% of RPC occupancy, is 3 hits.

Measured power consumption during run mode in nominal operation is ~1.2 W.

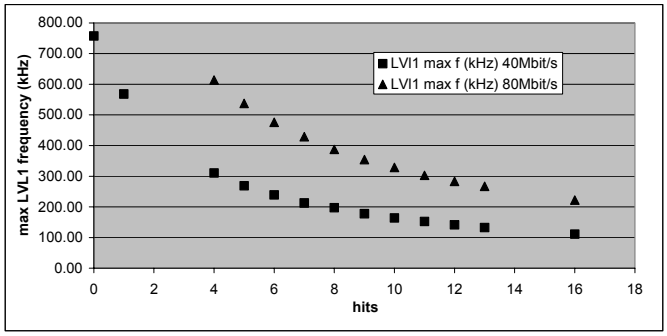


Figure 9: CMA readout latency

## III. CONCLUSIONS

CMA test showed a correct ASIC functionality. Still radiation test has to be performed to show chip correct functionality under the ATLAS RPC radiation environment. For this purpose a test under gamma photon irradiation is scheduled for Total Ionising Dose effects evaluation. A 60 MeV proton irradiation test is planned for Single Event Effects study.

Complete CMA functionality will be studied in a dedicated trigger slice test. For this test four CMAs will be mounted on a full equipped PAD board. Incoming signals from RPC detectors under muon test beam will be used.

Up to now no problems or functional bugs have been founded, so no other ASIC releases are previewed.

## IV. REFERENCES


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[2] Petrolo, A.Salamon, R.Vari, S.Veneziano: *Barrel LVL1 Muon Trigger Coincidence Matrix ASIC User Requirement Document* (ATL-COM-DAQ-2000-050)

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[4] ATLAS Policy in Radiation Tolerant Electronics: http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/radhard_MUON_RPC.htm

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[7] V.Bocci, G.Chiodi, S.Di Marco, E.Gennari, E.Petrolo, A.Salamon*,, S.Veneziano*: *Prototype Slice of the Level-1 Muon Trigger in the Barrel Region of the ATLAS Experiment* (LECC2001 proceedings)