

Tests of the CMS Level-1 Regional Calorimeter Trigger Prototypes

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Abstract

The CMS calorimeter regional trigger system is designed to detect signatures of isolated and non-isolated electrons/photons, jets, τ s, and missing and total transverse energy using deadtimeless pipelined architecture. This system comprises of 18 crates of custom-built electronics. The pre-production prototype backplane, boards, links and ASICs have been built and their performance is characterized.

1. Introduction

The CMS level-1 electron/photon, τ , jet, and missing transverse energy trigger decisions are based on input from the level-1 Regional Calorimeter Trigger (RCT) [1]. The RCT plays an integral role in the reduction of the input rate to the global trigger and finally the Higher Level Triggers (HLT) while separating physics signals from background with high efficiency. The RCT receives input from the brass/scintillator CMS hadron calorimeter (HCAL) and PbWO₄ crystal electromagnetic calorimeter (ECAL), that extend to $|\eta|=3$. An additional hadron calorimeter in the very forward region (HF) extends coverage to $|\eta|=5$. A calorimeter trigger tower is defined as 5×5 crystals in the ECAL of dimensions 0.087×0.087 ($\Delta\phi \times \Delta\eta$), which corresponds 1:1 to the physical tower size of the HCAL. Since the HF is not used in any electron or photon algorithm, it has a coarser segmentation in η and ϕ .

The algorithm to find electron and photon candidates uses a 3×3 calorimeter trigger tower sliding window centered on all ECAL/HCAL trigger towers out to $|\eta|=2.5$. Two types of electromagnetic objects are defined, a non-isolated and an isolated electron/photon. Four of each type of electron per regional crate are forwarded to the global calorimeter trigger for further sorting. The top four candidates of each type are received by the level-1 global trigger.

The jet trigger uses the transverse energy sums (ECAL+HCAL) for each 4×4 trigger tower calorimeter region in the barrel and endcap [2]. In the very forward region ($3 < |\eta| < 5$) of the CMS spectrometer, each HF tower is treated as a region and their $\Delta\phi$ division matches that of the 4×4 regions of the barrel and endcap. The jet or τ -tagged jet is defined by a 3×3 region E_T sum. In the case of τ -tagged jets ($|\eta| < 2.5$), none of the nine regions are allowed to have more than 2 active ECAL or HCAL towers (i.e. above a programmable threshold). Jets in the HF are defined as forward jets. Four of the highest energy central, forward, and τ -tagged jets are selected, allowing independent sorting of these 3 jet types until the final

stage of jet sorting and trigger decision. In total, there are twelve jets available at the global trigger level.

2. Calorimeter Trigger Hardware

The regional calorimeter trigger electronics comprises 18 crates for the barrel, endcap, and forward calorimeters and one cluster crate to handle the jet algorithms. This will be housed in the CMS underground counting rooms adjacent to the underground experimental area.

Twenty-four bits comprising two 8-bit calorimeter energies, an energy characterization bit, and 5 bits of error detection code will be sent from the ECAL, HCAL, and HF calorimeter electronics to the nearby RCT racks on 1.2 Gbaud copper links. This is done using one of the four 24-bit channels of the Vitesse 7216-1 serial transceiver chip on calorimeter output and RCT input, for 8 channels of calorimeter data per chip. The RCT V7216-1 chips are mounted on eight mezzanine cards located on each of 7 receiver cards for each of 18 RCT crates. The V7216-1 converts serial data to parallel data, which is then deskewed, linearized, and summed before transmission on a 160 MHz custom backplane to 7 electron isolation cards and one jet/summary card. The jet/summary card sends the regional E_T sums to the cluster crate and the electron candidates to the global calorimeter trigger (GCT). The cluster crate will implement the jet algorithms and forward the 12 jets to the global calorimeter trigger.

The Receiver Card, in addition to receiving calorimeter data on copper cables using the V7216-1, shares data on cables between RCT crates. Synchronization of all data is done with the local clock and Phase ASIC (described below) and checked for data transmission errors. Lookup tables are used to translate the incoming E_T values onto several scales and set bits for Minimum Ionizing and Quiet signals. Adder blocks begin the energy summation tree, reducing the data sent to the 160 MHz backplane.

The Electron Isolation card receives data for 32 central towers and 28 neighboring towers via the backplane. The electron isolation algorithm is implemented in the Isolation ASIC described below. Four electron candidates are transmitted via the backplane to the jet/summary (J/S) card. The electrons are sorted in a Sort ASIC on the J/S Card and the top 4 of each type are transmitted to the GCT for further processing. The J/S card also receives E_T sums via the backplane, and forwards them and the minimum ionizing and quiet bits to the GCT.

To implement the algorithms described above, five high-speed custom Vitesse ASICs are used: a Phase ASIC, an Adder ASIC, a Boundary Scan ASIC, a Sort ASIC, and an

Electron Isolation ASIC [3]. They were produced in Vitesse FX™ and GLX™ gate arrays utilizing their sub-micron high integration Gallium Arsenide MESFET technology. Except for the 120 MHz TTL input of the Phase ASIC, all ASIC I/O is 160 MHz ECL.

The Phase ASICs on the receiver card align and synchronize the data received on four channels of parallel data from the Vitesse 7216. The Adder ASICs sum up eight 11-bit energies (including the sign) in 25 ns, while providing bits for overflows. The Boundary Scan ASIC handles board level boundary scan functions and drivers for data sharing. Four 7-bit electromagnetic energies, a veto bit, and nearest-neighbor energies are handled every 6.25 ns by the Electron Isolation ASICs, which are located on the electron isolation card. Sort ASICs will be located on the jet/summary cards for sorting the e/γ and process the E_T sums. In the cluster crate Adder and Sort ASICs will be used for the jet algorithms. The Adder ASIC has been successfully tested and procured in the full quantity needed for the system. All other ASICs have been manufactured and are installed on the prototype boards described below [3]

3. Pre-production Prototypes

Custom pre-production prototype 9U VME crate, clock and control card, receiver card, and electron isolation card have been produced with the above ASICs. Mezzanine cards with the Vitesse 7216-1 serial link for the receiver card and dedicated test cards have also been constructed. Results from testing, including the bit error rate of the Vitesse 7216-1 4 Gbaud Cu Links, data synchronization and throughput measurements, and ASIC evaluation will be presented.

The successful conclusion of the first generation prototype program proved the design as described in Chapter 5 of the CMS Trigger Technical Design Report (TDR), which was approved in March 2001 [2]. Therefore, 2001 marked the start of the construction of full-function pre-production modules based on the TDR. All pre-production boards and ASICs in the system, with the exception of the Jet/Summary Card, have been manufactured. The Jet/Summary Card is ready to be built, but is holding pending results from testing the other boards that contain similar circuitry. In addition, all ASIC production has been finished.

We have built a pre-production crate, shown in Figure 1, with new backplane that implements all of the level-1 trigger algorithms approved by CMS and the LHCC, and documented in the Trigger TDR. The backplane is located in the middle of the crate between a card cage of 400 mm in depth at the rear and a card cage 280 mm deep in the front. As shown in the figure, the backplane is a monolithic, custom, 9U high printed circuit board with front and back card connectors. The top 3U of the backplane utilizes 4 row (128 pin) DIN connectors, capable of full 32 bit VME. The two leftmost front slots of the backplane uses three row (96 pin) DIN connectors

in the P1 and P2 positions with the standard VME pin out. Thus, a standard VME system module can be inserted in the two front stations with a form factor conversion between the first slot and remaining slots performed on the custom backplane. The rear of the crate behind the two standard VME stations is occupied by the power supply. The bottom 6U of the backplane, in the data processing section of the crate, utilizes a single high speed, controlled impedance, connector for both front and rear insertion at alternating card positions.

The backplane uses a 340-pin connector, by AMP Inc, to handle the high volume of data transmitted from the Receiver cards to the Electron Isolation and Jet Summary Cards. The AMP 340 pin stripline connectors have a power plane between every four signal pins, producing a impedance of 50Ω . Separate high current contacts, provided for the power plane connections, are used to transmit power to the boards. The connectors are housed in a cast aluminum shell that doubles as a board stiffener. The electrical characteristics of the connectors are excellent, allowing sub-nanosecond rise times with very low crosstalk.

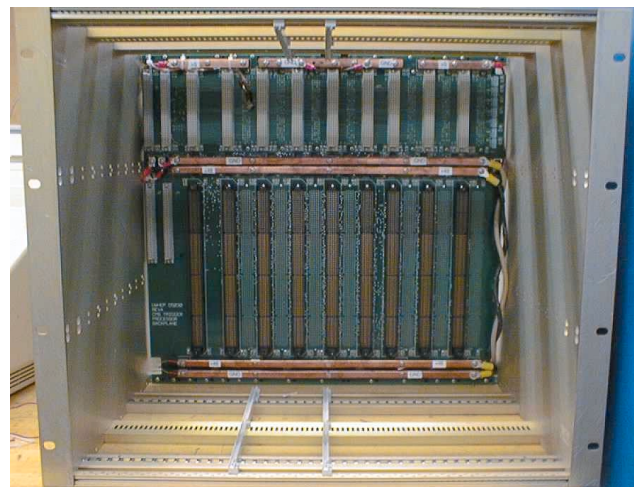
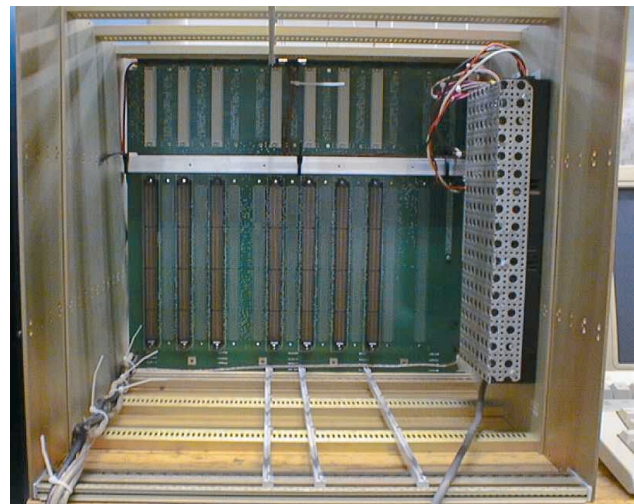


Figure 1. Pre-production crate front (bottom) and rear (top) views.

We have built a new Clock and Control Card, shown in Figure 2, that matches the timing in the new backplane and cards. We have built a full function Receiver Card, shown in Figure 3 and Figure 4, on which we have installed the Adder, Phase and Boundary Scan ASICs, as well as the new version of the 4 Gbit/s serial receiver mezzanine card, shown in Figure 5. Power on the full size cards is mostly provided by DC to DC converters connected to 48 V fed from the backplane power pins. The new Receiver Card features mezzanine cards with an improved version of the Vitesse serial receiver chip that is more tolerant of clock jitter.

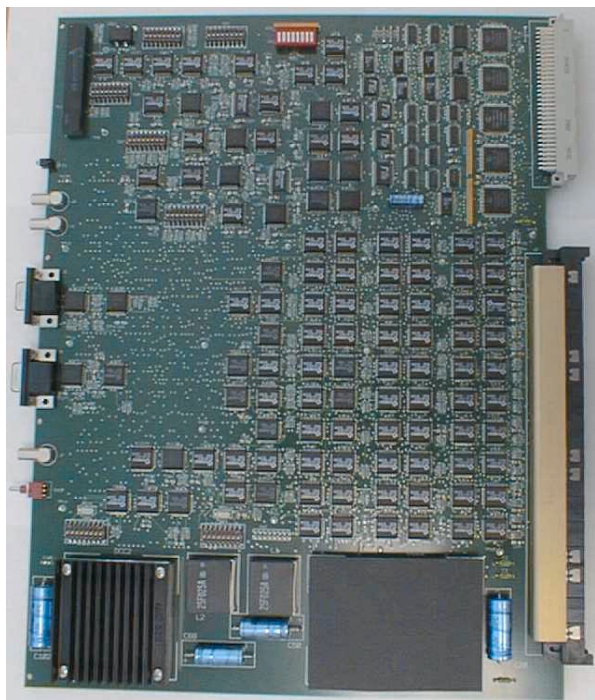


Figure 2. Preproduction Clock & Control Card.

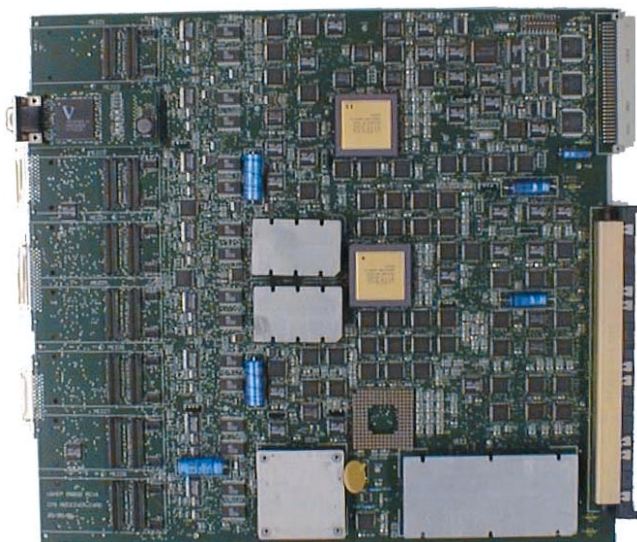


Figure 3. Pre-production receiver card front showing Adder ASICs and a Mezzanine Receiver Card installed.

We have also built a dedicated new Serial Test Card, shown in Figure 6 for testing these mezzanine cards and performing detailed bit error checking. Additional copies of this card will be used for production testing of the mezzanine cards and integration tests with ECAL and HCAL electronics. We have also built a full function Electron Isolation Card, shown in Figure 7, on which we have installed the Electron Isolation and Sort ASICs. The design and layout of the prototype Jet/Summary Card, is complete and it is being manufactured.

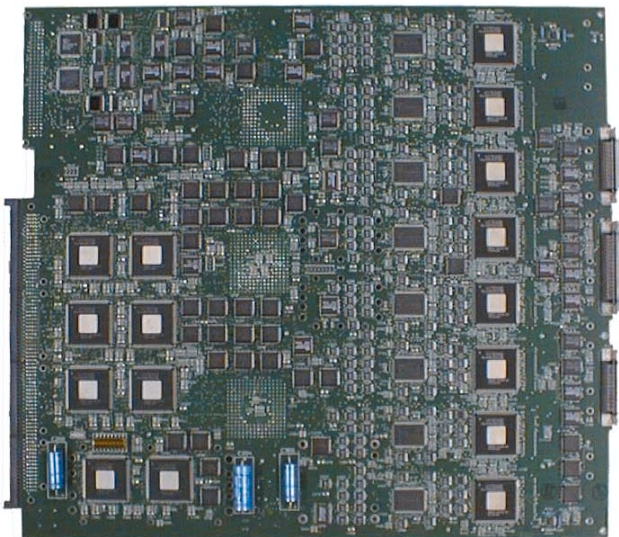


Figure 4. Pre-production Receiver Card rear showing Phase and Boundary Scan ASICs.



Figure 5. Pre-production 4 Gbit/s Copper Receiver Mezzanine Card.

We are engaged in a detailed testing and validation program of the pre-production trigger boards. As shown in Figure 8, we are testing a fully functional crate with the pre-production Receiver Card, Clock Card, Backplane and Electron Isolation card. When complete, these tests will fully verify all 5 Vitesse custom ASICs. Thus far, we have validated the Phase, Sort and Adder ASICs and

completed their production. Substantial portions of the Receiver Card, Clock Card, Electron Isolation Card and Backplane have been validated. Signal quality and timing alignment have been measured to be well within tolerances. Verification of data pathways and logic function is checked using Boundary Scan, which is fully implemented on all boards and ASICs.



Figure 6. Pre-production Serial Link Test Card.



Figure 7. Pre-production Electron Isolation Card with Electron ID and Sort ASICs installed.

We conducted tests of the pre-production 4 Gbit/s copper serial link system. The cable used in the tests is composed of pairs of 20 m lengths of 22 AWG Spectra Strip Skew-

Clear[®] shielded 2-pair cable with VGA-type 15-pin DIN connectors. We built a special “test” transmitter mezzanine card to drive the signals over the cables and used two Serial Link Test Cards to continuously transmit and receive pseudo-random data over many days with a trap on error, yielding a bit error rate of less than 10^{-15} .

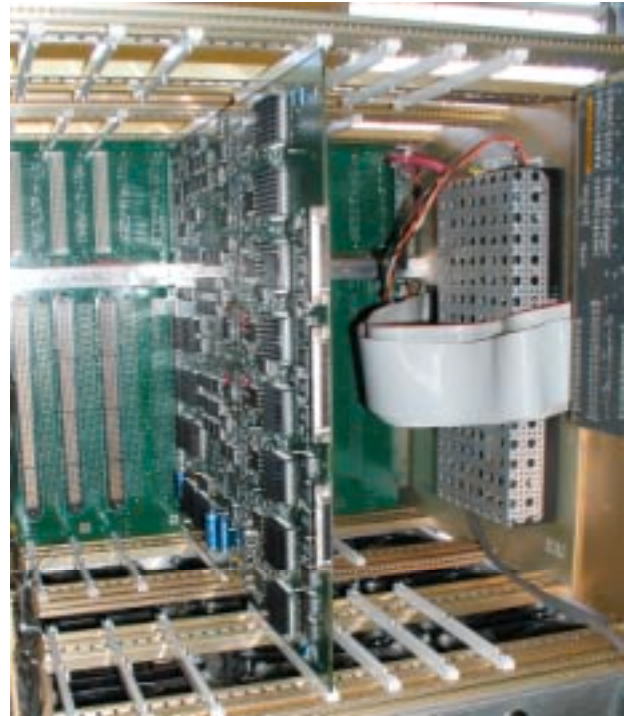


Figure 8. Receiver Card under test in crate.

4. Summary

Construction of the CMS level-1 Regional Calorimeter Trigger Pre-production Prototype Receiver Card, Isolation card, Clock and Control Card, Serial Link Mezzanine Card, Backplane, Crate and five custom ASICs that implement the CMS level-1 calorimeter trigger algorithms is complete. Tests conducted thus far have validated the design of the production boards.

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References

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- [3] W. Smith et al. CMS Regional Calorimeter Trigger High Speed ASICs, *Proceedings of the Sixth Workshop on Electronics for LHC Experiments*, Krakow, Poland, September 2000, CERN 2000-010.