
The ATLAS Level-1 Muon to Central Trigger Processor Interface (MUCTPI)

Kunihiro Nagano (CERN)

on behalf of the MUCTPI Team:

N. Ellis, P. Farthouat, K. Nagano, G. Schuler, C. Schwick, R. Spiwoks, T. Wengler

“8th Workshop on Electronics for LHC Experiments”

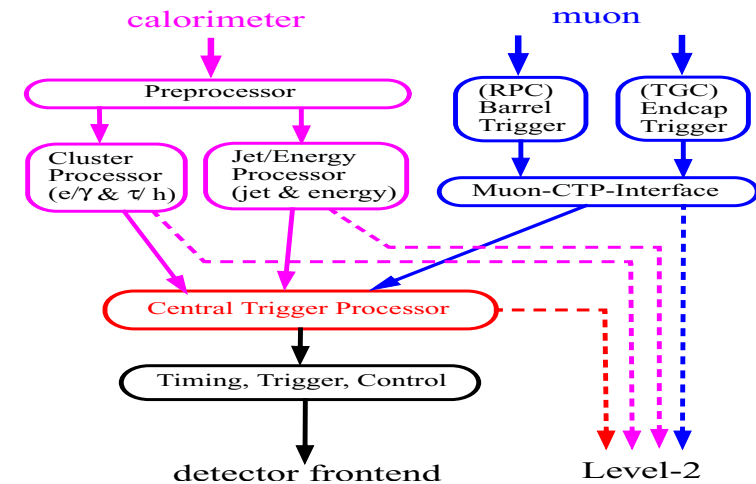
Colmar, France, Sep. 9 – 13, 2002

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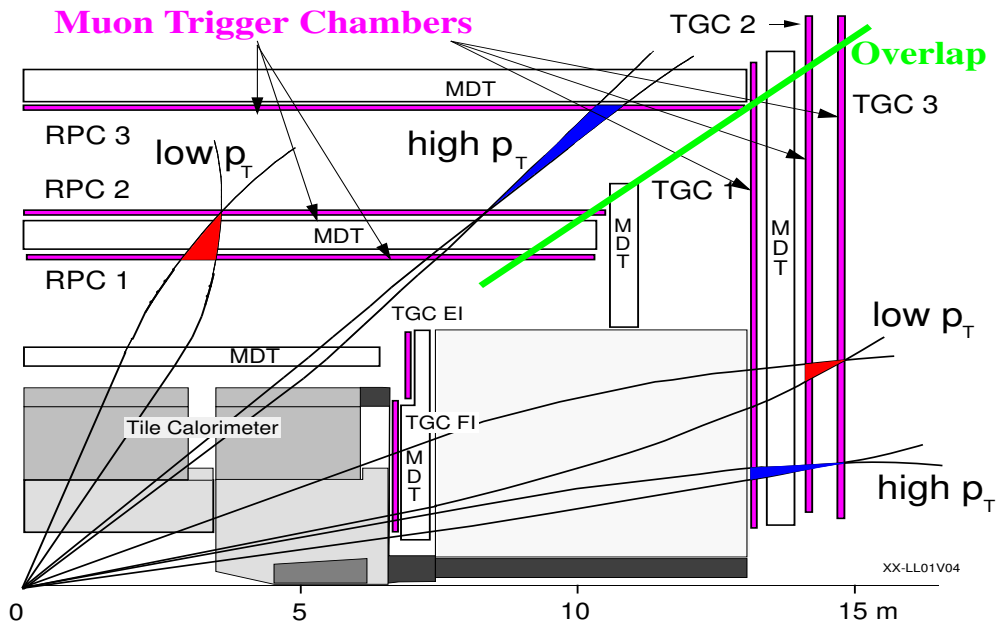
- ▶ Introduction
- ▶ Full-system tests with a prototype and integration tests with external systems
- ▶ System performance
- ▶ Summary

▶ ATLAS Level-1 Trigger

- Two main trigger systems: calorimeter and muon
- Reduce 40 MHz BC rate → 75 kHz
- Send Region-of-Interest (RoI) information to Level-2



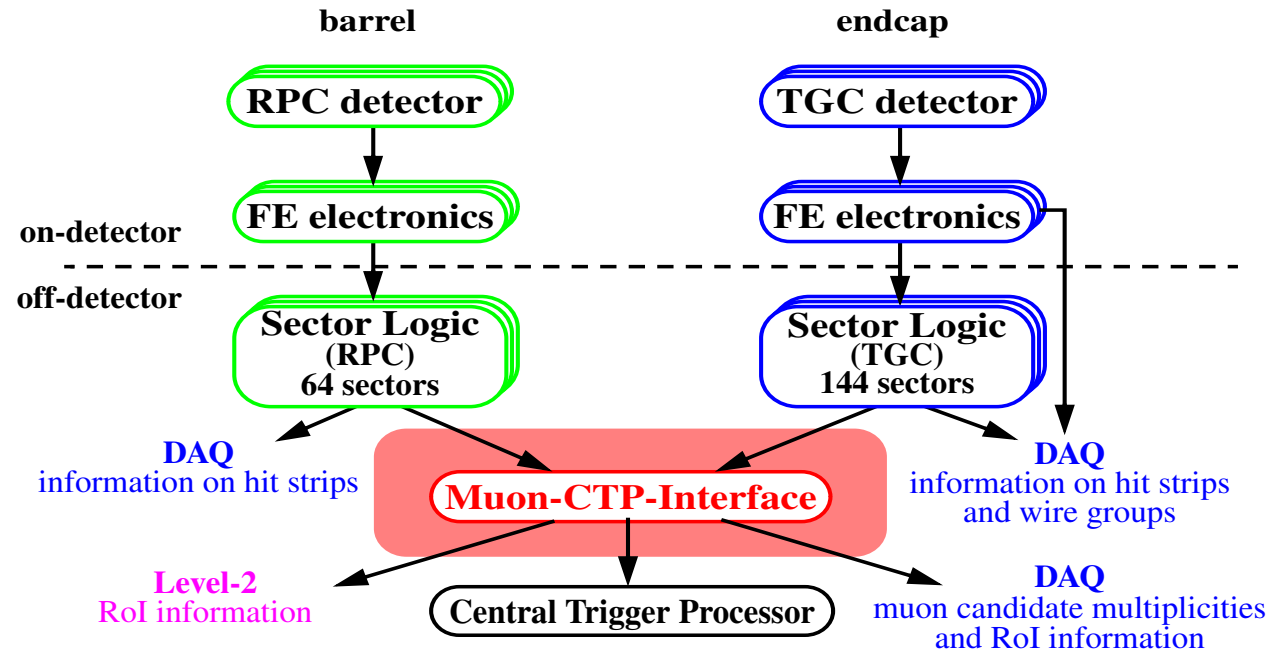
Level-1 Muon Trigger



- ▶ Barrel: Resistive Plate Chambers (RPCs)
- ▶ Endcap: Thin Gap Chambers (TGCs)

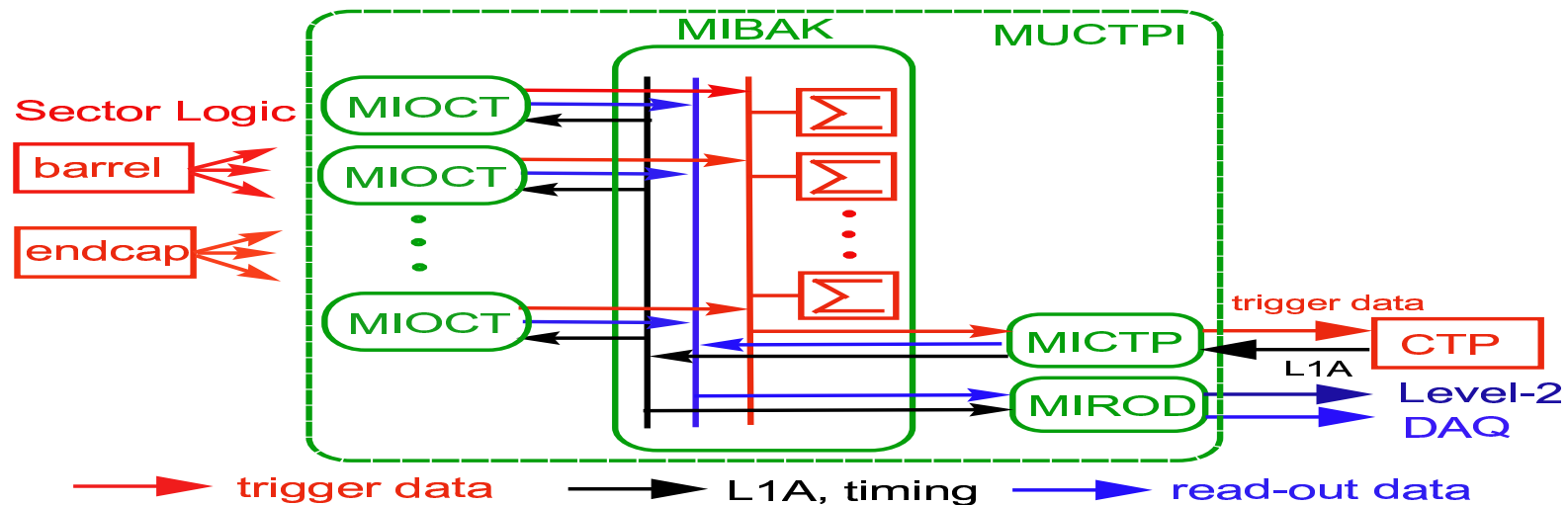
- Trigger chambers are grouped into sectors
- Tracks: coincidence between layers of chambers,
 p_T : size of the coincidence window
- Double counting of single μ crossing more than one sector (“overlap”) must be avoided.
→ particularly for low- p_T muons (with strong deflection in magnetic field), overlap may become a serious problem
- Expected number of μ candidates:
for a typical event: $\lesssim 1$

Level-1 Muon Trigger System



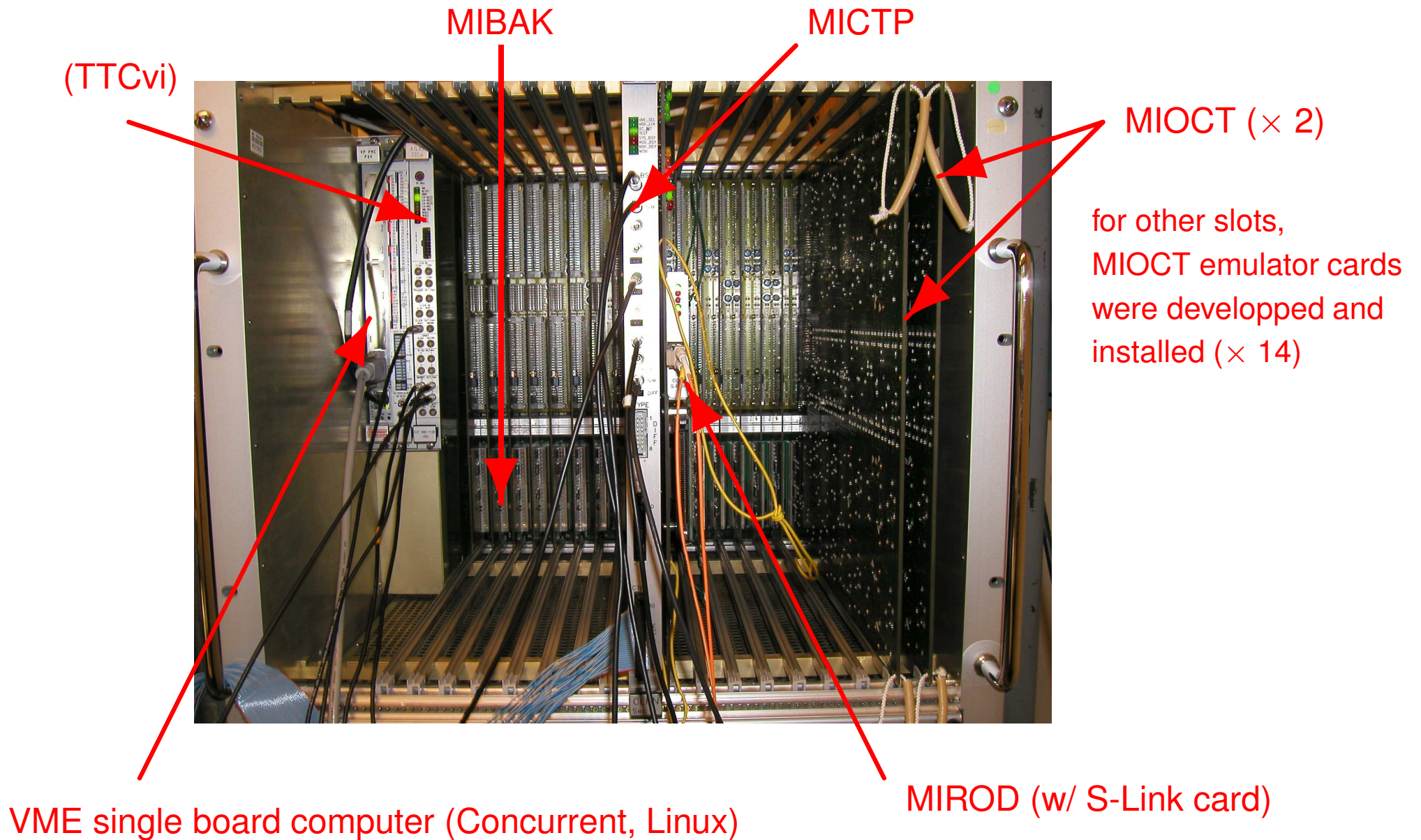
Muon-CTP-Interface (MUCTPI)

- ▶ Evaluates total multiplicity of level-1 μ candidates (max. multiplicity value is limited to 7)
 - For 6 programmable p_T thresholds
 - Possible overlaps across sectors are resolved
- ▶ Input links from: Sector Logic (trigger data)
- ▶ Output links to: CTP (multiplicity information), Level-2 (Region-of-Interest information), DAQ (event data)



- ▶ MIOCT: Octant Boards
 - Receive input from sectors in one octant (+z or -z side)
 - Overlap resolved in each octant (there is no overlap between octants)
 - Within sectors overlaps are handled by the RPC or TGC trigger logic
- ▶ MIBAK: active backplane for multiplicity summation
 - Transfer of data and fast signals
- ▶ MICTP: CTP interface
 - Interface to CTP (multiplicity data) and trigger, timing signals e.g. bunch crossing clock (BC), bunch counter reset (BCR), Level-1 accept (L1A), etc.
- ▶ MIROD: Readout Driver
 - Level-2 (RoI information): sort candidates by p_T , limit in number, send RoI to Level-2
 - DAQ (event data): send all candidates to DAQ

MUCTPI: Implementation



Demonstrator Prototype

- 2 MIOCTs: fully functional (14 sectors per module, overlap region fixed)
 - 1 MIBAK : fully functional
 - 1 MIROD : fully functional
- ⇒ MIOCT/MIROD/MIBAK: individual modules were tested and were verified to satisfy requirements (reported at LEB 2000)

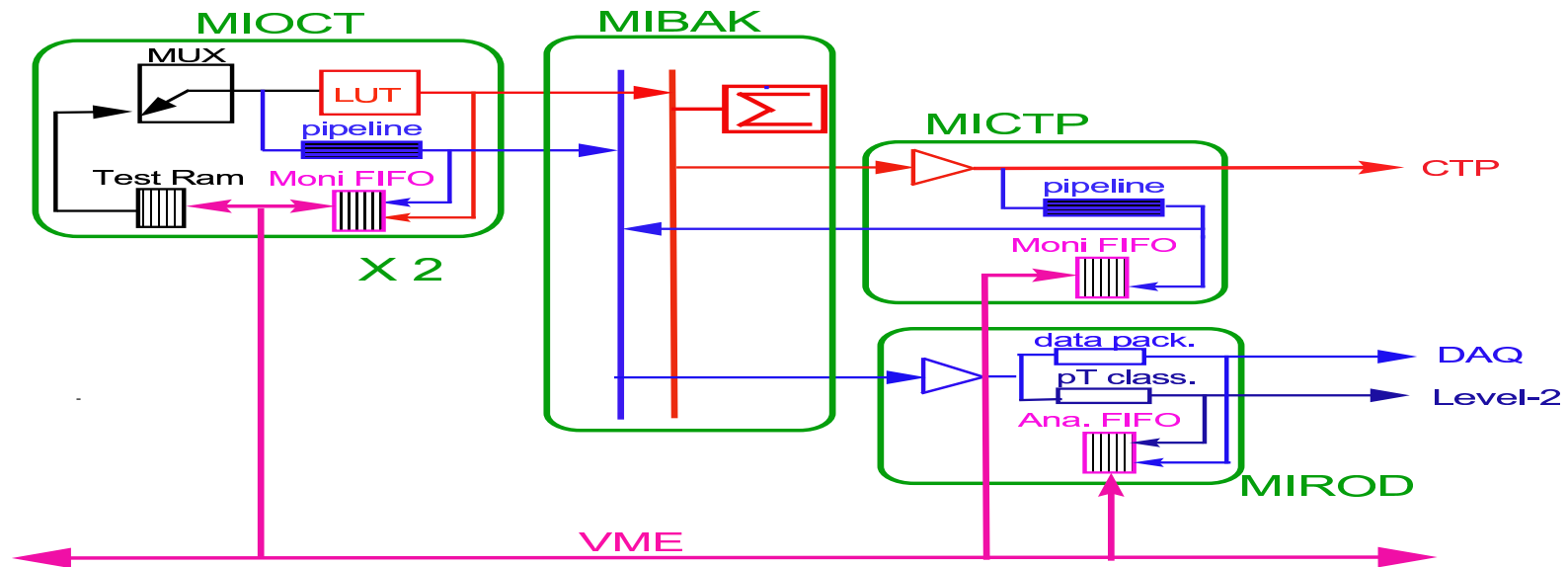
What's new

- 1 MICTP: prototype produced in 2002
 - Implemented using: CPLD (ALTERA EPM71), FPGA (ALTERA 10K), high speed differential receiver ICs (Texas Inst. SNLVDS32B) etc.
 - JTAG access for configuration of MIBAK CPLDs (used for multiplicity summation) and of MICTP internal PLDs
- ▶ Full-system test
- ▶ Integration tests to prototypes of: CTP, Sector Logic, Level-2, DAQ
- ▶ System performance

... covered by this presentation.



Setup

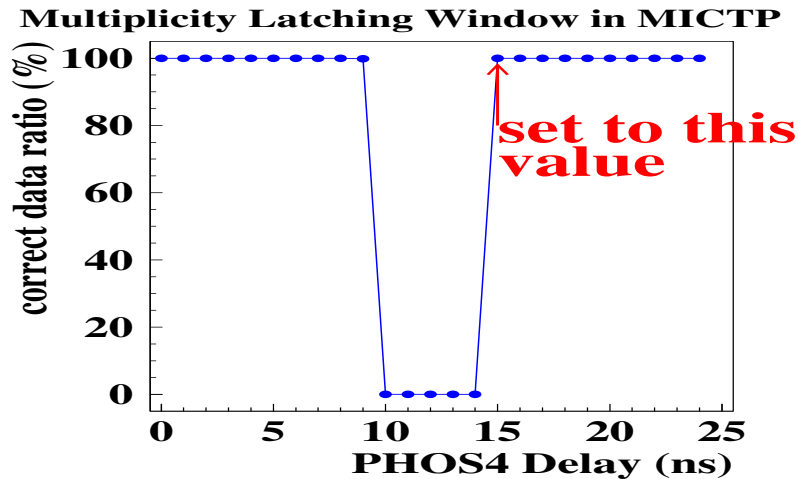


- Input data: MIOCT test memories (14 sectors \times 256 words)
- L1A and BCR: provided by TTCvi (using INHIBIT channels)
- Monitoring FIFOs of all modules \rightarrow results read out over VME and checked

Timing alignment between MICTP and MIOCT

- Adjust pipeline length for read-out
- Adjust offset value for BC counter

Latch multiplicity data at input to MICTP as early as possible to minimise latency



- ▶ Optimise 1 *ns* precision variable delay (CERN PHOS4 via I2C interface)
 - MIOCT sends test pattern in which almost all bits toggle.
 - at MICTP: data verification → “latching window”

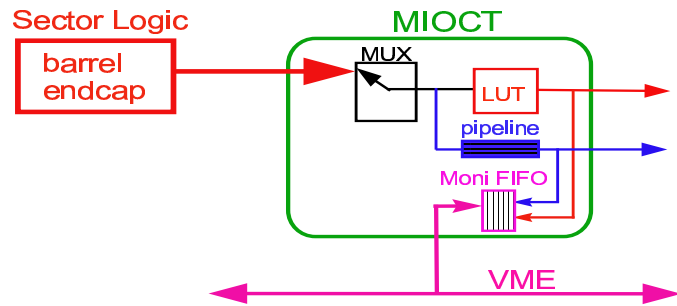
Validation of MUCTPI processing using offline event-generator and simulator

- test vectors were generated randomly
- comparison between simulation and read-out data
 - multiplicity (overlap handling)
 - internal data consistency (comparison between MICTP/MIOCT/MIROD)

⇒ No error in 100 K test vectors, stable run over 2 days

Trigger Path Connectivity: from Sector Logic

Setup: Sector Logic (SL) \Rightarrow MIOCT (LVDS, 32 bit \times 40 MHz)



- Sector logic prototype provides data to an input of one of the MIOCT boards
- MIOCT monitoring FIFO was read-out to verify data integrity

Integration tests to:

- \rightarrow barrel SL demonstrator
- \rightarrow endcap SL prototype

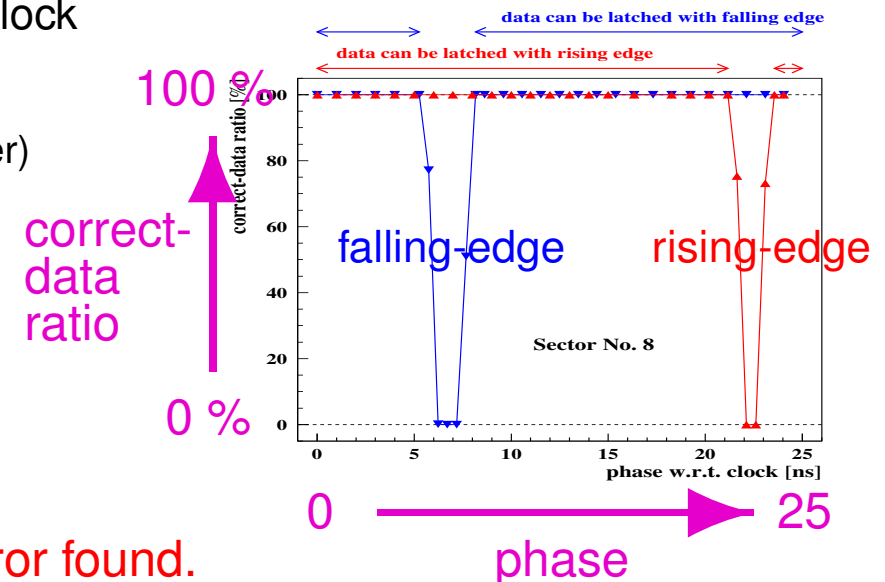
Special thanks to: A. Salamon, S. Veneziano *et. al* (barrel) and R. Ichimiya, H. Kurashige *et. al* (endcap)

Data Latching

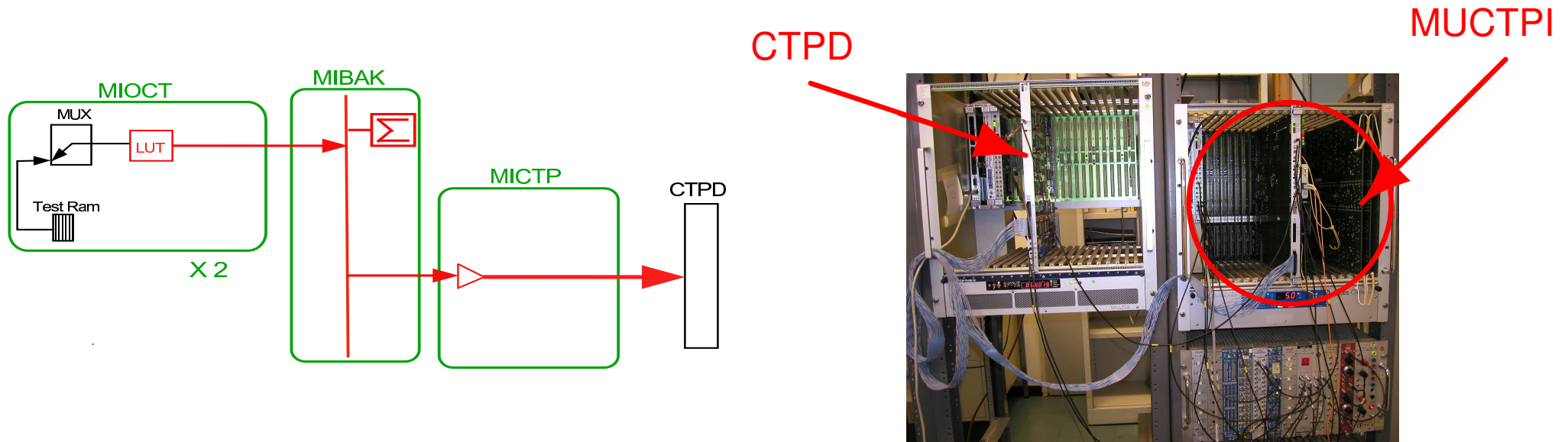
- Method: latches data on either rising or falling edge of clock
 - Monitor: measure phase of sector word w.r.t BC clock
CERN/EP/MIC TDC32 (controlled via embedded JTAG controller)
- \Rightarrow Latching window: 17 \sim 20 ns for both edges,
10 \sim 15 ns overlaps each other
- \Rightarrow Sector input data can be latched safely on MIOCT

Data Integrity and stability

\Rightarrow $\sim 10^9$ events were checked over ~ 48 hours, no error found.



Setup: MICTP \Rightarrow CTP demonstrator (ECL differential, 18 bit \times 40 MHz)

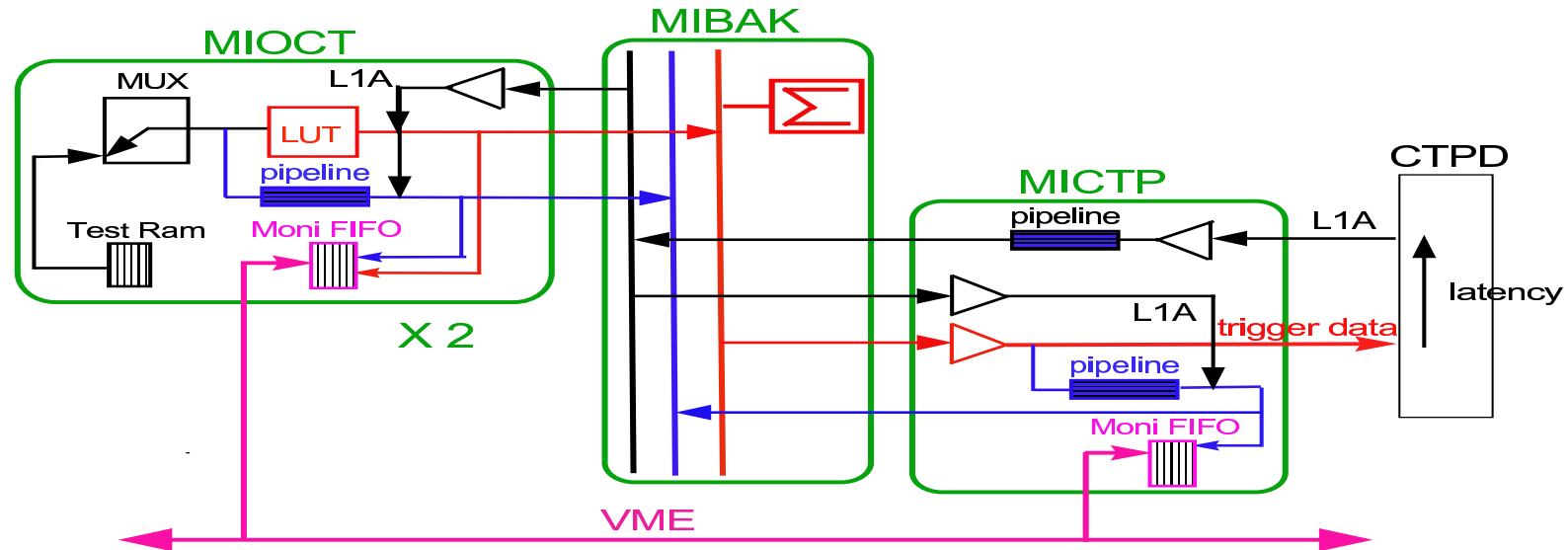


- CTP demonstrator (CTPD): 32 bit input and 32 trigger items
(final design: 160 bit inputs and 96 trigger items; CTPD was built 6 years ago to prove the principle)

multiplicity data latching by CTPD

- ▶ Phase: measured in steps of 1.5 ns , latching window was obtained
→ latch as early as possible to minimise latency
- ▶ Data verification: no error, stable over a few hours

Timing-in of MUCTPI



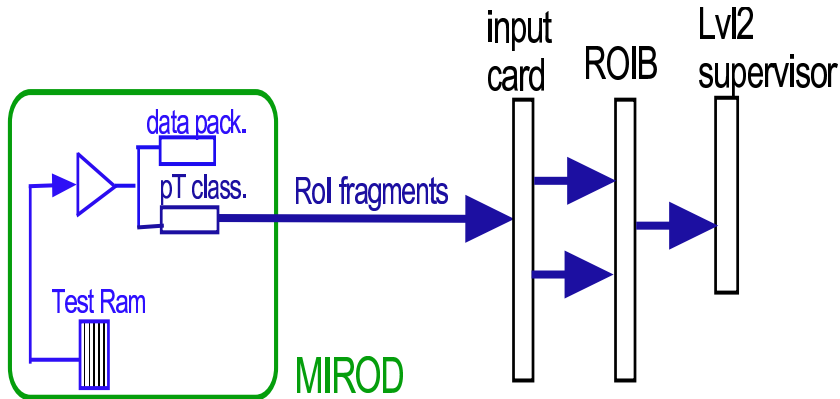
► L1A timing-in:

- Sector data loaded in test memory of MIOCTs produces multiplicities that are sent to the CTPD which in turn generates the L1A \Rightarrow MUCTPI should r/o “the event” which has triggered
- A global delay in MICTP + pipeline length each in MICTP (multiplicity) and MIOCT (sector data) were tuned to accommodate the CTPD latency
- MIOCT’s readout pipelines are sufficient but have limited flexibility to cope with unexpected increases of the L1A latency

► BCR timing-in: (a TTCvi provided BC and BCR to both CTPD and MUCTPI)

- Adjust offset for BC counter in MICTP and MIOCT modules

Setup: MIROD \Rightarrow Region-of-Interest Builder (S-Link)



- ▶ Region-of-Interest Builder (ROIB) demonstrator:
 - Receive ROI fragments (from N sources), construct detector-wide ROI
 - Outputs to Level-2 supervisor (M destinations allowed)
 - Implemented in VME 12U

- Input: MIROD test memory: cycling through with a programmable speed
- Data verification: at Level-2 supervisor (RIO2 single board computer)

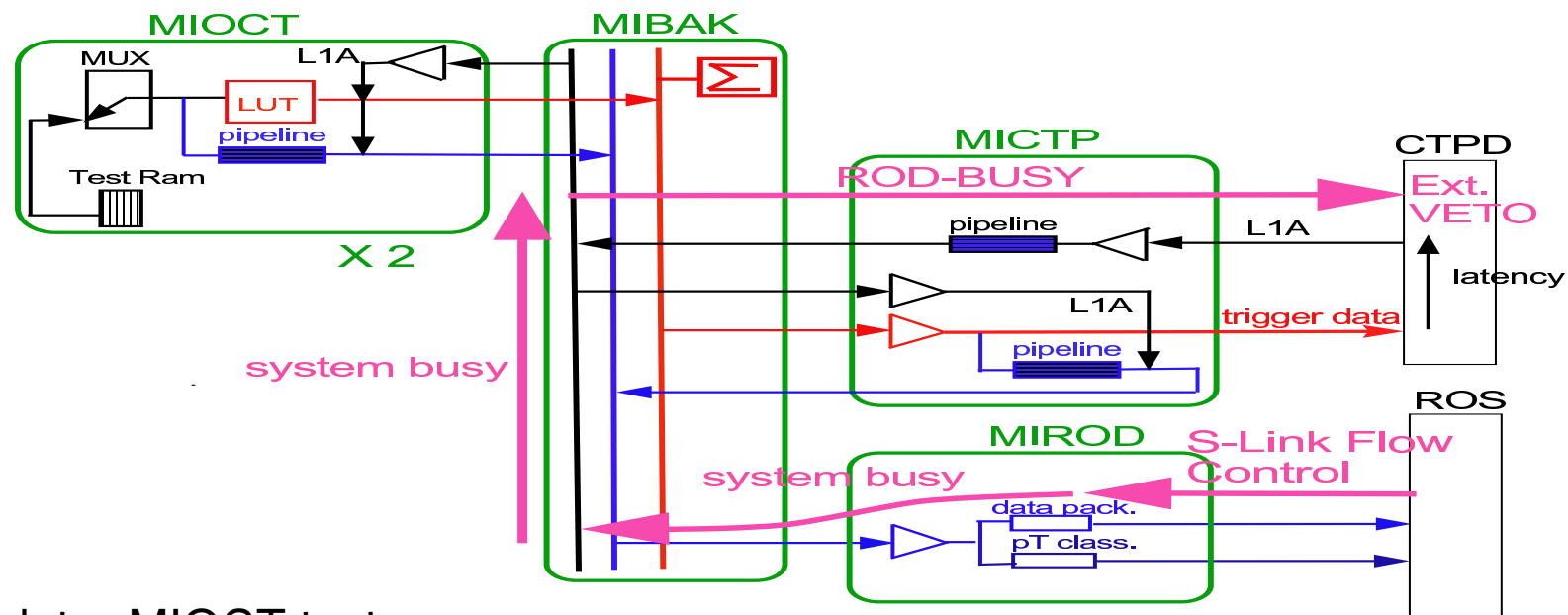
Results of the integration test

Special thanks to: J. Dawson, Y. Ermoline, J. Schlereth *et. al*, ROIB colleagues

- ▶ Read-out rate
 - 100 (80) kHz without (with) data verification
(CPU of Level-2 supervisor limited throughput)
- ▶ Latency
 - 2.6 μ s: L1A \rightarrow RoIB_{in} for 12 muon candidates event

Read-out Path Connectivity: to Read-out System (ROS)

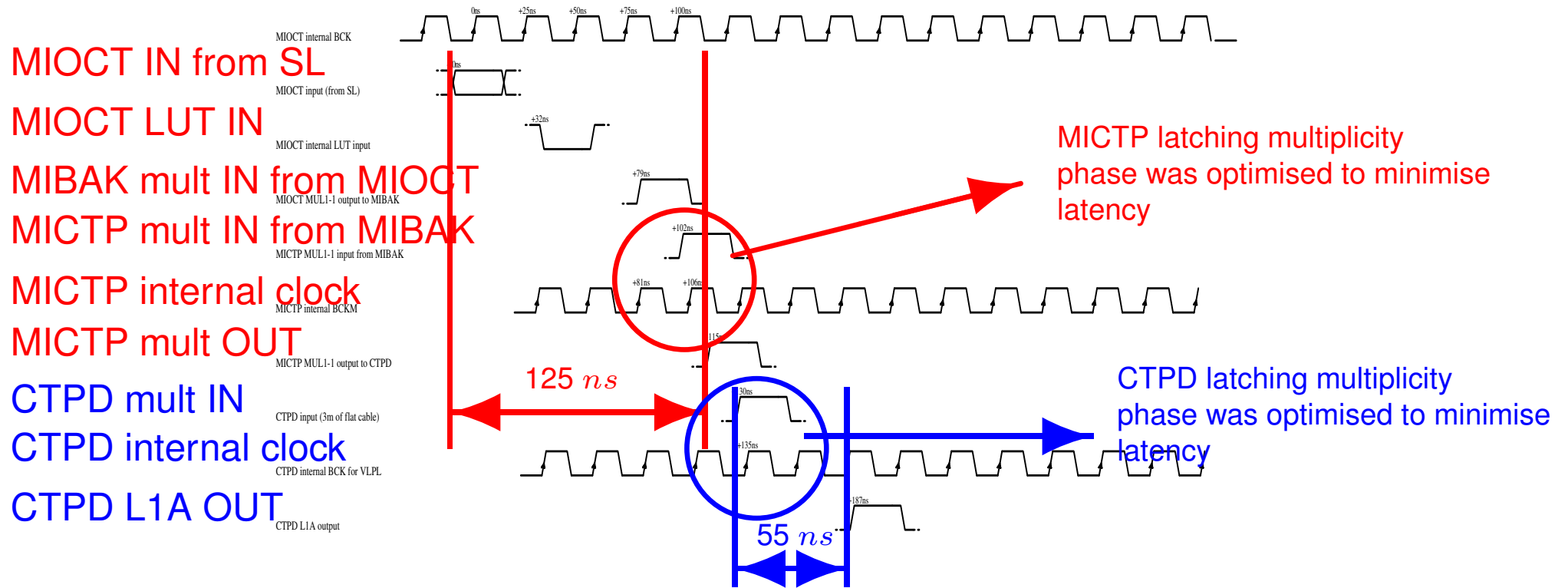
Setup



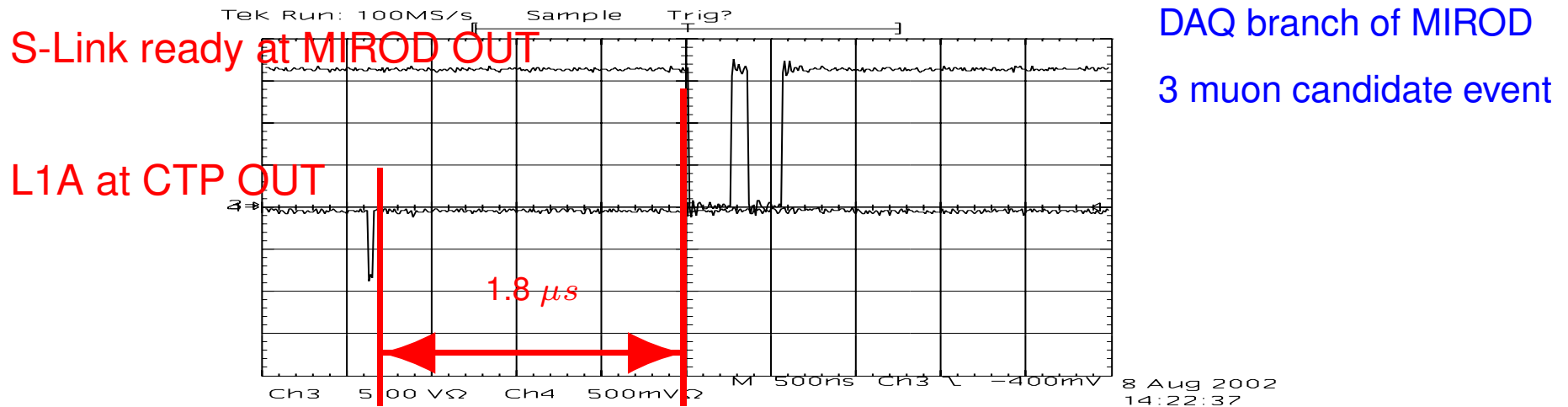
- ▶ Input data: MIOCT test memory
- ▶ L1A generation: CTPD
- ▶ Read-out destination: Read-out System (ROS) emulated on a PC, via S-Link, i.e.
 - integration test to ROS:
 - PC: Pentium-III, 1 GHz, DAQ/EF-1 ROS software
 - S-Link implementation: DMA, PCI bus
- ▶ Read-out data verification: on ROS (PC)
- ▶ L1A throttle: MUCTPI busy was fed into the CTPD as an external VETO
 - S-Link flow control ripples back as ROD-BUSY through MIROD → MIBAK → MICTP → CTPD

Special thanks to: G. Lehmann, E. van der Bij *et. al*, ROS colleagues

Performance: Level-1 Trigger Latency

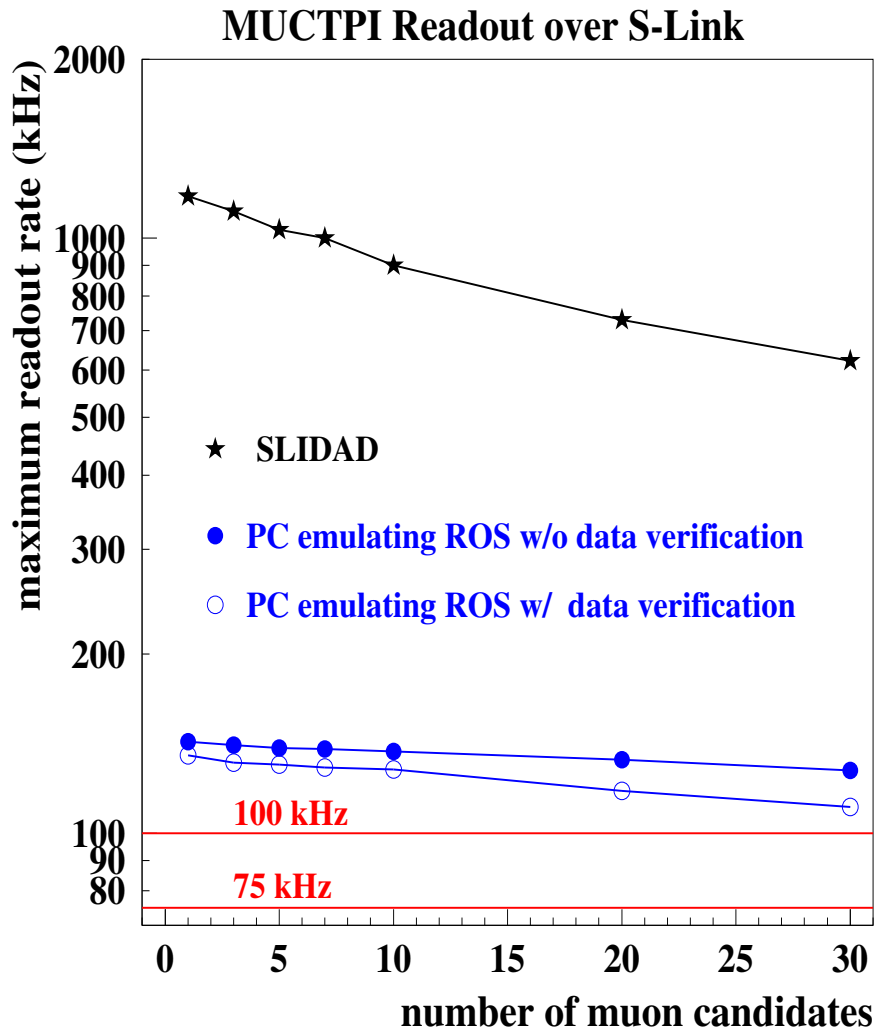


- ▶ Level-1 trigger latency of MUCTPI \equiv “MIOCT IN from SL” to “MICTP mult OUT”
 $\Rightarrow \sim 125 \text{ ns}$ (5 BC clocks) \iff latency budget = 8 BC clocks
 \Rightarrow measured latency fits well in budget
- ▶ c.f. CTP latency \equiv “CTPD mult IN” to “CTPD L1A OUT”
 $\Rightarrow \sim 55 \text{ ns}$ (< 2.5 BC clocks) \iff latency budget = 5 BC clocks
 (this small latency is for the CTP demonstrator that has reduced capability c.f. the final CTP.)



► Read-out latency

- DAQ branch: 1.8 (2.5) μs for 3 (56) μ candidates event
 - Level-2 branch: 1.8 (3.9) μs for 3 (56) μ candidates event
 - For Level-2 br., MIROD sorts candidates in p_T , send up to 12 (max. 16) highest- p_T candidates as RoI information to Level-2
 - For DAQ br., processing in MIROD is simpler
- ⇒ NOTE: Numbers of μ candidates presented here are much larger than expected in normal operation.
- ⇒ Latency: 2 \sim 3 μs for a few μ candidates event in absence of queueing effects
→ fits well in budget



- ▶ Back-pressure VETO mechanism worked
- ▶ Data verification at ROS (PC) showed no error
⇒ ran stably w/o any error over 24 hours
- ▶ Maximum read-out rate: (DAQ branch)
 - SLIDAD (S-Link Infinite Data Drain):
 - ~ 1200 kHz for 1 μ event
 - ~ 650 kHz for 30 μ event
 - ⇒ MUCTPI intrinsic read-out capability
 - PC emulating ROS:
 - ~ 140 kHz for 1 μ event
 - ~ 130 kHz for 30 μ event
 - ⇒ PC emulating ROS limited the read-out rate in the current setup

- ▶ The ATLAS Level-1 Muon to Central Trigger Processor Interface (MUCTPI)
 - receives trigger information synchronously with the 40 MHz LHC clock from all trigger sectors of the muon trigger
 - calculates total multiplicity values for 6 programmable p_T thresholds
 - avoids double counting single muons traversing more than one sector

- ▶ The MUCTPI demonstrator prototype has been produced and subjected to extensive stand-alone tests and integration tests with external systems.
 - trigger latency: 125 ns
 - read-out latency: $2 \sim 3 \mu\text{s}$
 - maximum intrinsic read-out rate: $\sim 1 \text{ MHz}$ for typical events with up to a few μ candidates

- ⇒ The MUCTPI demonstrator prototype is fully functional and fulfils its specification.
- ⇒ The implementation and choice of technologies have been validated.
- ⇒ Some improvements, including enhanced flexibility of the overlap handling, must be included in the final design.