The ATLAS Level-1 Muon to Central Trigger Processor Interface (MUCTPI)

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Abstract

The Level-1 Muon to Central Trigger Processor Interface (MUCTPI) receives trigger information synchronously with the 40 MHz LHC clock from all trigger sectors of the muon trigger. The MUCTPI combines the information and calculates total multiplicity values for each of six programmable p_T thresholds. It avoids double counting of single muons by taking into account the fact that some muons cross more than one sector. The MUCTPI sends the multiplicity values to the Central Trigger Processor (CTP) which takes the final Level-1 decision. For every Level-1 Accept (L1A) the MUCTPI sends Region-of-Interest (RoI) information to the Level-2 trigger and event data to the data acquisition (DAQ) system. Results are presented on the functionality and performance of a demonstrator prototype of the MUCTPI in full-system stand-alone tests and in several integration tests with other elements of the trigger and data acquisition system. Lessons learned from the demonstrator are discussed along with plans for the final system.

I. Muon Trigger System

The ATLAS Level-1 trigger [1] is based on multiplicity information from clusters found in the calorimeters and from tracks found in dedicated muon trigger detectors. The muon trigger detectors are resistive plate chambers (RPCs) in the barrel region and thin-gap chambers (TGCs) in the end-cap and forward region. Coincidences of hits in different layers are used to identify muon candidates. The width of the roads used for the coincidences determines the trigger transverse-momentum threshold of the candidates. An overview of the ATLAS muon trigger is shown in Figure 1.

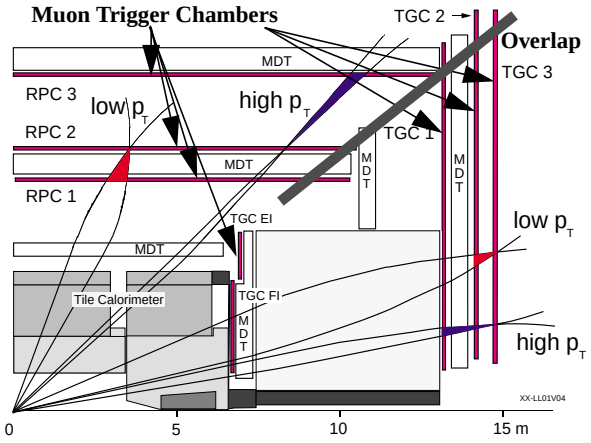

Figure 1: ATLAS Level-1 Muon Trigger

The trigger detectors are segmented into sectors. Each sector can identify up to two muon candidates classified using six programmable p_T thresholds. Detector-specific sector logic sends details of the two highest-p_T candidates in each sector to the MUCTPI [2] which calculates detector-wide multiplicities. Special attention is paid to muons which traverse more than one set of trigger chambers [3]. In particular within the barrel and between the barrel and end-cap regions, muon candidates could be counted twice. Particular attention must be paid to low-p_T muons that are deflected by comparatively large angles in the magnetic field of the toroid magnet. This would lead to an unacceptable rate of fake di-muon triggers and needs to be avoided. Overlap of chamber regions within sectors and between end-cap and forward sectors is handled by the detector-specific logic. There is no overlap in azimuthal angle φ between the octants.

The MUCTPI sends the total multiplicity values for all six programmable p_T thresholds to the CTP which takes the final Level-1 decision. An overview of the muon trigger system is shown in Figure 2.

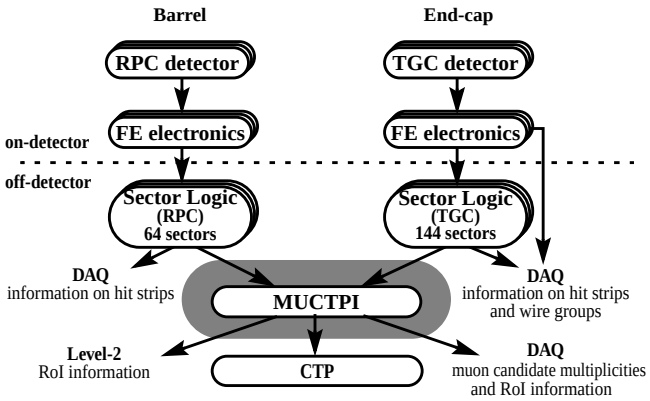

Figure 2: Muon Trigger System Overview

II. Muon to Central Trigger Processor Interface (MUCTPI)

The MUCTPI receives trigger information synchronously for each bunch crossing (BC) of the LHC from all trigger sectors of the muon trigger. It calculates total multiplicity values of muon candidates taking into account the overlap of some of the sectors. It sends the total multiplicity information for each of the six p_T thresholds to the CTP. On reception of an L1A it sends RoI information to the Level-2 trigger and event data to the DAQ system.

The MUCTPI receives 32-bit data words from a total of 208

sectors at a frequency of 40 MHz, corresponding to a total rate of 33 GByte/s. The latency of the multiplicity summation does not exceed 200 ns (8 BCs). The multiplicity value for each threshold is limited to 3 bits, i.e. a maximum value of 7. The MUCTPI accepts L1As up to a maximum rate of 100 kHz and provides data to the Level-2 trigger and the DAQ system. Sufficient on-line monitoring is provided to verify the correct functioning of the MUCTPI.

The MUCTPI consists of several modules. Sixteen Muon Interface Octant (MIOCT) modules each receive the data for one octant in φ and one half of the detector in pseudorapidity η. The Muon Interface backplane (MIBAK) sums the multiplicities of all MIOCTs, provides data transfer and broadcasts timing signals for all modules. The Muon Interface CTP (MICTP) module sends the multiplicities to the CTP and receives timing signals from the CTP. The Muon Interface Read-Out Driver (MIROD) module collects information from the MICTP and the MIOCTs and sends data to the Level-2 trigger and the DAQ system. An overview of the MUCTPI is shown in Figure 3.

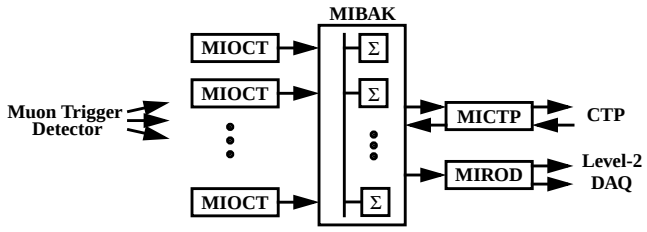

Figure 3: Overview of MUCTPI

A. MIOCT Module

The MIOCT modules receives sector data words synchronously with BC clock from each of 14 sectors. The sectors are assigned to a MIOCT module such that all overlap can be handled by that MIOCT module. There is no overlap between different MIOCT modules.

The 32-bit sector data words each contain information on up to two muon candidates. They are synchronized to the rising or falling edge of the BC clock and the timing can be aligned among the different sectors using programmable delays. The MIOCT module calculates the multiplicities for the six programmable p_T thresholds taking into account the overlap of some of the sectors. The results are sent to the MICTP via the MIBAK backplane. The MIOCT module also stores the sector data words in pipelines. When an L1A is received the corresponding sector data words are read out and sent to the MIROD via the MIBAK backplane. Data for up to two BCs before and two BC after the triggering BC can be included. Empty sector data words can be suppressed. A copy of the data can also be written into a monitoring FIFO which can be read out via VMEbus.

B. MIBAK Backplane

The MIBAK backplane consists of three parts. The first part is an active backplane for the summation of the multiplicities from all 16 MIOCT modules. The second part performs the data transfer from the MICTP and the 16 MIOCT modules to the MIROD module. The third part broadcasts timing signals between the MICTP and all other modules.

C. MICTP Module

The MICTP module receives the total multiplicities and sends them to the CTP. It also stores the multiplicities in a pipeline. When an L1A is received the corresponding multiplicities are read out and sent to the MIROD via the MIBAK backplane. The MICTP module further receives timing signals from the CTP and makes them available on the MIBAK backplane. The timing signals include the BC clock, the bunch counter reset (BCR), the L1A, the event counter reset (ECR), and test signals. It also receives the wired-OR busy line of all modules. This signal is sent to the CTP in order to throttle the generation of L1As should data buffers become full.

D. MIROD Module

When an L1A is received and the MICTP and all MIOCT modules have data available the MIROD module starts the data collection process over the MIBAK backplane. General event information and all muon candidates are extracted. Thresholds are applied to the p_T values of the candidates and sector numbers are mapped to geometrical identifiers. The extracted information is pushed into three processing branches. In the first branch the candidates are sorted in descending order in p_T value, limited in number, and sent as RoI information to the Level-2 trigger if they pass programmable thresholds of p_T value. In the second branch all candidates are sent to the DAQ system. In the third branch events are selected based on different programmable selection algorithms and are written into a monitoring FIFO which can be read out via VMEbus.

III. Demonstrator Prototype Implementation

A demonstrator prototype of the MUCTPI has been implemented. One MICTP, two MIOCTs and one MIROD have been built as $9U \times 400$ mm VMEbus modules. Several emulator cards for the remaining MIOCT modules have been built as $9U \times 60$ mm cards. The MIBAK backplane has been built and mounted in the J3 position of a 9U VMEbus crate. A photo of the demonstrator is shown in Figure 4.

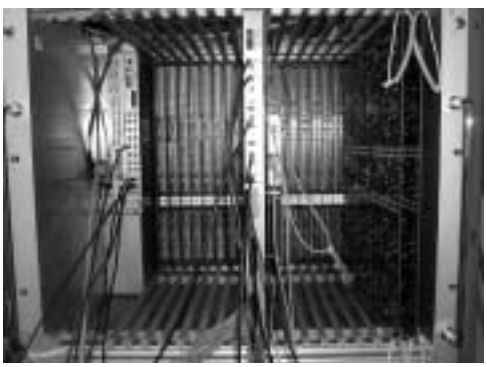

Figure 4: MUCTPI Demonstrator

A. MIOCT Module

The MIOCT modules have been built using programmable logic devices [4]. For a full description of the MIOCT module see Reference [5]. The reception of data from the detector-specific logic is carried out using LVDS receivers. The relative phase of one bit of each sector data word is measured using the CERN/EP/MIC TDC32 chip [6]. Test memories implemented in embedded memories of the FPGAs responsible for receiving the data, are used to provide test data. Synchronization and alignment of data, calculation of overlap conditions, and summation of multiplicities are carried out using several FPGAs and CPLDs, as well as SRAMs used as look-up tables. The control of the TDC and the programming of the CPLDs are achieved using JTAG. A CPLD-based VMEbus controller gives access to the on-board resources using VMEbus A32 D16/D32 data transfers.

B. MIBAK Backplane

The multiplicity summation on the MIBAK backplane has been implemented using CPLDs [4]. The data transfer from the MICTP and from the MIOCTs to the MIROD is implemented using Bus LVDS (BLVDS). Signal integrity studies have been carried out for this part of the system in order to validate the design before construction. Cadence SigXplorer has been used with help from CERN/IT/CE/AE group [7]. The timing signals are transferred between the MICTP module and all other modules using positive ECL signal level. Hardmetric connectors of 2-mm type with five columns and shielding are used to connect all modules to the MIBAK backplane.

C. MICTP Module

The MICTP module has been implemented using programmable logic devices [4]. For a full description of the MICTP module see Reference [8]. The relative phase of the incoming signals is measured using the CERNM/EP/MIC TDC32 chip [6]. The phases of the internal clocks are adjusted using the CERN/EP/MIC PHOS4 chip [9]. Test memories, control of read-out and pipelines for read-out data are implemented using several FPGAs. External FIFOs are used for storing data for read-out to the MIBAK and for monitoring. A CPLD-based VMEbus controller gives access to the on-board resources using VMEbus A32 D16/D32 data transfers.

D. MIROD Module

The MIROD module has been implemented using programmable logic devices [4]. For a full description of the MIROD module see Reference [10]. The MIROD module uses FPGAs for the implementation of a token passing protocol, the data extraction and data processing in the three different branches. Play-back memories implemented in SRAM for the MIBAK data and in embedded RAM for the MIBAK control can be used to emulate the functioning of the MIBAK backplane. S-Link [11] is used for the transfer of data to the Level-2 trigger and to the DAQ system. The event formatter for the Level-2 trigger and the DAQ system uses the ATLAS Read-Out Driver (ROD) event format [12]. The design file is written using VHDL and can be used in RODs for other sub-detectors [13]. The MIROD module can be used in MIBAK analyser mode in which the MIBAK signals are recorded into the muon candidate FIFO. The S-Link controller contains an optional analyser FIFO which allows the storage of data words and control data in real-time. The FIFOs can be read out through VMEbus. An FPGA-based VMEbus controller implements VMEbus A32 D16/D32 data transfers. The MIROD module can generate a VMEbus interrupt when one of its FIFOs reaches a programmable watermark.

IV. Tests and Results

A. Software and Test Programs

Test software has been developed for the VP PMC/P34 VMEbus single-board computer from Concurrent Technologies [14], running the Linux operating system in kernel version 2.2.12. The test software is written in C++ and uses the VMEbus library of the ATLAS Read-Out System (ROS) [15] for VMEbus master mappings. The library allows one to read and write single words in A32 D16 and D32 mode. The test software allows one, in particular to generate and down-load test data into the test memories of the modules, to configure the modules, to read out the monitoring FIFOs and to verify the data. Data generation and verification are interfaced to the ATLAS simulation software [16]. An interface to the ATLAS run control [17] still needs to be developed. A TTCvi module [18] was used to generate the necessary timing signals, in particular BC, BCR, and for some tests also the L1A.

B. Results of Module Tests

Before integrating the MUCTPI system, all modules were tested individually by down-loading data into the test memories and reading out the monitoring FIFOs.

- MIOCT Module:

The phase measurement mechanism for the sector data was verified to work correctly. Differences of phase between sector inputs of ± 1 ns can be measured. The clock dispersion between different sectors on the MIOCT module is of ± 1 ns. The relative timing alignment between different sectors works correctly for latency differences of up to 400 ns (i.e. 16 BCs). Using more than 10^5 different sets of random test data, the overlap handling and multiplicity summing was verified to work according to specification. The read-out of data, including zero suppression, was verified to work correctly.

- MICTP Module:

The phase measurement mechanism for the timing signals was verified to work correctly with a precision of ± 1 ns. The timing signals can be aligned correctly with respect to the BCR and L1A signals. Using the test memory to input the multiplicities, the read-out of the MICTP module was verified to work correctly.

- MIROD Module:

Using the play-back memories, the token protocol for the MIBAK backplane was verified to work correctly. The data

extraction and data processing in the three different branches of the MIROD work correctly, in particular the ordering and selection of a limited number of muon candidates in the Level-2 branch, and the event selection mechanism in the monitoring branch. Using an S-Link infinite data drain (SLIDAD) [11] and fewer than ten muon candidates in the test memories, the MIROD could provide data at a maximum rate of 1 MHz to both, the Level-2 trigger and the DAQ system.

C. Results of Full-system Tests

After testing the modules individually, the full MUCTPI was tested by down-loading test data into the test memories of the MIOCTs and by reading out the monitoring FIFOs of all the modules, in particular of the MICTP and of the MIROD.

The timing alignment of the different modules was verified to work correctly by using test data which correlates data content and timing with respect to BCR and L1A. The pipelines for read-out after L1A in the MIOCTs and the MICTP were found to be sufficient but will be extended for the final system to give improved flexibility to cope with unexpected increases of the L1A latency. Systematic long runs of two days with 10^5 different sets of test data were made to verify the multiplicity summation, the correct data collection over the MIBAK backplane, and the correct data processing in the MIROD for the Level-2 trigger and the DAQ system.

D. Results of External Integration Tests

Integration tests with other parts of the ATLAS T/DAQ system were performed in a pairwise fashion as the modules became available.

- Sector Logic:

Input to the MIOCT modules was tested using the barrel sector logic demonstrator [19] and the end-cap sector logic prototype [20]. The sector logic modules were programmed to provide data to the MIOCT in a repeated and cyclic way. The phase of the data was measured with a precision of about 0.8 ns. The data can be latched stably in a window of about 20 ns with either the rising or the falling edge of the internal clock of the MIOCT. The latching windows overlap by about 10 ns, which means that data can be latched safely given that the skew is small. The data integrity was tested in a systematic long-term test of almost 48 h. Not a single error was detected in about 10^9 events generated. This is equivalent to a bit error rate of better than about 10^{-10}.

- CTP demonstrator:

The output of the MICTP to the CTP was tested using the CTP demonstrator [21]. The phase of the data was measured at the input of the CTPD with a precision of about 1.5 ns. The latching of the data was verified to be correct in a window greater than 20 ns. The internal clock of the CTPD can be moved in order to latch the data safely given that the skew is small. The data were verified to be correct by capturing them in CTPD monitoring FIFO.

- Level-2 Trigger:

The output of the MIROD to the Level-2 was tested using the Region-of-Interest Builder (RoIB) demonstrator . Some problems were identified concerning the implementation of the S-Link in the RoIB, as well as concerning internal data buffering in the MIROD. After fixing these problems, rates of RoI fragments sent from MIROD to the RoIB of up to 100 kHz without data verification could be sustained. The data were verified to be correct at the Level-2 supervisor processors which received the data at the output of the RoIB.

- DAQ System:

The output of the MIROD to the DAQ system was tested using a desk-top PC emulating the ROS . Rates of event fragments sent from MIROD to ROS of up to 100 kHz could be sustained using a simple data receiving program. The limitation of the rate arises from the S-Link reception in the PC which uses DMA and the PCI bus. Using the emulated ROS functions rates of up to 35 kHz were measured. In this case the limitation of the rate arises from the performance of the CPU in the PC. The correctness of the data was verified in long runs of several hours.

E. Overall Performance

The overall performance of the MUCTPI was measured using the fully integrated MUCTPI, the CTPD, a PC emulating the ROS, and a TTCvi generating the timing signals. The CTPD was used to generate the L1A based on multiplicities received from the MUCTPI. The busy signal of the MUCTPI was used by the CTPD to throttle the generation of L1As. Some signals were measured directly on the modules using an oscilloscope.

- Level-1 Trigger Latency:

Using the test memories in the MIOCTs and adding the observed latency for sector data latching, the total Level-1 trigger latency of the MUCTPI was measured to be 125 ns (i.e. 5 BC). This is well within the allowed budget.

- Read-out Latency:

The latency between the L1A arriving at the MICTP and the data being available in the MIROD on the S-Link to the Level-2 trigger or the DAQ system was measured. Using zero suppression in the MIOCTs and test data containing three muon candidates, the read-out latency for the Level-2 trigger and the DAQ is about 1.8 μs. Using data containing 56 muon candidates, the latency for the Level-2 trigger increases to about 3.9 μs. In this case the RoI information sent to the Level-2 trigger was limited to contain 12. The limit on the number of candidates is a programmable parameter of the MIROD that can be adjusted in the range up to 16. For the same test data, the latency for the DAQ increases to about 2.5 μs. This value is lower than for the Level-2 trigger due to the simpler processing. All latency values are well within the allowed budget.

- Read-out Rate:

Using the busy signal of the MUCTPI to throttle the generation of L1As by the CTPD, test data containing between one and 30 muon candidates could be sent to a SLIDAD on the DAQ branch of the MIROD with rates between about 1100 and 620 kHz, respectively. The same tests data could be sent to a

PC emulating the ROS with rates of about 130 kHz. This rate is higher than the one quoted in Section IV.D. because of a faster PC being used, but it is still limited by the DMA and the PCI bus. All read-out rates for numbers of muon candidates between one and 30 are within the allowed budget. In the experiment typically only very few muon candidates are expected.

V. Conclusion

The MUCTPI demonstrator prototype has been successfully implemented, tested and integrated with other parts of the ATLAS Trigger/DAQ system. The MUCTPI demonstrator prototype works according to specification.

The MUCTPI introduces a Level-1 trigger latency of 125 ns. The read-out of the MUCTPI, providing data to the Level-2 trigger and to the DAQ system, introduces a read-out latency of about 2 to 3 μs for events with around ten muon candidates. Read-out rates of up to between about 1100 and 620 kHz can be sustained for events with fewer than 30 muon candidates if the ROS is assumed to be always free. Using a PC emulating the ROS, rates of about 130 kHz were measured.

Although it was originally envisaged as a demonstrator prototype, the MUCTPI described in this paper already provides essentially all the functionality and performance required by ATLAS. The main aspect were improvement is needed is the handling of sector overlap where greater flexibility and programmability is required.

VI. Acknowledgments

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- The ROS group, in particular G. Lehmann, and for the help with S-Link E. van der Bij.

VII. References

[1] ATLAS Collaboration, First-level Trigger Technical Design Report, CERN/LHCC/98-14, June 1998.

[2] A. Corre et al., A Demonstrator for the ATLAS Level-1 Muon to Central Trigger Processor Interface (MUCTPI), Proc. 6th Workshop on Electronics for LHC Experiments, Cracow, Poland, 11-15 September 2000, CERN/LHCC/2000-041.

[3] P. Farthouat, Interfaces and Overlaps in the Level-1 Muon Trigger System, ATLAS EDMS note ATL-DA-EN-0001.

[4] The MUCTPI modules mainly use Altera Max7000S and Flex10K devices, http://www.altera.com.

[5] http://edms.cern.ch/item/CERN-0000003738.

[6] http://micdigital.web.cern.ch/micdigital/tdc32.htm.

[7] http://product-support.web.cern.ch/product-support/electronicscae.html.

[8] http://edms.cern.ch/item/CERN-0000004008.

[9] http://micdigital.web.cern.ch/micdigital/Thomas/Delay-chip%20SpecificationsV1.pdf.

[10] http://edms.cern.ch/item/CERN-0000003747.

[11] http://hsi.web.cern.ch/HSI/s-link/.

[12] C. Bee et al., The Event Format in the ATLAS DAQ/EF Prototype -1, ATLAS DAQ note ATLAS-DAQ-98-129, Version 2.0, March 2002.

[13] http://home.cern.ch/schwick/vhdl/AtlasRODFormatter/index.html.

[14] http://www.gocct.com.

[15] http://atlasinfo.cern.ch/Atlas/GROUPS/DAQTRIG/ROS/ros.htm.

[16] http://atlas.web.cern.ch/Atlas/GROUPS/SOFTWARE/OO/architecture/General/index.html

[17] http://atlas-onlsw.web.cern.ch/Atlas-onlsw/.

[18] P. Gallno, TTC-VMEbus Interface (TTCvi), http://ttc.web.cern.ch/TTC/intro.html.

[19] V. Bocci et al., The Sector Logic Demonstrator of the Level-1 Muon Barrel Trigger of the ATLAS Experiment, Proc. 7th Workshop on Electronics for LHC Experiments, Stockholm, Sweden, 10-14 September 2001, CER/LHCC/2001-034;

K. Nagano et al., Report of the Dataflow Integration Test of the Barrel Muon Trigger Sector Logic Demonstrator and the Muon-CTP-Interface, ATLAS EDMS note ATL-DA-TR-0003, October 2001.

[20] R. Ichimyia et al., An Implementation of the Sector Logic for the Endcap Level-1 Muon Trigger of the ATLAS Experiment, these proceedings;

R. Ichimiya et al., Report of the Integration Test between the Endcap Muon Trigger Sector Logic and the Muon-CTP-Interface, ATLAS EDMS note ATL-DA-TR-0004, January 2002.

[21] G. Schuler (RD27 Project), Central Trigger Processor Demonstrator, ATLAS EDMS note ATL-DA-ER-00005, November 2000.

[22] R.E. Blair et al., A Prototype RoI Builder for the Second Level Trigger of ATLAS Implemented in FPGAs, Proc. 5th Workshop on Electronics for LHC Experiments, Snowmass, Colorado, 20-24 September 1999, CERN/HCC/1999-033;

J. Dawson et al., Report on the Dataflow Integration Test of the Muon-CTP-Interface and the RoI Builder, ATLAS EDMS ATL-DA-TR-0001, February 2001.

[23] G. Lehmann et al., The ATLAS DAQ/EF Prototype -1 as Testbeam Data Acquisition System, Proc. IEEE-NPSS Real Time Conference 2001, 4-8 June 2001, Valencia, Spain;

G. Lehmann et al., Report on the Dataflow Integration Test of the Muon-CTP-Interface and the Read-out System, ATLAS EDMS note ATL-DA-TR-0002, May 2001.