Radiation-Hard ASICs for Optical Data Transmission in the ATLAS Pixel Detector

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Abstract

We have developed two prototype radiation-hard ASICs for optical data transmission in the ATLAS pixel detector at the LHC: a driver chip for a Vertical Cavity Surface Emitting Laser (VCSEL) diode for 80 Mb/s data transmission from the detector, and a Bi-Phase Mark decoder chip to recover the control data and 40 MHz clock received optically by a PIN diode. During ten years of operation at the LHC, the ATLAS optical link circuitry will be exposed to a maximum total fluence of 10^{15} 1MeV equivalent n/cm^2. We have successfully implemented both ASICs in 0.25 μm CMOS technology using enclosed layout transistors and guard rings for increased radiation hardness. We present results from recent prototype circuits and from irradiation studies with 24 GeV protons up to 57 Mrad.

I. Introduction

The ATLAS pixel detector [1] consists of three barrel layers and three forward and backward disks which provide at least three space point measurements. The low voltage differential signal (LVDS) from the pixel detector is converted by the VCSEL Driver Chip (VDC) into a single-ended signal appropriate to drive a Vertical Cavity Surface Emitting Laser (VCSEL). The output current of the VDC is to be variable between 0 and 20 mA through an external control voltage, with a standing current of roughly 1 mA to improve the switching speed of the VCSEL. The rise and fall times of the VCSEL driver current are required to be less than 1 ns and the duty cycle of the VDC output signal should be (50 +/- 4)%. In order to minimize the power supply noise on the final chip carrier board, the VDC should also have constant power consumption.

The optical signal from the VCSEL is transmitted to the Readout Device (ROD) via a fiber. The 40 MHz beam crossing clock from the ROD, bi-phase mark (BPM) encoded with the command signal to control the pixel detector, is transmitted to a PIN diode via a fiber. Figure 1 shows an example of a BPM encoded signal. It is derived from the 40 MHz beam crossing clock by sending only every second transition.

In the absence of command 1 bits, this results simply in a 20 MHz clock. Any 1 bits in the command (or data) stream are encoded as extra transitions in the middle of a 25 ns period.

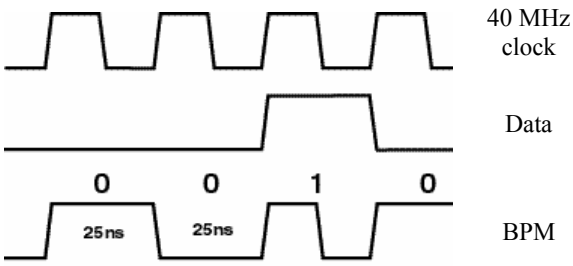

Figure 1: Example of a BPM encoded signal

This BPM encoded signal, received by a PIN diode, is decoded using a Digital Opto-Receiver Integrated Circuit (DORIC). The DORIC's recovered clock and data (or command) signals are in LVDS form. Figure 2 shows a simple block diagram of the DORIC circuit. The amplitude of the current from the PIN diode is expected to be in the range from 40 to 600 μA. The 40 MHz clock recovered by the DORIC is required to have a duty cycle of (50 +/- 4)% with a total timing error of less than 1 ns. The bit error rate of the DORIC circuit is required to be less than 10^{-11} at end of life.

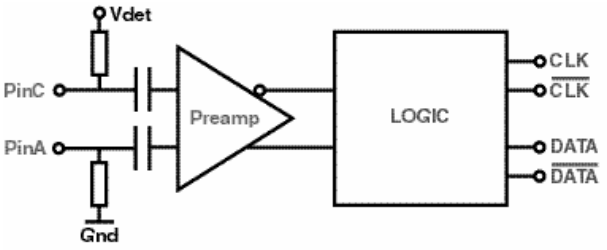

Figure 2: Simple block diagram of the DORIC circuit

To ensure that the DORIC logic locks into the correct recovered clock frequency, it needs to be trained over a

certain time period. The specs currently allow for a 25 µs time period, during which a continuous string of data 0 bits is being sent, which is simply a 20 MHz clock at the DORIC input. The clock recovery circuit derives a leading edge from each input transition. Trailing edges are locked to the leading edges via internal voltage controlled delays. This 40 MHz recovered clock is the input to a delay locked loop which adjusts the internal delays until a 50% duty cycle is reached. The circuit is then ready to decode data bits. After having locked into the correct frequency, the clock recovery circuit is blind to any extra transitions near the middle of the 25 ns intervals, and will continue to decode the clock correctly even in the presence of data 1 bits.

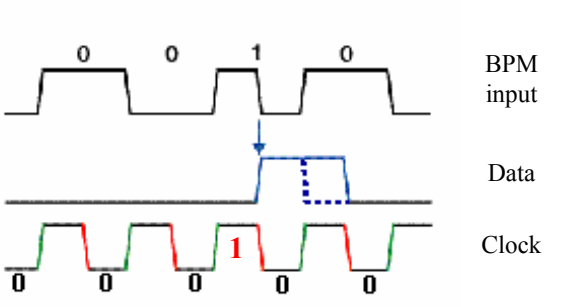

Figure 3: Data recovery procedure of DORIC logic

The data recovery circuit uses each input transition to latch the state of the recovered clock just prior to the current transition into a flip-flop (see Figure 3). For data 0 bits, the recovered clock is always in a low state prior to each input transition. When a data 1 bit is present however, the recovered clock is in a high state just prior to the input transition. The thus decoded data 1 bit is then stretched to make it more stable (see dotted and solid data 1 bit in Figure 3).

II. VDC AND DORIC DESIGN HISTORY

The pixel detector design of the VDC and DORIC takes advantage of the development work for similar circuits [2] used by the outer detector, the SemiConductor Tracker (SCT). Both SCT chips attain radiation-tolerance by using bipolar integrated circuits (AMS 0.8 micron BICMOS) and running with high currents in the transistors. These chips are therefore not applicable for the higher radiation dosage and lower power budget requirements of the pixel detector.

We have implemented the VDC and DORIC circuits in standard deep submicron (0.25 µm) CMOS technology. Employing enclosed layout transistors and guard rings [3], this technology promises to be very radiation hard.

Four deep submicron prototype runs of the VDC and DORIC circuits have been received between summer of 2001 and summer 2002. The most recent deep submicron submission of the VDC and DORIC also includes four channel versions of both circuits.

III. RESULTS FROM RECENT DEEP SUBMICRON SUBMISSIONS

Over the course of the four submissions, the VDC's total current consumption has been reduced and the current consumption between the bright and dim states of the VCSEL diode have been made more constant. The VDC circuits from the second and third submission meet the specifications with rise and fall times below 1 ns. Since the final VCSEL arrays will be of common cathode type, the latest submission of the VDC circuit was made compatible with these arrays. In Figure 4 we show the VCSEL current generated by the VDC from the latest submission as a function of the external control current I_{set}. The current was measured with 10 Ohms in series with the VCSEL, which partially explains the early turnover of the current at high values of I_{set}. We note that the VDC circuit from the third submission (compatible with common anode VCSEL arrays) achieved 20 mA VCSEL current. The output current of the latest VDC design therefore still needs to be improved.

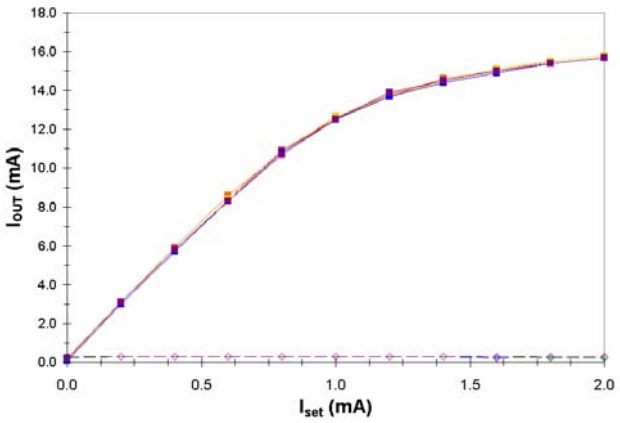

Figure 4: VCSEL current vs. I_{set} of the latest VDC circuit

We also observe that the dim current of this latest VDC circuits needs to be increased to roughly 1 mA. Further, we observe fairly balanced current consumption on the latest VDC circuits, and find that the duty cycle of the output signal is within specs. However, the rise and fall times of the output signals are in the range from 1.0 ns to 1.4 ns over the operating range of the circuit. Since the VDC needs to be compatible with common cathode VCSELs, the switching of the current into the VCSEL is now performed by pFETs instead of nFETs. Clearly, the speed of the pFET switching circuitry still needs to be improved.

In the DORIC circuit, a feedback loop with a large time constant was added to fully cancel the offsets at its differential gain stage which vary from chip to chip. Further, the gain of the differential pre-amp was lowered and the layout carefully examined to minimize the coupling of digital signals into the pre-amp.

In the third deep submicron submission, the differential pre-amp was replaced by a single-ended pre-amp. This allows for the PIN diode to be biased directly, keeping the up to 10 V high bias voltage off the DORIC chip. Both versions of the pre-amp allow the DORIC circuit to decode control data and clock correctly down to PIN diode currents of roughly 25 μA, meeting the requirement of PIN current thresholds below 40 μA. The duty cycle and timing errors of the recovered 40 MHz clock are also within specifications. In Figure 5 we show the duty cycle of the recovered clock, measured on DORICs from the third submission. We conclude that 9 out of 11 examined DORIC circuits meet the specs with duty cycles within (50 +/- 4)%.

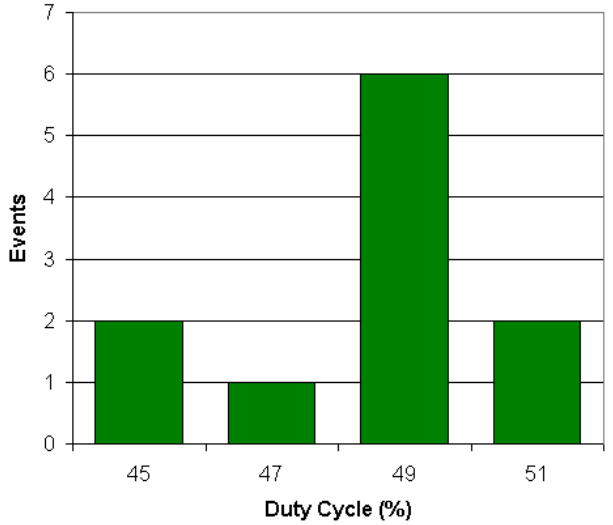

Figure 5: Duty cycle of recovered clock in the DORIC circuit's third submission

In the latest submission, the pre-amp circuit was optimized for common anode PIN arrays. The delay control circuit was improved to center the recovered clock duty cycle closer at 50% and a reset was added for slow and controlled recovery of the clock decoding circuit. All improvements to the circuitry were successfully tested. After this submission, we learned that the DORIC pre-amp will need to be compatible with common cathode PIN arrays. This will require one more round of optimizations to the DORIC's pre-amp circuitry.

IV. Irradiation Studies

We have irradiated 13 DORICs and 13 VDCs from the first 0.25 μm submission with 24 GeV protons at CERN in September 2001 up to a dosage of 50 Mrad. We observed no degradation in the amplitude and clock duty cycle of the output of the VDC. For the DORIC, the PIN current threshold for no bit errors remained constant except for one die which required a much higher threshold one month after the irradiation. It was unclear whether the observed degradation on one chip was due to radiation or mishandling.

In August 2002, we irradiated VDC and DORIC circuits from the latest deep submicron submission in the same proton beam at CERN. In a so-called cold box setup, we performed electrical testing of single channel VDC and DORIC circuits. For the 10 tested DORIC circuits we observed that the PIN current thresholds remained constant at 12 μA up to the total dose of 57 Mrad. For the 8 tested VDC circuits we found the bright and dim VCSEL currents to be constant throughout the irradiation. The duty cycle of the output signals increased by roughly 2% after 57 Mrad, which is acceptable.

We also irradiated two opto-boards which are hybrid boards containing complete optical link chains. In Figure 6 we show an opto-board fully populated with four-channel DORIC and VDC chips as well as PIN arrays and VCSEL arrays. Bit error test boards in the control room send BPM signals over optical fibers to the PIN arrays on the opto-boards. The DORIC circuits decode the BPM signals and the recovered data and clock is being routed to the VDC chips on the other side of the same opto-board. The VDCs then drive the VCSEL arrays and the optical signals are being returned to the control room. The returned (decoded) signals are compared to the signals which were originally sent out, and bit errors are counted. The two opto-boards were irradiated up to a total dose of 23 Mrad. After each 4 to 6 Mrad of accumulated dose, the VCSEL arrays were allowed to anneal for 12 to 22 hours while being driven with 20 mA.

We observed that the PIN current thresholds for no bit errors are of order 8 to 10 μA and remain constant up to the total dose of 23 Mrad. We have also monitored the optical power returned from the opto-board to the control room over the course of the irradiation. We were able to observe a general trend during the irradiation: after an irradition period, the returned optical power usually decreased; after the VCSEL annealing period, the optical power usually increased, as expected. The variations from this general rule are most likely due to inconsistencies in the quality of the optical connections which had to be made for each measurement of the optical power. In future irradiation tests, we plan to improve on the quality and repeatability of the optical connections. We observed that the returned optical power from the opto-board decreased by less than 50% after the total dose of 23 Mrad.

An additional opto-board, populated with single channel DORIC and VDC chips, was irradiated up to a total dose of 32 Mrad. The results from this board are similar to the results obtained with the two opto-boards described above.

V. Summary

We have developed prototype circuits of the VDC and DORIC in deep submicron (0.25 μm) technology using enclosed layout transistors and guard rings for improved radiation hardness. The prototype circuits meet all the requirements for operation in the ATLAS optical link and further appear to be sufficiently radiation hard for ten years of operation at the LHC.

REFERENCES

[1] ATLAS Pixel Detector Technical Design Report, CERN/LHCC/98-13.

2] D.G. Charton et al, "System Tests of Radiation Hard Optical Links for the ATLAS Semiconductor Tracker," Nucl. Instr. and Meth. A443, 430 (2000).

[3] G. Anelli et al, "Radiation Tolerant VLSI Circuits in Standard Deep Submicron CMOS Technologies for the LHC Experiments: Practical Design Aspects," IEEE Trans. on Nucl. Sci., Vol. 46, No. 6, 1690 (1999).

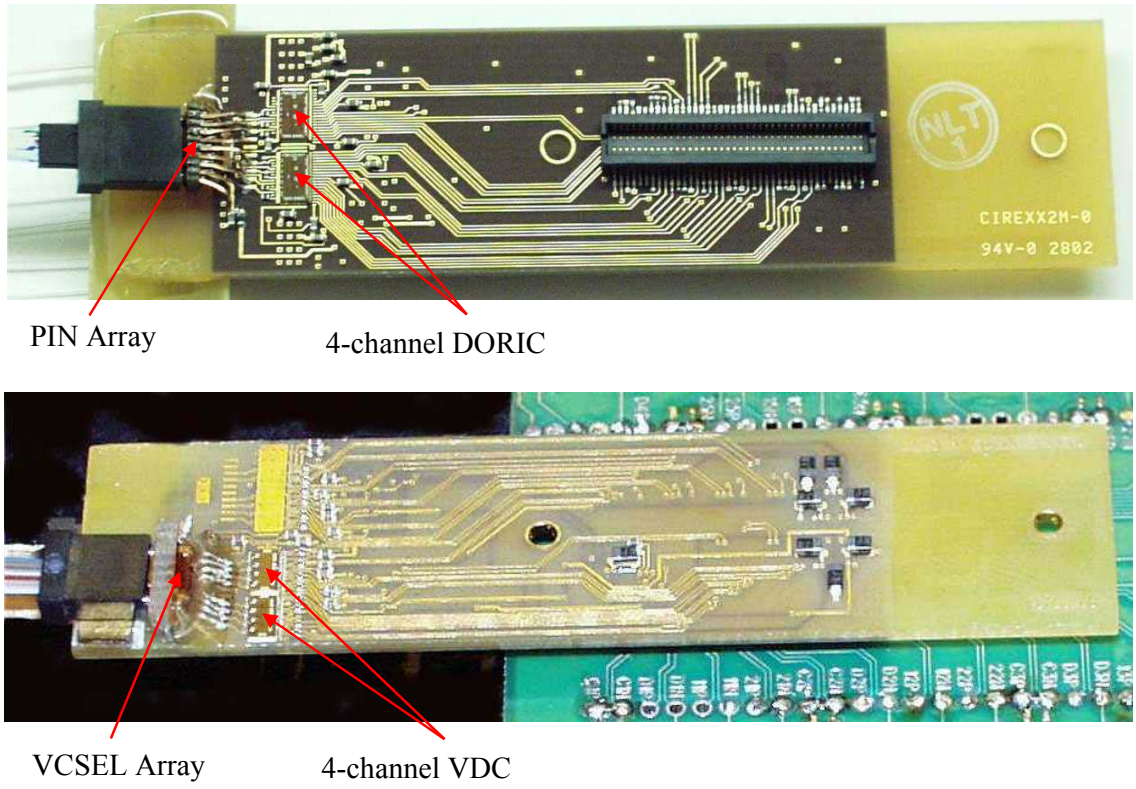

Figure 6: Fully populated opto-board for irradiation study