Status Report of the ATLAS SCT Optical Links

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for

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Abstract

The readout of the ATLAS SCT and Pixel detectors will use optical links, assembled into harnesses. The final design for the barrel SCT opto-harness is reviewed. The most recent radiation tolerance studies are described. Test results from the first pre-series opto-harness are summarised. Results are given for the new 12 way VCSEL and PIN arrays to be used for the off-detector opto-electronics. Mechanical and cooling issues are addressed.

I. INTRODUCTION

Optical links will be used for the readout of the ATLAS SCT detectors [1]. Each detector module has an associated opto-electronic board containing 2 data transmitters running at 40 Mbit/s and one receiver. Optical links are used to transmit incoming timing, trigger and control (TTC) signals from readout drivers (RODs) in the experimental cavern to the front-end electronics and to transmit data signals from the front-end electronics to the RODs. The RODs encode the control signals using a BPM12 ASIC, coupled to a VCSEL array. The data signals are received at the RODs using a p-i-n diode array coupled to a DRX12 ASIC.

Each detector module uses two data fibres and one TTC fibre. Biphase mark encoding is used to send 40 Mbit/s control signals along with a 40 MHz clock down the single TTC fibre; the optical signals are received by a p-i-n diode and decoded by DORIC chips. Data in electrical form from the front-end chips is used to modulate two VCSELs by means of a VCSEL driver chip (VDC). The architecture of the links is shown in Fig.1.

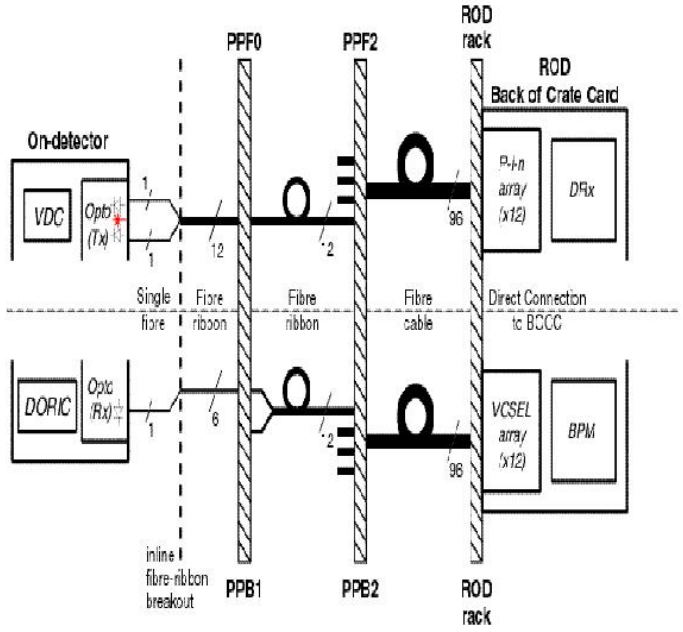

Figure 1. SCT links architcture.

Single optical links are combined into harnesses, which each use six opto-packages. An opto-package contains one p-i-n diode and two VCSELS. The fibres from the opto-packages are combined into ribbons, terminated in MT connectors. They then form an assembly in conjunction with the flat cables taking the electrical power to the silicon modules and front-end electronics. Each detector module is served by an opto-flex cable, which carries the opto-package, VDC and DORIC, with connectors to interface to the module and to the power cables. Fig.2 shows part of a barrel harness; the fibres run in furcation tubing, which may be seen entering the opto-packages. The VDC and DORIC chips lie beneath the cover next to the opto-packages and the connectors at the top of the picture mate with silicon detector modules.

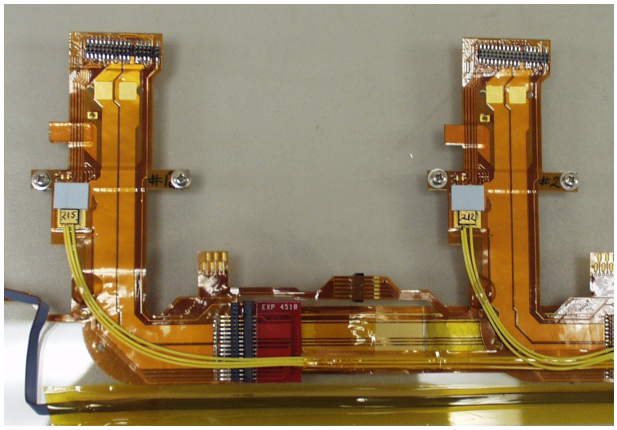

Figure 2. SCT barrel harness

II. TOTAL DOSE RADIATION HARDNESS

VCSELS

Truelight TSD-8A12 GaAlAs VCSELs will be used for the SCT opto-links, although other VCSEL types been investigated previously.

Degradation in VCSELs is dominated by displacement damage, increasing the number of non-radiative recombination centres. These dominate the recombination rate below threshold at low levels of irradiation and the net effect is to increase the threshold current [2]. Damage to VCSELs has been observed to anneal out during use by injection annealing [3]; this has been attributed to local heating and/or recombination assisted migration of defect centres.

Twenty Truelight VCSELs were irradiated using 30 MeV protons at INER, Taiwan. A typical flux of 2×10^{10} $cm^{-2}s^{-1}$ was used for the irradiations, up to a fluence of 2×10^{14} cm^{-2}; this is 40% higher than the worst case expectation in the SCT, using NIEL scaling to normalise for the expected particle energy spectrum incident on GaAs.

The light output of the VCSELs versus forward current was recorded before irradiation, after irradiation and after injection annealing [4]. Injection annealing was carried out for 168 hours at a drive current of 10 mA, followed by 168 hours at 20 mA. It will be possible to run the VCSELs at up to 20 mA in the SCT in order to make use of injection annealing. The VCSELS were biased during the irradiation.

A degradation of laser threshold and a decrease in slope efficiency was observed after irradiation; nevertheless, significant recovery occurred after annealing. The lasers remain within the operating specification for the optical links after the irradiation and annealing. A linear fit was performed to the data from the 20 VCSELs and the results are presented in Table 1.

Parameter	**Mean Value**
Threshold current pre-irradiation (mA)	3.28 ± 0.09
Slope efficiency pre-irradiation (μW/mA)	180.5 ± 9.6
Increase in threshold current post-irradiation (mA)	2.98 ± 0.39
Ratio of slope efficiency before/after irradiation	0.73 ± 0.04
Increase in threshold current after irradiation & 10mA anneal (mA)	0.94 ± 0.11
Ratio of slope efficiency after irradiation & 10mA anneal to pre-irradiation value	0.88 ± 0.03
Increase in threshold current after 20mA anneal cf. pre-irradiation value (mA)	0.42 ± 0.13
Ratio of slope efficiency after 20mA anneal to pre-irradiation value	0.98 ± 0.03

Table 1. VCSEL proton irradiation results

Other links components

Centronic p-i-n diodes will be used; neutron irradiations were performed at RAL, UK and proton irradiations at CERN. Full details are given elsewhere [5].

The responsivity was typically 0.5 A/W before irradiation, falling to 70% of this value after a fluence of 0.25×10^{14} neutrons cm^{-2} (1MeV,Si) and staying at this level up to 1×10^{15} cm^{-2}. The dark current increase after irradiation was negligible compared to the expected signal size.

Accelerated ageing was carried out, leading to a prediction of a maximum of 6 failures during the 10 year lifetime of the SCT.

The integrated circuits used in the optical links have been produced in the AMS 0.8 micron BiCMOS process, which is not radiation qualified. Conservative design was used to minimise radiation effects. Only npn bipolars are used, being run at high current densities to minimise the effect of radiation-induced changes. The circuit itself was designed to be insensitive to changes in the small-signal current gain. Care was taken with the chip layout and the area of the active devices was kept small to maximise the energy deposition required to cause single-event upset (SEU).

Irradiations using reactor neutrons were performed in Ljubljana, Slovenia and the chips were ^{60}Co gamma irradiated at the University of Birmingham, UK.

A batch of VDC chips was exposed to a 10 Mrad (Si) ionising dose and a neutron fluence of $3\times10^{14}cm^{-2}$ (1MeV,Si), whilst DORIC chips received 50 Mrad (Si) and a fluence of $2\times10^{14}cm^{-2}$ (1MeV,Si). No degradation in performance was observed.

An accelerated ageing study was performed on irradiated DORIC chips, which predicted a maximum of 0.3 % failure in 10 years. Full details of these studies are presented in [6].

Chips from each wafer to be used in production are now undergoing qualification for radiation hardness; at present no failures have been observed.

Separate radiation damage and ageing studies have been performed on the optical fibre, low-mass power tapes and passive components. A complete functional opto-flex

assembly was proton-irradiated at CERN and its behaviour was as expected from the studies of individual components.

III. SINGLE EVENT UPSET

The TTC links send clock and command signals down a single fibre. The p-i-n diode converts the optical input to electrical form and the DORIC chip recovers the bunch crossing (BC) clock and the command signals. Our previous study at PSI [7] using 405 MeV/c pions showed that incident particles could cause a signal in the p-i-n diode sufficiently large to introduce errors in the recovered command signals. The worst case error rate measured was found to correspond to a fraction of lost module data of 9×10^{-4} in the SCT, which is considered negligible.

Depending on the time of arrival of the incident particle relative to the BC clock, an error may also be introduced in the clock signal itself, causing clock edges to appear early by up to 6.25ns. This can result in a loss of synchronisation between the front-end ABCD chips driven by the optical link concerned and those in the rest of the detector.

This effect was investigated in a 24 GeV/c proton beam at the CERN PS. A forward hybrid was placed in the beam and read out using an optical link, whilst a reference barrel module was placed in the counting room, being read out electrically. An L1 trigger was sent, followed by a beam spill and further L1 triggers. At each trigger, the BC count was recorded, so that an SEU would result in a mismatch between that of the test and that of the reference system.

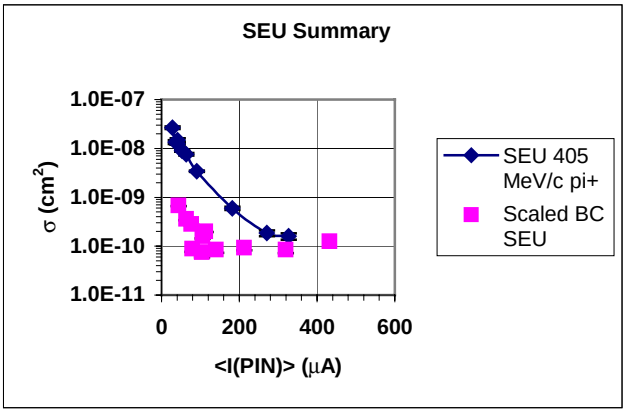

Figure 3. SEU in command signals and BC clock

The cross section for SEU was defined as the number of errors per unit particle fluence. The BC counter SEU cross section is shown as a function of p-i-n diode current (hence light level) in Fig.3, where the PSI results are also shown for comparison. The BC SEU cross section is much smaller than cross section for bit errors in the command signal, demonstrating that the ABCDs are rather insensitive to clock jitter. Assuming that an SEU causes loss of synchronisation until the next BC counter reset, the fraction of lost module data due to this source has been calculated to be 7.8×10^{-5}.

IV. VCSEL AND P-I-N DIODE ARRAYS

The off-detector opto-electronics will be based on 12-way arrays of VCSELs and epitaxial silicon p-i-n diodes. The VCSELs are at present of the same type as used for the on-detector opto-packages but the packaging will be based on selecting and cutting 12-way arrays from the VCSEL wafer. It is expected that future arrays will use the brighter oxide-confined VCSELs from the same manufacturer. The chip is attached to a PCB, which is equipped with precision holes for MT guide pins as shown in Fig.4. The VCSEL chip is die bonded onto the PCB and wire bonds used to make electrical connections to the VCSELs. The MT connector is attached using the guide pins and a latch is used to retain the connector.

A similar packaging approach is to be used for the 12 way p-i-n diode arrays.

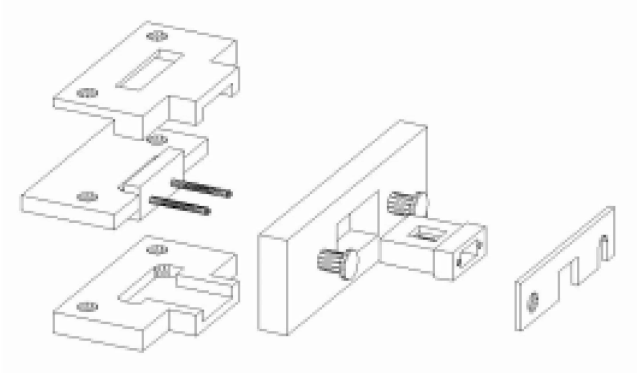

Figure 4. VCSEL array packaging.

V. BPM-12 AND DRX-12

The off-detector opto-ASICs are the BPM-12 and DRX-12. The DRX-12 chip is a simple 12 channel discriminator. Each channel receives the electrical signal from one of the channels of the PIN diode in the array. Each channel has an adjustable threshold and provides an LVDS output. The BPM-12 chip receives the 40 MHz BC clock and 12 streams of command data. It uses biphase mark encoding to encode the data for each channel onto the clock. A simple VCSEL driver output is used to drive each channel of the VCSEL array. The BPM-12 chip can adjust the amplitude and delays for the output signal. It also has the capability to adjust the mark-space ratio of the output signal.

These chips are manufactured in the AMS 0.8 um BiCMOS process. The production wafers have been produced and testing is underway [8].

An oscilloscope trace showing the optical output from a Truelight 12-way VCSEL array driven by a BPM-12 chip is given in Fig.5. The data sent was a stream of ones, leading to a 40 MHz signal.

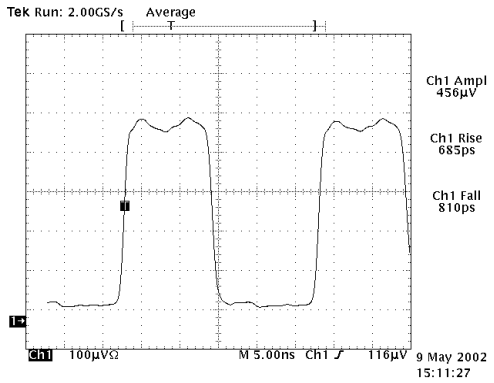

Figure 5. VCSEL array driven by BPM-12

VI. TEST RESULTS FROM PRE-SERIES HARNESS

During the construction of the SCT, the harnesses will be assembled by Radiantech Inc., Taiwan. They will be tested at all stages in production. They will be shipped to RAL, UK, where they will be tested before and after assembly to the SCT barrels.

The first pre-production series harness has been received at RAL and is undergoing testing. Electrically it is fully functional apart from one missing clock output. All the optical links work correctly. The performance of the 12 harness VCSELs is shown in Fig.6; they were operating with a 50% duty cycle during this measurement. The p-i-n diodes had a mean responsivity of 0.44 A/W, in a range of 0.40 to 0.46 A/W.

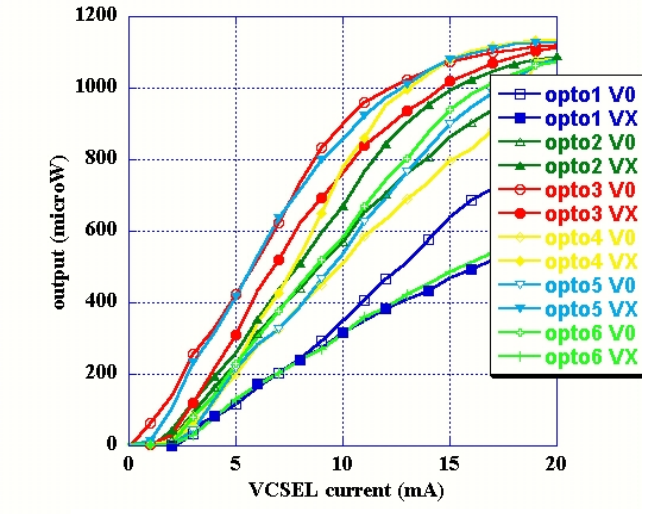

Figure 6. VCSEL LI curves

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The bit error rate (BER) of the links in the harness was measured using a sequencer module to provide a pseudo-random input, an optical interface module (OptIF) [9] and a LITMUS [10] module to compare the data sent with that retreived for both data and TTC links. The BER is defined as the fraction of the bits sent which return corrupted. All links in the first pre-series harness have now been tested for periods in excess of 12 hours with no errors, leading to an upper estimate of the BER of 6×10^{-13}, which may be compared to the specified maximum value of 1×10^{-9}.

VII. MECHANICAL MODELLING OF CLEARANCES

The harnesses will be installed between the surface of the support structure, a carbon fibre barrel, and the detector modules. The modules are supported away from the barrel surface by carbon fibre brackets. The space available for the harnesses is severely constrained and the opto-flex cables must follow the bracket shape to reach from the barrel surface to the module connector.

The inner end of each opto-flex cable lies on top of the stack of (up to 5) power tapes, the precise stack thickness depending on position. The opto-flex must have sufficient compliance to absorb the differing stack heights. In addition, the barrel structure may exhibit some eccentricity. This is compensated for in the machining of the pads upon which the brackets are mounted, resulting in differences of up to 1mm in the distance between the barrel surface and the module connector from module to module. These differences must also be tolerated by the opto-flex.

A jig representing a section of the barrel and one bracket was used to simulate a worst case scenario (Fig.7). The maximum permissible error on the barrel diameter and the maximum number of tapes acting together to push the opto-package upwards towards the silicon module were used. An aluminium mock-up of the silicon module was mounted and the clearances estimated using slip gauges. The most critical clearance was that between the upper surface of the opto-package or ASIC cover and the lower surface of the module. This was measured to be 1.40+/-0.05mm, in good agreement with the design value.

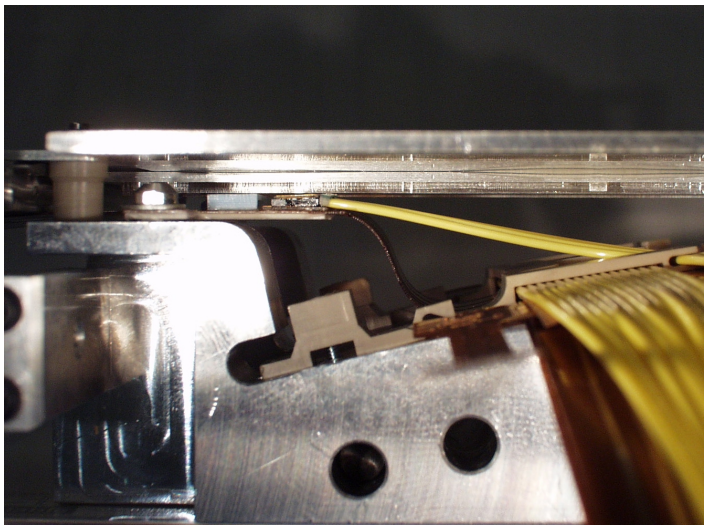

Figure 7. mechanical model showing clearance between chip cover and Si module

VIII. THERMAL BEHAVIOUR

The lifetime of the VCSELs and p-i-n diodes in the opto-package depends on their temperature. The most significant

sources of heat on the opto-flex cable are the ASICs, which together liberate around 0.4W and determine the opto-package temperature. Although the VCSELs are subject to self-heating, all lifetime studies were done on packaged devices. Thus, the VCSEL temperature quoted is the package temperature. It is desirable that this temperature should not exceed 10°C. Thus, solder-filled vias conduct heat away from the ASICs through the opto-flex, to an AlN stiffener on its lower side, which conducts heat towards the module cooling block.

A finite-element analysis (FEA) of the heat transfer through the opto-flex was carried out. The temperature drop between the cooling pipe and the ASICs due to conduction alone was predicted to be around 25°C. This was then compared with measurements made using a resistor glued on an opto-flex cable and used as a heater. Several Pt100 sensors were used to record the temperature at different points on the opto-flex and data recorded as a function of ambient temperature (Fig.8, where the temperature drop between the pipe and opto-package is dT1+dT2+dT3). As the ambient temperature decreases, more heat is lost to the environment; the FEA corresponds to the case where such heat loss is zero. At an ambient temperature of -5°C, a temperature drop of around 20°C was recorded over the opto-flex, which is reasonably close to the expectation from the FEA. For the environmental and coolant temperatures in the SCT, a temperature close to 0°C is predicted for the opto-package. This allows a good margin for error.

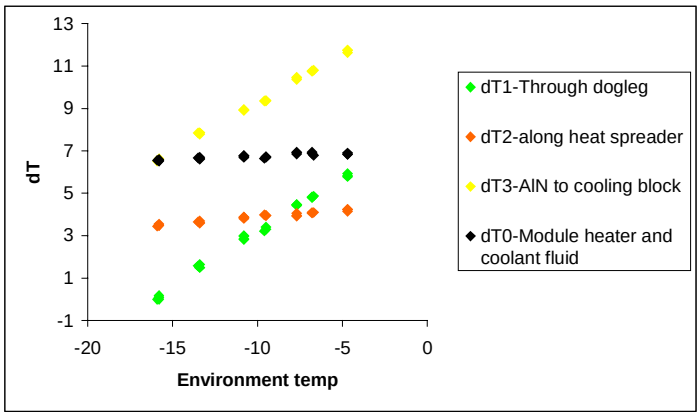

Figure 8. temperature drops over different sections of the opto-flex

IX. SOME SYSTEM TEST RESULTS

Extensive tests have been performed with up to 15 SCT modules mounted on a prototype carbon fibre sector and with earlier prototypes of the SCT barrel opto-harnesses [11]. These results showed that the measured module noise was the same as the noise measured with the individual modules on an electrical test stand. Many studies of the grounding and screening have been performed in order to minimise the immunity to noise injection.

One unexpected but important result was the discovery that there were significant light leaks into the silicon detector from the fibres. The fibres near the opto-package are contained in a 900 µm diameter furcation tubing. The tubing selected was rather transparent at 850 nm and the light leaking out of the fibres, caused a significant increase in the silicon detector leakage current and noise.

Samples of furcation tubing were set up containing fibres carrying light at 850nm; they were coiled tightly to maximise the escape of light and measured with a large area photodiode. The light power escaping was significant on some samples but was close to zero for black tubing, which will now be used exclusively for production.

X. CONCLUSIONS

The bulk of the development work for the SCT optical links is now complete.

The links optical and electronic components have been shown to be sufficiently radiation-hard with respect to total dose and single event effects.

The lifetime of these components will be more than adequate if they are cooled below room temperature. It has therefore been necessary to ensure that heat can be transferred away from the active components.

Mechanical issues have been resolved by a combination of careful computer and physical modelling.

The first industrially-made harness has now been received and forms part of a small pre-production series which will be used to refine the manufacturing process before full-scale production begins.

XI. ACKNOWLEDGEMENTS

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XII. REFERENCES

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