# Design and Performance of the CMS Pixel Readout Chip

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## *Abstract*

Readout chips for pixel detectors at LHC are exposed to enormeous fluence rates that are in the range of $2 * 10^7$ particles per second and cm$^2$. The architecture of a pixel readout chip must be chosen such, to have minimal data losses even at these large data rates. The CMS pixel readout chip is based on a Column Drain Architecture that should have the necessary performance. We present the design and measured performance of the CMS pixel chip in DMILL technology. The measurements in a high rate LHC-like testbeam will be shown, where the data losses of a bump-bonded pixel chip as a function of particle fluence has been studied.

## I. Introduction

The CMS pixel detector system consists of 4 end disks and up to 3 barrel layers [1]. In figure 1 a sketch of a barrel module is shown. A sensor [2] of the size 6.450x1.604cm$^2$ is bump-bonded to 16 readout chips PSI43 which are glued to a Si-baseplate. In front of each chip 6 capacitors can be seen, which are needed for on-chip voltage regulators. A three layer capton HDI, which is glued on top of the sensor, distributes the signal and power lines throughout the module. The comunication is controlled by a token bit manager chip (TBM), which is bonded to the HDI.

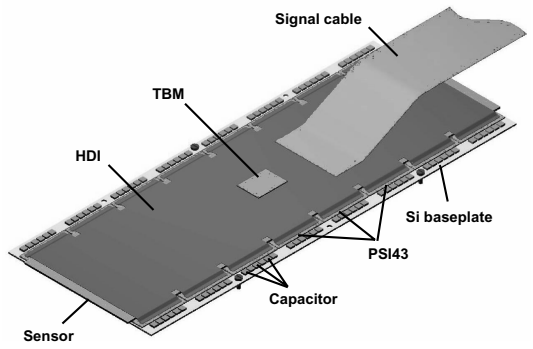


Figure 1: CMS pixel barrel module

The innermost layer is positioned at a distance of 41 to $45\ mm$ from the beam line. At high luminosity LHC running condition, this corresponds to a particle track rate of up to $25\ MHzcm^{-2}$ and a mean pixel multiplicity per track of 5.
In section two a chip architecture is presented that should be able to handle such high rates. The basic principle is presented in sub section A. The implementation in the radiation hard DMILL technology is explored in sub section B where it is compared to the lab measurements. Section three presents a high rate pion beam test setup (A) and shows some of its results (B).

## II. CMS Pixel Readout Chip

### *A. Column Drain Architecture*

The goal of the so called column drain architecture is to store pixel hits in a columnwide buffer, where a suppression of not trigger confirmed hits is performed. The CMS pixel readout chip has three distinct parts: the pixel array, the double column periphery and a control and interface block. They are described in the following.
The pixel array consists of 52x53 pixel unit cells (PUC) which are organised in 26 double columns (DC). Each PUC contains a charge preamplifier which is bump-bonded to the sensor and an adjustable comparator which sets a hit flip flop. The outputs of all hit flip flops in a DC build up a hard wired $OR$ signal. This signal is processed in the DC periphery.

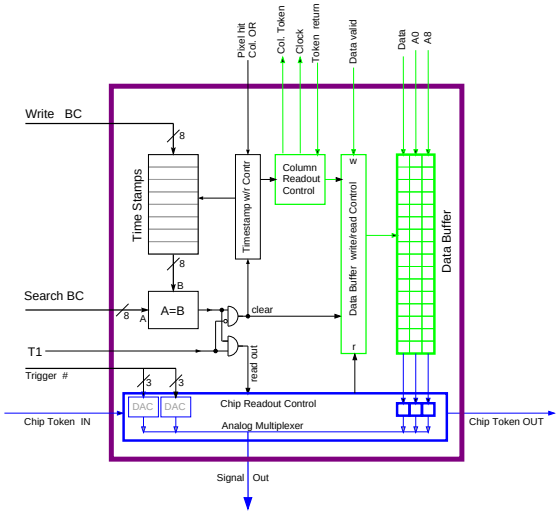


Figure 2: Schematic view of the double column periphery

A schematic view of the DC periphery is shown in figure 2. The appearance of the afore mentioned column $OR$ initiates two tasks: the value of a 40 MHz gray code counter (WBC) is written to a time stamp buffer and the address and analog pulse height of the hit pixels are copied to the periphery and

stored in a data buffer. The data are kept there for the L1 trigger latency: the time stamps are compared to a second gray code counter (SBC), which runs parallel to the WBC with an offset corresponding to the L1 latency. If there is an equality between a stored time stamp and the SBC value, the system checks, whether an external trigger signal is active. If not, the corresponding data buffer is cleared. Otherwise the DC is marked ready for beeing read out. No new pixel hits are accepted in this DC, until the event is read out. The readout is controlled by a token bit, which goes from DC to DC.
The control and interface block contains 6 voltage regulators, 21 DACs which provide the chip with adjustable voltages/currents, a 4 phase clock generator, an I$^2$C like programming interface and LVDS line drivers/receivers. It is explained more detailed in the next sub section.

## *B. DMILL Implementation and Lab Measurements*

The CMS pixel readout chip has been implemented in the DMILL technology. It is a radiation hard, 0.8$\mu m$ SOI process used in several HEP or space instrumentations. In the rest of this section some aspects of particular interests will be elaborated.

### *1) On-chip voltage regulators*

The PSI43 chip uses 6 different on-chip voltage regulators. This allows the analog and digital voltages to be programmed. In addition the digital voltage supply is split into 3 separate parts with its own regulators: one for the LVDS driver/receivers and clock generator, one for the DACs and one for the digital core components. That way we seperate components with strongly fluctuating current consumption from the more critical parts. This strongly reduces cross coupling effects and noise.
Figure 3 shows the response of the voltage regulators to a load current step from 28 to 39 $mA$. The regulated output voltage is 4.5 $V$ with a drop out of 500 $mV$. Shown is the change of the output voltage as a function of time for different external filter capacitors. The output impedance is $\approx 800\ m\Omega$.

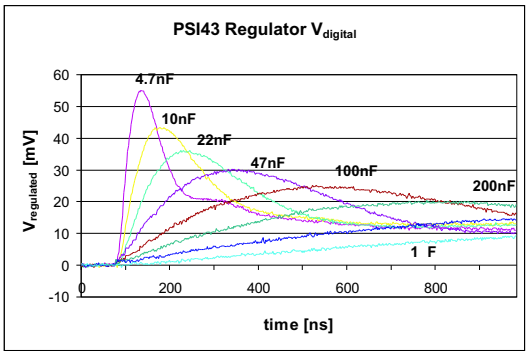


Figure 3: Response to current step for different filter capacitors

Figure 4 shows the supply voltage regulation as a function of the frequency. The input voltage has an AC component of 100 $mV$. Plotted is the AC component of the regulated voltage for different external filter capacitors.
The regulator works up to $\approx 500\ kHz$. For higher frequencies the external capacitors are needed. For the CMS pixel modules the use of several hundred $nF$ is planned.

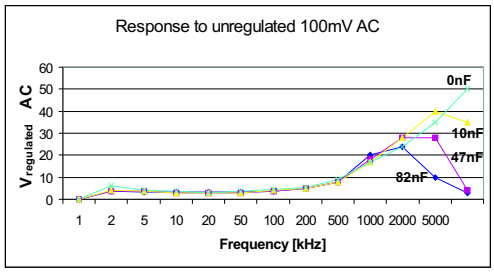


Figure 4: Power rejection for different filter capacitors

### *2) Modified I$^2$C programming interface*

A programming interface is needed to program the DACs, pixel trims, pixel/column masking, pixel calibration, trigger latency and the readout frequency (40/20 MHz). An I$^2$C like interface has been chosen, with modifications done to allow much higher speed. This is needed to program the large amount of pixel trims within a reasonable time. The operating frequency is now 40 MHz. The price for speed is the abandonment of a full handshake and the read back possibility. The later is compensated partially by an extra clock cycle in the event readout structure (see point 4). A burst mode had been introduced to program the pixel trims sequentially without sending the individual addresses.

### *3) On-chip generation of calibrate pulses*

There is a possibility to send calibrate pulses to the preamp input. This is an extremely usefull feature to setup the readout chain and for diagnostic reasons. The pulses are coupled to the input via a 1.6 $fF$ capacitor. They are generated on the chip with a programmable (8-bit) pulse height (equivalent to 0 to 40000 electrons) and a 8-bit delay within a range of 45 $ns$. Pixels can be enabled row/double column wise.

### *4) Event structure and address encoding*

The PSI43 readout chip generates the following event structure: a 3 clock cycle long header followed by a 6 clock cycle long block for each pixel. The first cycle in the header is an ultra black, which is needed for the separation of the individual chips in the module event readout structure. It is followed by a black and the analog status of the last addressed DAC. Figure 5 shows an event header for 5 different settings of a DAC. In the 3rd cycle we can see the actual state of the last addressed DAC. This is also a very fast check for the proper working of the I$^2$C programmming during prototype testing.
The header is followed by a 6 cycle data structure for each pixel, containing the DC/pixel address and the analog pulse

height. The address bits are analog encoded. The pixel address has 5 levels, the DC address 6.

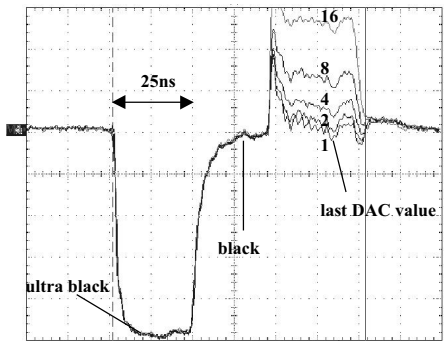


Figure 5: Readback of last addressed DAC

Figure 6 shows the overlay of 5 single pixel hit readouts. The DC address is the same for all 5 events, while the row address has 5 different LSBs. There is the 3 cycle header, followed by the MSB and LSB of the DC address, the 3 pixel address bits and the pulse height. Two things have been observed: 1) the analog address encoding works quite fine. The levels are well separated and allowed a robust decoding. 2) There are, however, relatively large level shifts in the pixel address among different DCs. This could be tracked down to a bad matching of (undersized) transistors. Although this is not a fundamental problem and can be calibrated away, it will be improved in future readout chips.

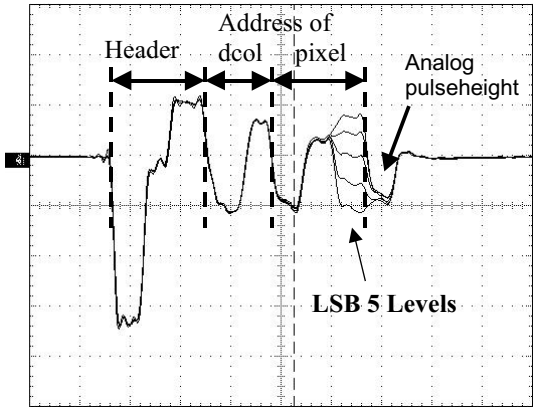


Figure 6: Event readout structure

*5) Performance of the pixel analog block*

The pixel unit cell has a two stage charge amplifier. The typical peaking time is around 23 $ns$ with an analog power consumption of 40 $\mu W$ per pixel (including comparator). The intrinsic noise is measured to be 120 $e^-$. A sensor leakage current of $> 10\ nA$ can easily be accepted at the input. The output is fed to a comparator whose threshold can be adjusted globally and has a 3 bit local trim capability. Figure 7 shows the time when the comparator flips as a function of the injected charge. For a threshold of $2500\ e^-$ we observe a timewalk of $23\ ns$, which is marginal.

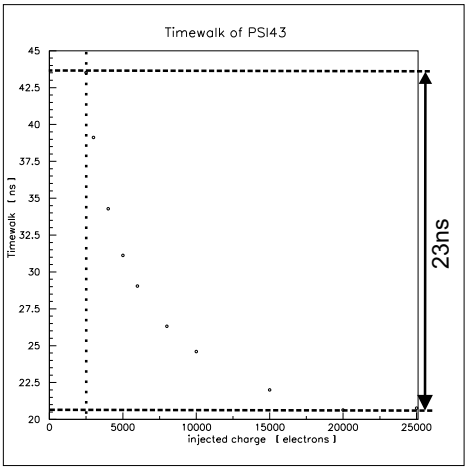


Figure 7: Time walk of the pixel unit cell

## III. High Rate Test Beam

### A. Test Setup

We have tested the PSI43 readout chip under LHC rate conditions. The performance has been investigated in a pion beam at the Paul Scherrer Institut in Villigen, Switzerland. We used 300 $MeV/c$ pions with a fluence of up to $\approx$ 35 $MHz/cm^2$ and a beam profile of 10/20 $mm$ FWHM in $x/y$. The beamline had a 50 $MHz$ structure.

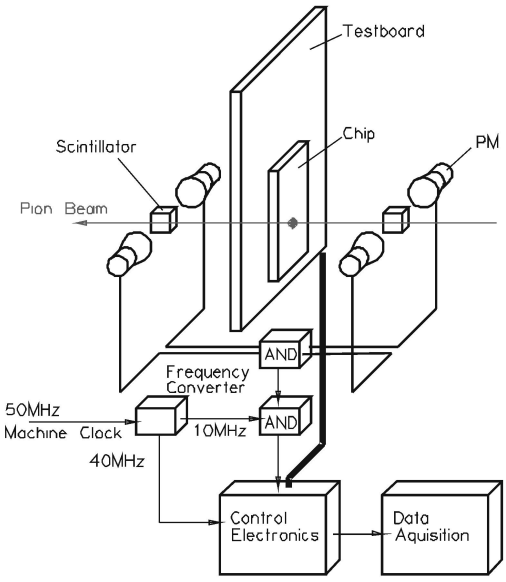


Figure 8: Beam test setup

Figure 8 shows the test setup. We have build a beam telescope with 2 very small scinillators (2x2x2 $mm^3$). They have been read out with 4 PMTs which were brought into coincidence. Because of the 50 $MHz$ beam structure, every $5^th$ bunch crossing coincides with every $4^th$ clock cycle of the 40 $MHz$ clock and can be used for trigger confirmation and eventual read out. This has been achieved by syncronizing the PMT coincidence output with a 10 $MHz$ clock deduced from the 50 $MHz$ machine clock. Two independent control electronic setups have been used to minimize systematic effects.

## *B. Test Results*

Some problems have been encountered in the testbeam setup in operating at 40 $MHz$. The speed was limited by the data buffer mechanism to 36 $MHz$, since the chip was operating at a temperature of $\sim$ $45^o$C. Simulations have shown, that one loses $\sim$ 15% in speed compared to nominal operating temperatures of $-5^o$C in CMS. For our test setup this problem could be solved by providing a slightly asymmetric clock at 40 $MHz$.
Figure 9 shows the analog pulse height distribution for a single pixel. The sensor thickness is 280 $\mu m$. Also shown are the distributions for two runs with calibrate pulse injects for an equivalent of 16000 and 33000 $e^-$ respectively.

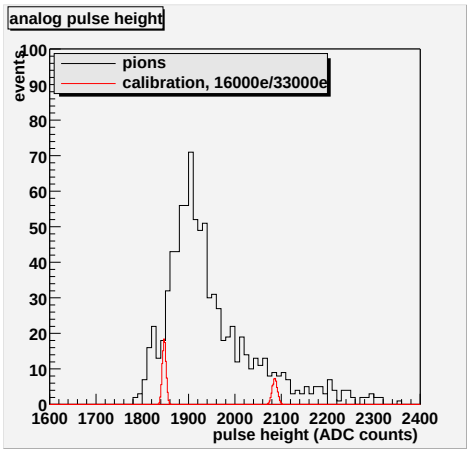


Figure 9: Analog pulse height distribution

The timing of the readout can be seen in figure 10. The efficiency is plotted versus the bunch crossing BC number. As can be seen, the efficiency at the nominal BC (numbered 0) is 98%. One observes a spill over to the next BC of 2% due to time walk. One should mention here that the pion bunch has a width of 4.6 $ns$, which adds to the time walk of the chip. In one measured chip we observed 14% efficiency at BC+5, which we explain by an overshoot of the preamp/shaper system due to an incorrect adjustment of the feedback transistors that resulted in too much differentiationof the pulse. Aside from this the background was at the expected level for a track rate of 1.1 (14) $MHz/cm^2$ for chip 2 (chip 1).

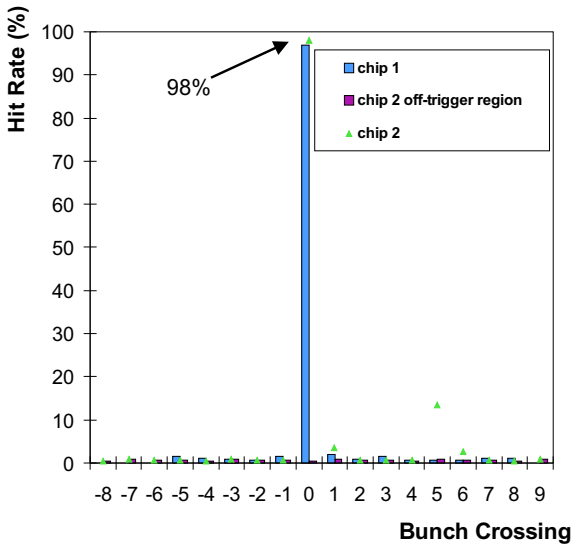


Figure 10: Timing

The architecture is per design not completely deadtime free. Data losses as a function of fluence rate have been simulated for the test beam. As can be seen in figure 11, the dominating contribution comes from the column drain setup. That means that a DC doesn't accept a hit if the same DC was hit one BC before.

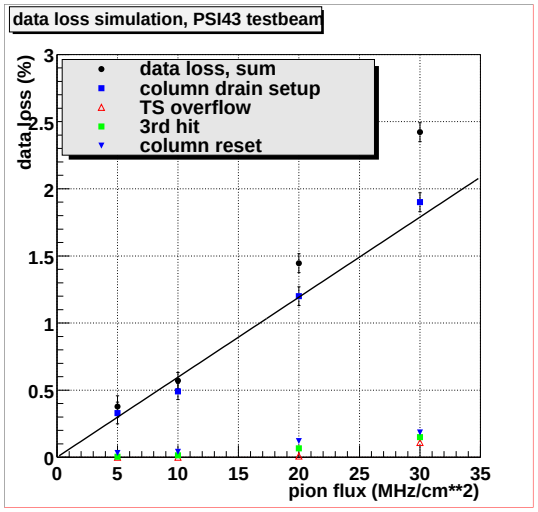


Figure 11: Simulated data loss

In that case the data loss rate should approximately coincide with the random hit rate (i.e. for an off-BC region). This could be confirmed in the measurement and is shown in figure 12. Other contributions to the data loss are: time stamp overflow, non acceptance of a 3 $^{rd}$ hit while the column drain mechanism is active and the reset of a DC after it has been read out, which leads to a loss of history of around 3 $\mu s$.

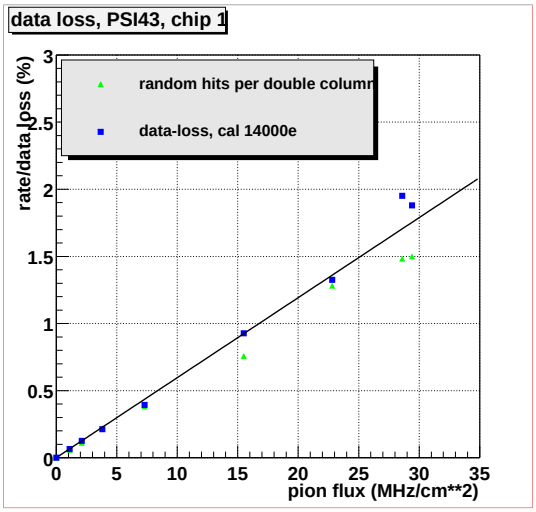


Figure 12: Measured data loss and random hit rate

Figure 13 shows the detection inefficiency as a function of the pion fluence. The upper most curve corresponds to detection of physical tracks with a threshold of 3000 $e^-$. The inefficiency of 2% at low rates can be explained by the spill over into the next bunch crossing as explained earlier. The lower two curves show the data loss for calibration pulse injects with two different thresholds. The chip was fully exposed to the beam, so that there were reallistic activities in the chip. The slope of the curves with the same threshold are in good agreement.

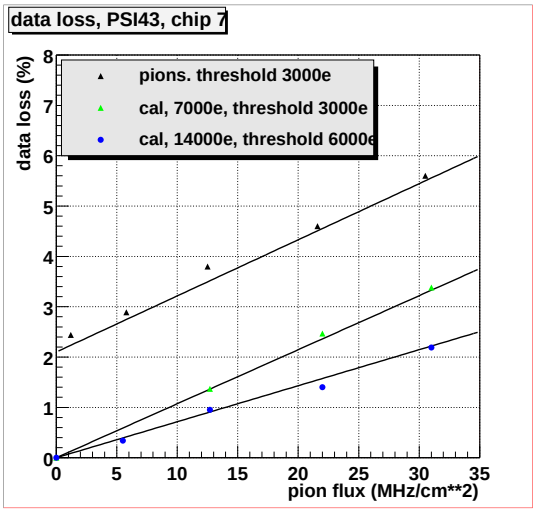


Figure 13: Detection efficiency verus particle fluence

Finally we measured the single event upset (SEU) rate in the pixel mask bit. It is a minimal sized flip flop with a power supply of 4.5 $V$. Starting with all pixels masked we exposed the chip during $6^1/_2$ hours to the beam with a mean fluence of 18 $MHz/cm^2$. Of a total of 2756 pixels 17 (0.6%) responded after the irradiation. The pixel map for the accumulated data is shown in figure 14. From this one calculates a SEU cross section of

$$\sigma = (1.5 \pm 0.4)\dot{1}0^{-14}\ cm^2. \quad (1)$$

This is compatible with earlier measurements done at PSI [3].

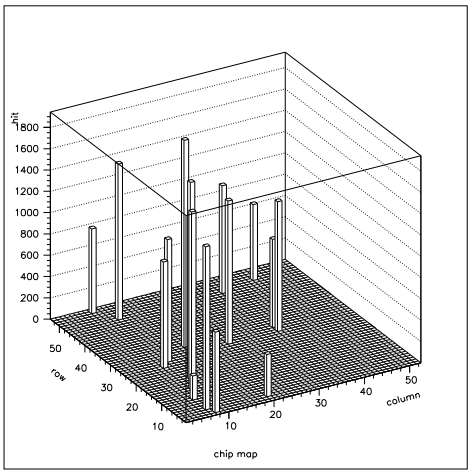


Figure 14: Single event upsets in mask flip flop

## IV. Conclusion and Outlook

The first complete readout chip for the CMS pixel detector in DMILL has been produced and tested in the lab and in a high rate LHC-like test beam. Basically the chip is fully functional. There are a few minor limitations like the speed and the time walk, which are marginal.

The translation of the chip into a 0.25 $\mu m$ CMOS process has been started. This will allow to reduce the pixel size to $100x150$ $\mu m$. To avoid the problem of the address level shifts, we will implement a digital internal address encoding.

## V. References


[1] CMS Tracker Project, Technical Design Report, CERN/LHCC 98-6, chapter 2

[2] *Sensor development fot the CMS pixel detector*, G. Bolla et al., Nucl. Instr. and Meth. A485 (2002) 89-99

[3] *Pion Induced Single Event Upset in the CMS Pixel Detector Readout*, M. Barbero et al., CMS Note 2000/036