Performance of the Beetle Readout Chip for LHC*b*

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Abstract

This paper presents the design and first measurements on the version *1.2* of the *Beetle* chip.

The *Beetle* is a 128 channel pipelined readout chip which is intended for the silicon vertex detector, the inner tracker and the pile-up veto trigger of LHC*b*. In case of multianode photomultiplier tubes being used for the RICH readout, it is foreseen also to use the *Beetle*.

Section II. gives a short overview of the chip architecture whereas section III. shows first measurements on the *Beetle 1.2*. In section IV. the results from a Total Ionizing Dose (TID) irradiation test is summarized, while an outlook on further tests given in section V.

I. Introduction

The development of the *Beetle* readout chip started in late 1998. Since this time the *Beetle* chip family has grown up to 3 complete readout chips (*Beetle 1.0*, *1.1* and *1.2*) and 8 chips with different test structures and prototype components.

Caused by a layout error, *Beetle 1.0* had to be patched with a focused ion beam to become functional. *Beetle 1.1* fix this bug among others but still a few problems remain:

- Peaking time of the front-end is too slow: $t_{peak} > 27$ ns
- Signal remainder 25 ns after peak is to large
- Maximum input charge rate is small for the expected occupancy
- Digital circuits are not robust against Single Event Upset

Featuring a new front-end, the successor version *Beetle 1.2* now fulfills all LHC*b* specifications. In addition the digital control circuitry is also robust against SEU.

II. Chip Architecture

The *Beetle* [1] is an analogue pipelined readout chip and implements the RD20 front-end architecture [2]. For a fast trigger decision it provides a comparator with prompt binary output signals. Using the comparator output signals instead of analogue front-end signals, the *Beetle* can alternatively operate in a binary pipelined mode. Figure 1 shows a schematic block diagram of the latest version *Beetle 1.2*.

The chip integrates 128 channels. Each channel consists of a low-noise charge sensitive preamplifier, an active CR-RC pulse shaper and a buffer. The rise time of the shaped pulse is ≤ 25 ns, the spill-over left 25 ns after the peak is less than 30 % of the maximum. The chip provides two different readout paths. For the *binary readout* the front-end's output couples to a comparator which features invertable outputs to detect input signals of either polarity and individually adjustable threshold levels. Four adjacent comparator outputs are logically ORed, latched, multiplexed by 2 and routed off the chip via low voltage differential signaling (LVDS) ports at 80 MHz. The *pipelined readout path* can operate in either a *binary* mode by using the comparator outputs or an *analogue* mode by sampling the front-end buffer's output with the LHC bunch-crossing frequency of 40 MHz. The sampled amplitudes are stored in an analogue memory (pipeline) with a programmable latency of 160 sampling intervals maximum and an integrated trigger buffer of 16 stages. Upon a trigger the corresponding signals stored in the pipeline are transferred to the multiplexer via a resettable charge sensitive amplifier. The number of output ports is configurable and allows a readout time of at minimum 900 ns per triggered event. The output of a sense channel is subtracted from the analogue data to compensate common mode effects. All amplifier stages feature forced bias currents. On-chip digital-to-analogue converters (DACs) with a resolution of 8 bits generate the

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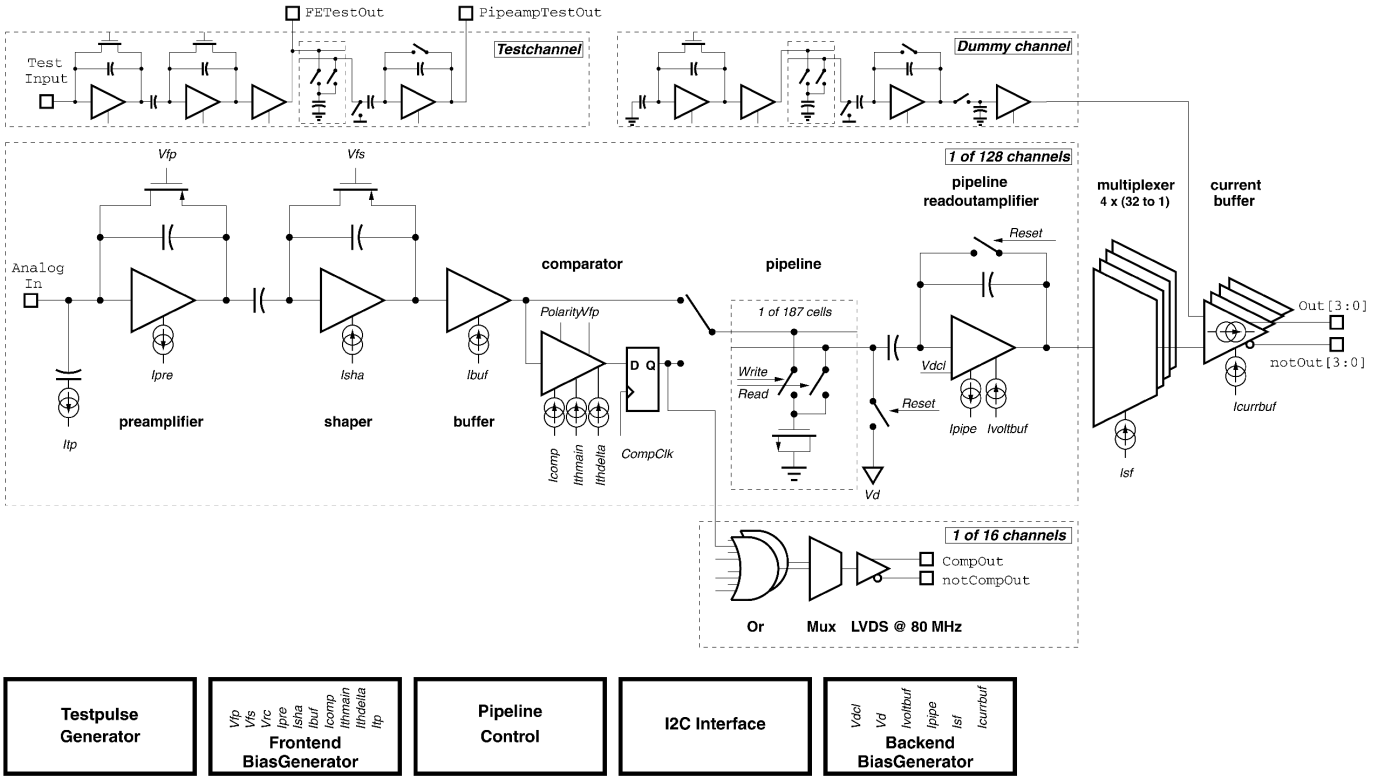

Figure 1: Schematic block diagram of the *Beetle* readout chip.

bias currents and control voltages. For test and calibration purposes, an adjustable charge injector is implemented on each channel. For applications which require a minimum number of transmission lines and put less strict demands on the readout speed, several *Beetle* chips can be read out in a daisy chain. All bias settings and configuration parameters, e.g. trigger latency, readout mode and readout speed, can be programmed and read back via a standard I^2C-interface [3]. All digital I/Os, except for the I^2C-lines and the daisy chain ports, use LVDS signals.

The *Beetle* is designed in a commercial 0.25 µm CMOS technology and has a die size of 6.1 x 5.1 mm^2 (Figure 2). The pitch of the analogue input pads is 40.24 µm. If no prompt readout is required, the chips can be mounted side-by-side, since no connections to the top and bottom side of the chip are required. This allows an overall pitch of 50 µm matching most silicon sensors. In case of the silicon vertex detector, the readout chip will be positioned only 5 cm from the LHC beam, which means that the *Beetle* has to be radiation hard. The chip is designed to withstand a total dose in excess of 10 Mrad (100 kGy) by taking the following design measures [4]: forced bias currents are used in all analogue stages instead of fixed node voltages; enclosed gate structures for NMOS transistors suppress increasing leakage currents under irradiation; a consistent use of guard rings minimizes the risk of Single Event Latchup (SEL) [5].

III. BEETLE 1.2 CHIP

The *Beetle 1.2* chip was submitted in April 2002 with the intention to fix all known bugs and to implement all missing features of its predecessor.

A. Design Changes

Many components are changed on *Beetle 1.2*. The most important modifications are:

- Implementation of a new front-end
- Single Event Upset (SEU) robust control circuits
- Modifications in the comparator (adjustable time constant of the integrator, mask registers for each channel)
- New analogue current output driver (fully differential, larger swing)
- DAC resolution reduced from 10 to 8 bits
- Increased maximum deliverable bias current (2 mA)

In addition to this major modifications, many minor changes have been done, e.g. the introduction of Schmitt-Triggers in the I^2C-input pads, extended pad-openings of the analogue input pads, introduction of a power-up reset and an improved power routing including additional power pads.

The robustness of the *Beetle 1.2* against SEUs was achieved by two different mechanisms. All flip-flops in the control circuitry are implemented in a triple redundant way including majority voting at the output. The DAC registers use a self-triggered correction mechanism: a bit is represented by three flip-flops with majority voting. A change in one of the three flip-flops triggers the flip-flops and the previous state is re-written. An integrated 8-bit counter counts the number of triggered corrections. It can be read via the I^2C-bus.

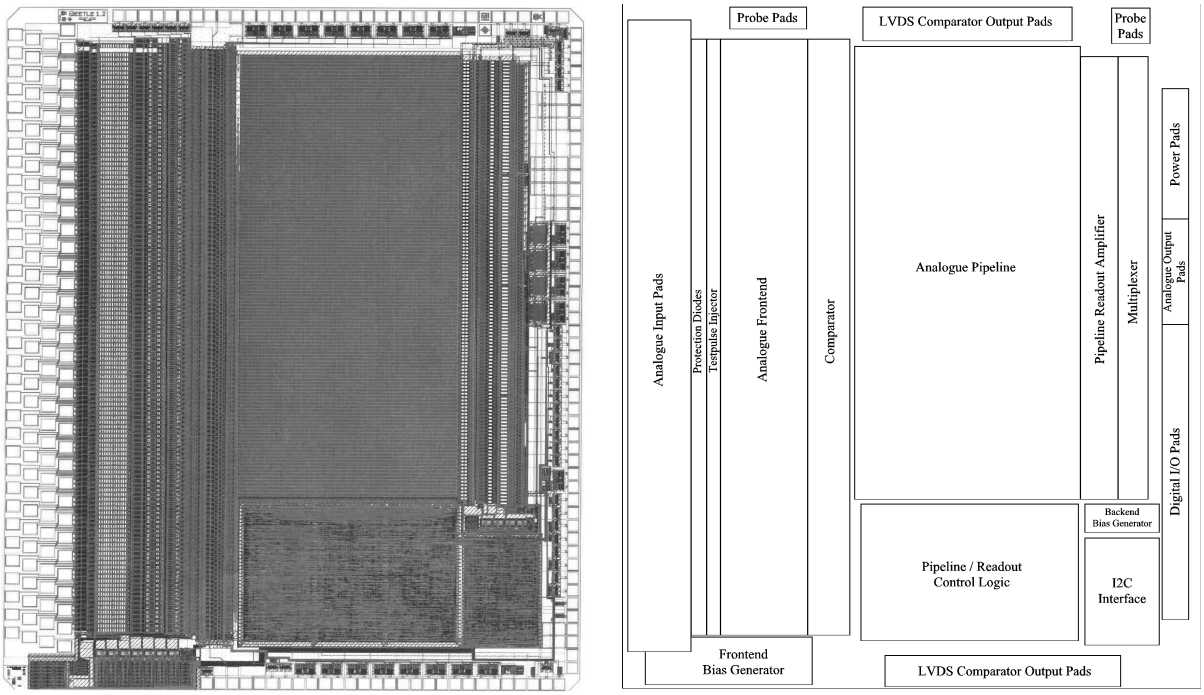

Figure 2: Layout of the *Beetle* 1.2 chip and its corresponding floor plan. The die size is 6.1 mm x 5.1 mm.

B. *Measurements*

1) *Analogue Readout*

Figure 3 shows the chip's output signal using the analogue pipelined readout mode multiplexing all 128 channels on one port. The output data stream contains two parts: first a 16 bit header. It encodes a Start-bit, the Parity-bit of the Pipeline Column Number (PCN), the status of the internal Error Detection and Correction (EDC), 3 bits for the parities of the internal shift registers (*TpSelect*, *CompMask* and *CompChTh*), the 2 LSBs of the internal SEU counter and the 8 bit PCN of the triggered event. With the programmed settings, the header bits corresponds to $\pm 42.150\ e^-$. After the header, the 128 analogue channels are read out. In Figure 3 input signals corresponding to 44.000 e^- and 22.000 e^- have been applied to 5 respectively 4 different input channels. The bent structure of the baseline is not yet understood.

2) *Front-end*

Information about the front-end pulse shape can be directly obtained from the test channel output *FETestOut* (Figure 1). Figure 4 shows the shaped front-end pulse of this test channel. Different load capacitances (C_p) have been applied to the preamplifier's input (3 pF, 13 pF, 26 pF, 36 pF and 51 pF). For the chosen bias settings the peaking time (0...100%) with any measured C_p is less than 24 ns. The remainder 25 ns after peak is also less than 30% for C_p values up to 35 pF. The results are consistent with measurements of the *BeetleFE 1.1* front-end test chip.

Some preliminary noise measurements on the *Beetle 1.2* front-end were done. The results are shown in Figure 6. A linear fit through the measured data results in the following Equivalent Noise Charge (ENC) value:

497 e^- + 48.3 pF/e^- Heidelberg

This value is in good agreement with measurements performed on the same front-end on the *BeetleFE 1.1* test chip.

429 e^- + 47.0 pF/e^- NIKHEF
436 e^- + 47.7 pF/e^- Zurich
483 e^- + 45.7 pF/e^- Heidelberg

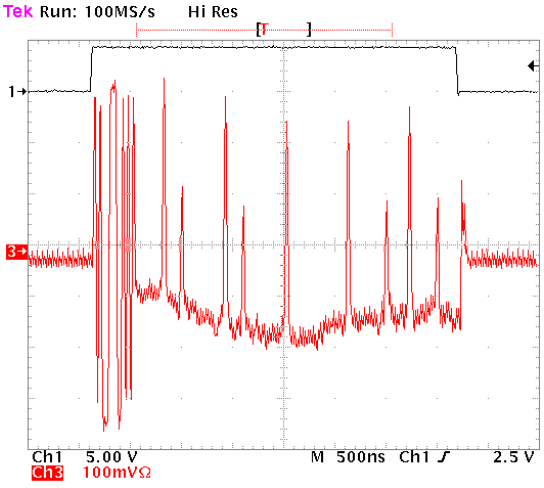

Figure 3: 128 analogue channels of the *Beetle 1.2* are multiplexed on one output port at 40 MHz.

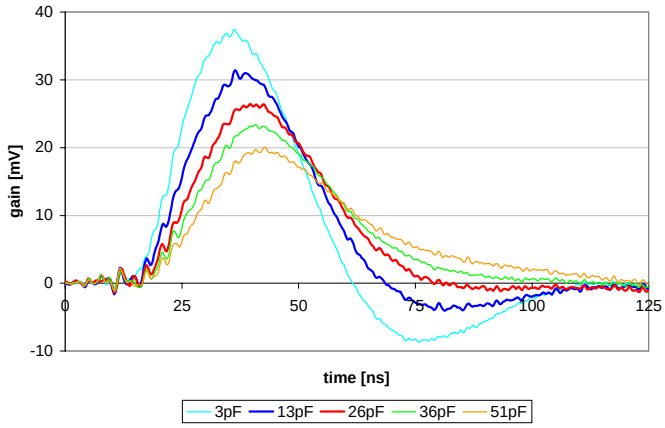

Figure 4: Front-end pulse shape of a 22.000 e^- input signal measured at 3, 13, 26, 36 and 51 pF external load capacitances

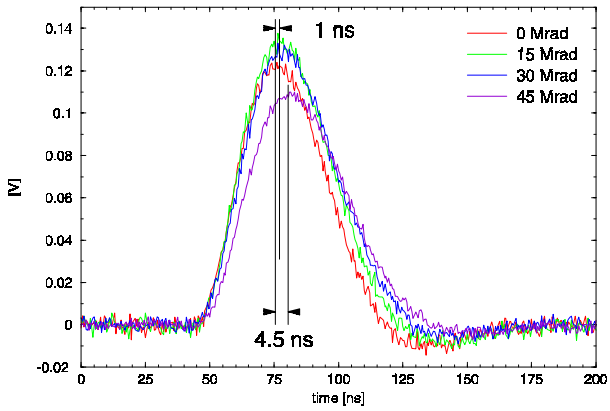

Figure 5: Measured front-end pulse shape after a total accumulated dose of 0, 15, 30 and 45 Mrad

IV. Radiation Hardness

In October 2001, 4 *Beetle 1.1* chips were irradiated at the X-ray facility of the CERN microelectronic group. 2 chips were kept at room temperature whereas the other 2 chips were annealed at 100 °C after the irradiation. The total accumulated doses are: 10 Mrad, 10 Mrad, 30 Mrad and 45 Mrad for the different chips.

During the irradiation the *Beetle* was operated (trigger and readout) at the nominal settings. No functional errors in the control circuitry have been observed. Figure 5 shows a pulse shape scan of the *Beetle 1.1* which was irradiated to 45 Mrad. The peaking time and the amplitude of the output pulse change only slightly up to 30 Mrad. After 45 Mrad the peaking time increased by 4.5 ns, while the gain decreased by about 10%.

V. Future Plans

A detailed characterization of the *Beetle 1.2* chip is still due since we received the chips not until August 2002. The following measurements will be performed:

- Homogeneity and gain scans of the complete pipeline
- Test and characterization of all different readout modes
- Detailed comparator studies (thresholds, cross-coupling, matching)
- Random trigger test of the control circuitry
- Detailed ENC measurements
- A TID irradiation test with a sample of *Beetle 1.2* chips
- Beam-test and hadron irradiation to prove the SEU robustness of the chip

Further information and test results will be available at **http://wwwasic.kip.uni-heidelberg.de/lhcb**

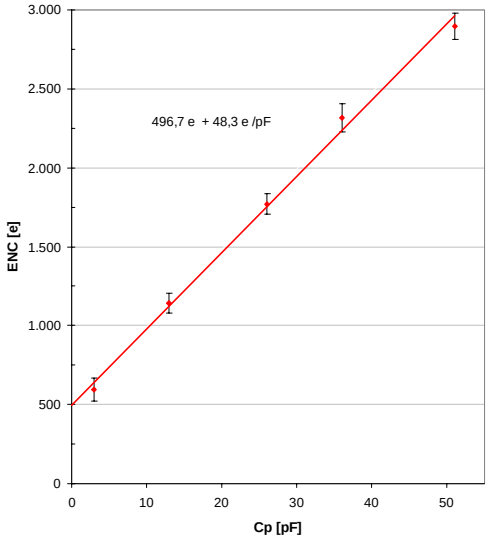

Figure 6: Preliminary ENC behaviour of the *Beetle 1.2* front-end

VI. References

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