The ATLAS Pixel Chip FEI in 0.25µm Technology

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for the ATLAS pixel collaboration

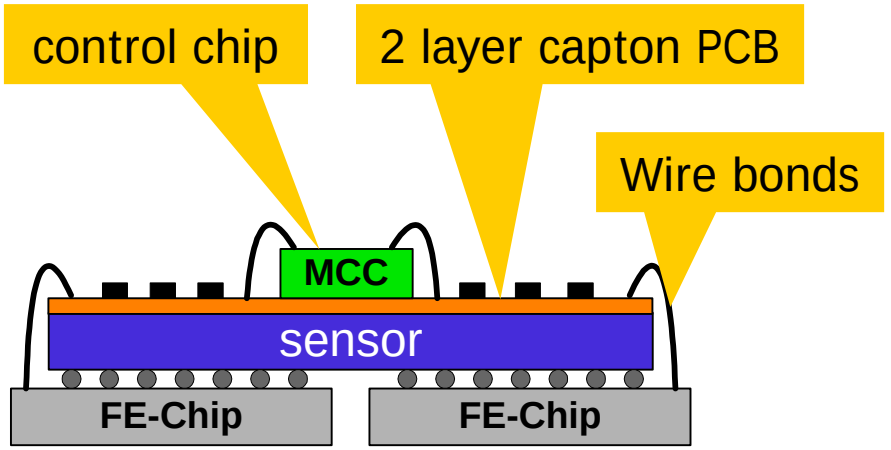
The ATLAS Pixel Chip FEI

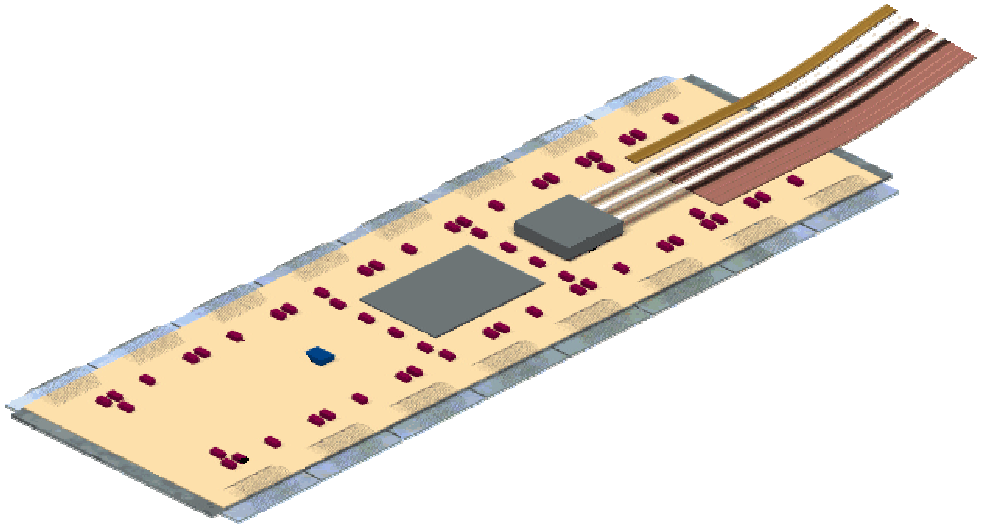
- Short Introduction to ATLAS Pixel
  - mechanics, modules and cooling
- The Front End Chip FEI
  - analog section
  - digital readout
  - some circuit details
- Results
  - lab measurements, (test beam), irradiation
- Summary

The ATLAS Pixel Module

Flex capton solution:

- Connections between FE-Chips, module control chip, other components and cable through a thin capton PCB
- Larger pixels between chips
- Size = 16.4 × 60.8 mm^2
- 16 chips with ~ 50000 pixels
- ~ 2000 modules needed

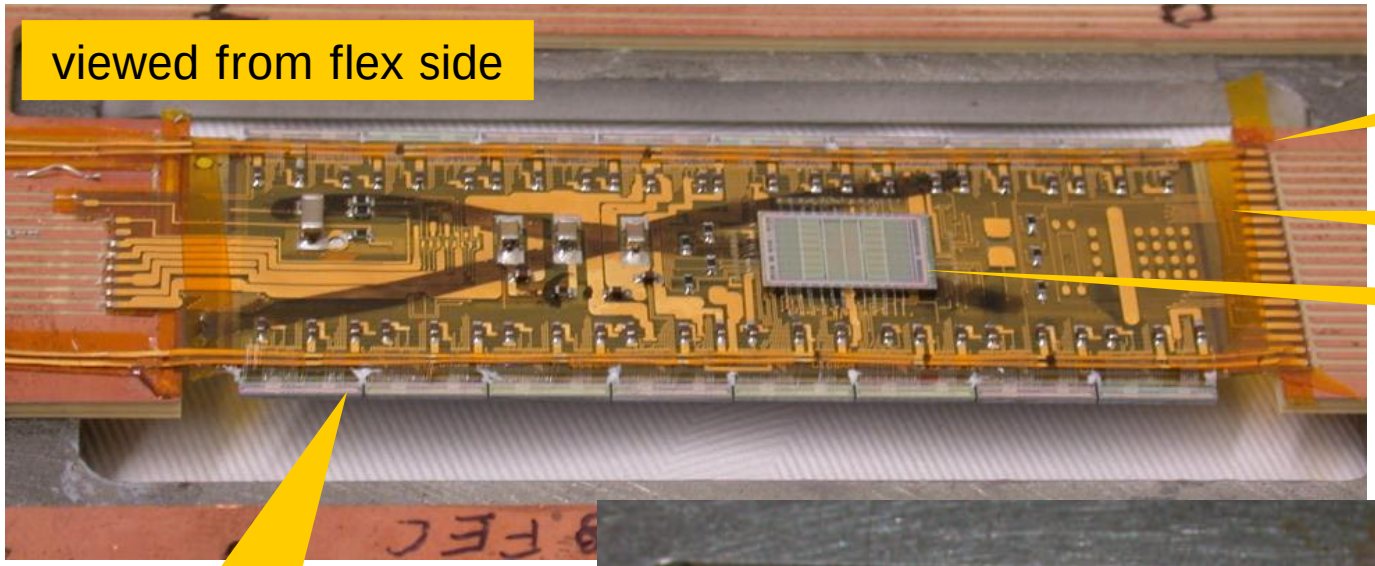


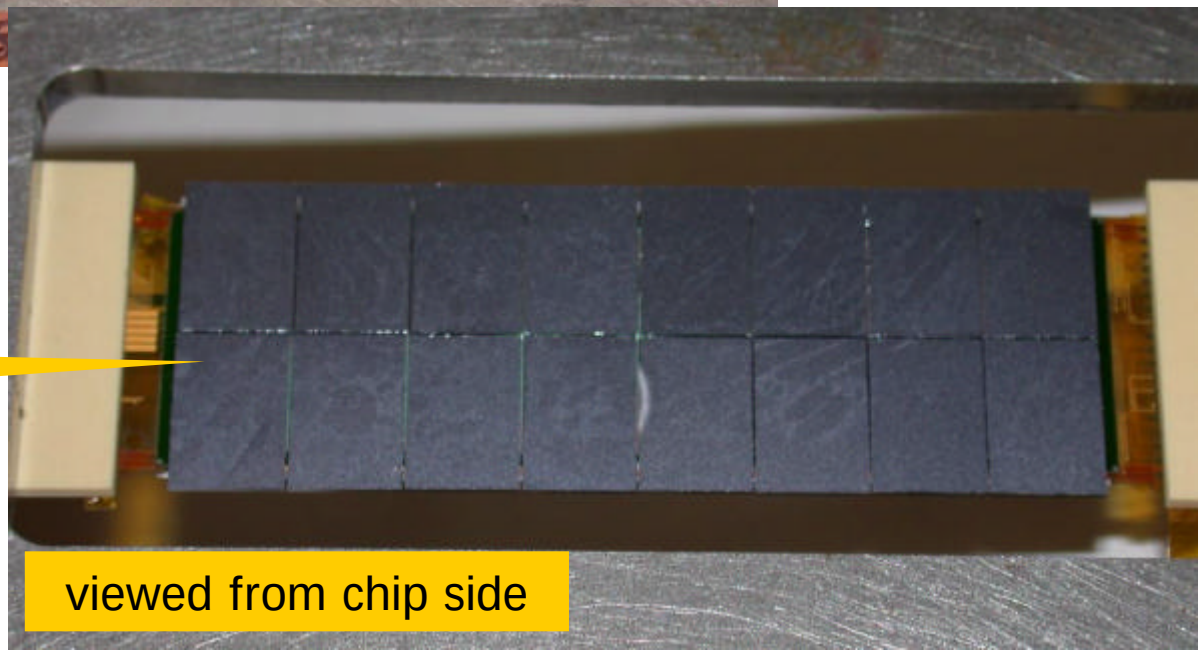


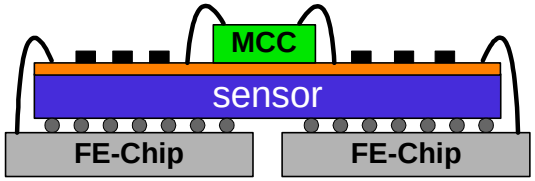
- Material:
  - 200 µm silicon sensor 0.22 %
  - chips thinned to 200 µm 0.14 %
  - bumps, bonds, glue… 0.10 %
  - caps, support, cooling, cables 0.90 %

  Total: 1.4 – 1.8 %

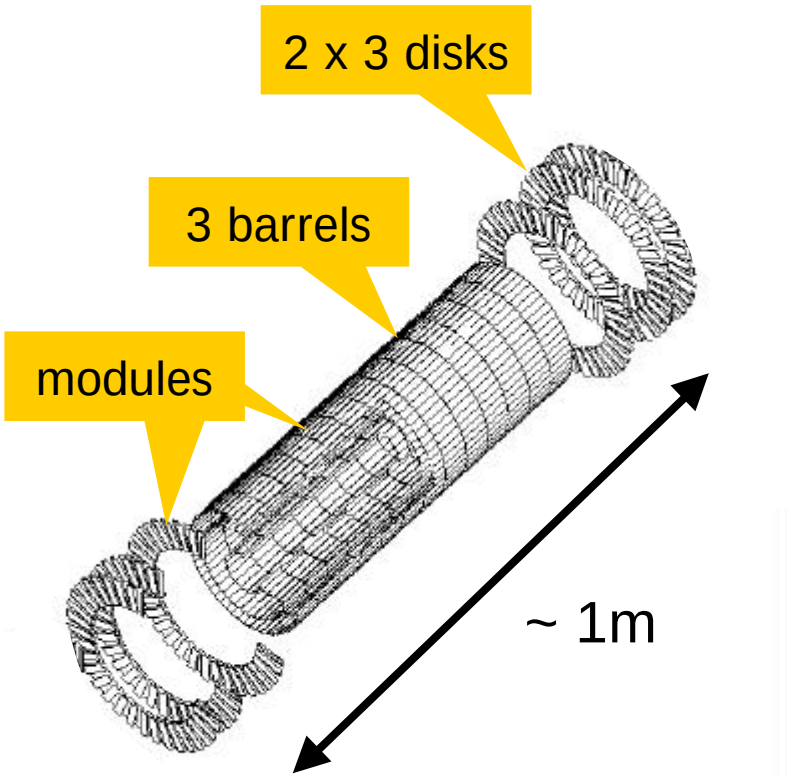
Flex Module in Mounting Frame

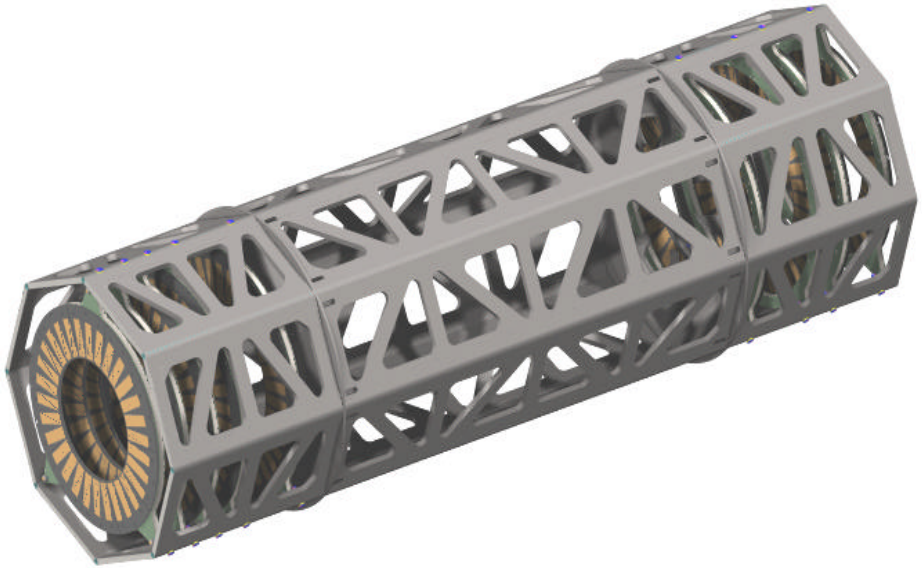






Overall layout

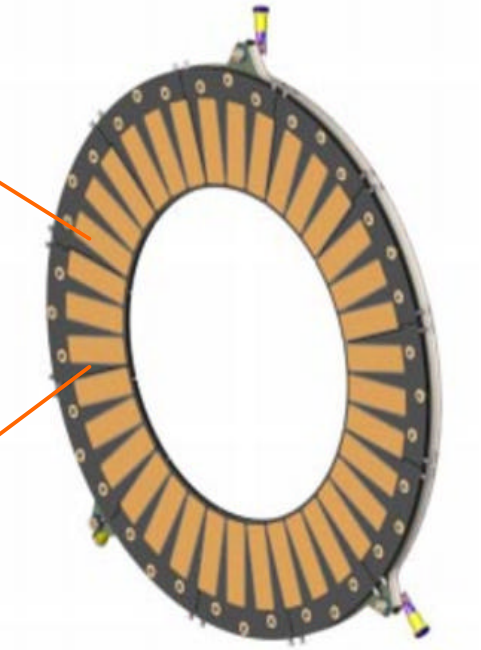


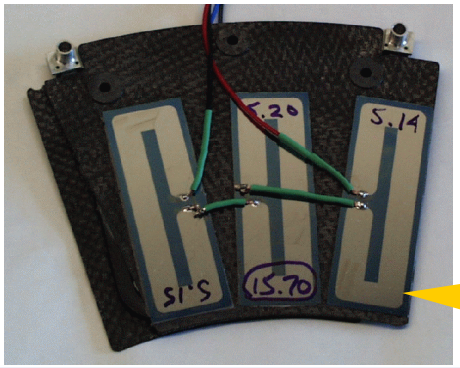


- Global support is a flat panel structure
- Made from carbon composite material (IVW, Kaiserslautern)
- Total weight is 4.4kg
- 3 pieces, center part consists of two half-shells to open

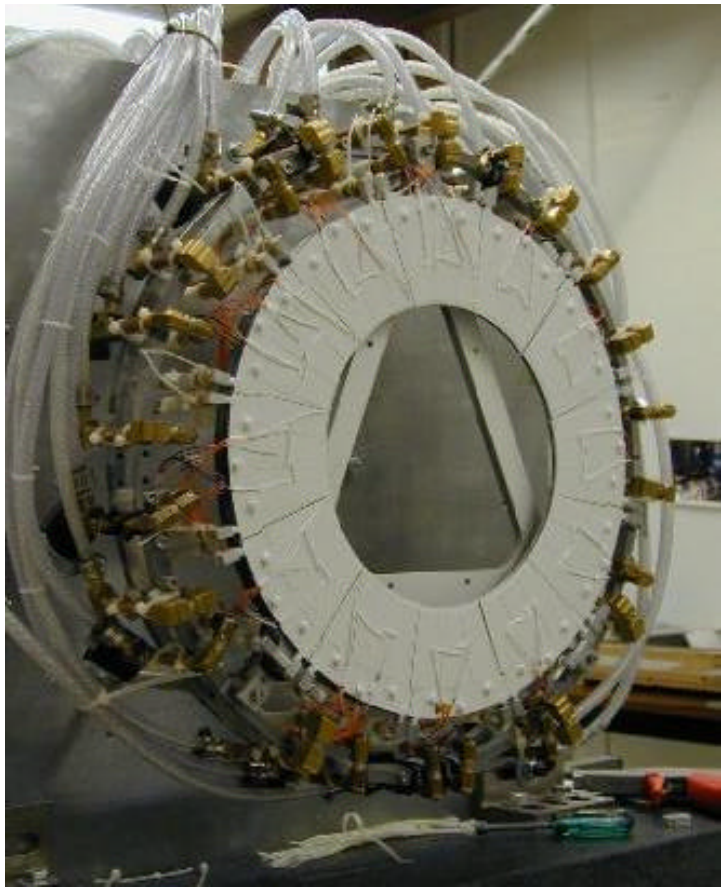
Disks and Sectors

- Disks are divided into sectors
- Coolant flows in tube between two C-C facings
- Modules are arranged on both sides for overlap
- Production in USA





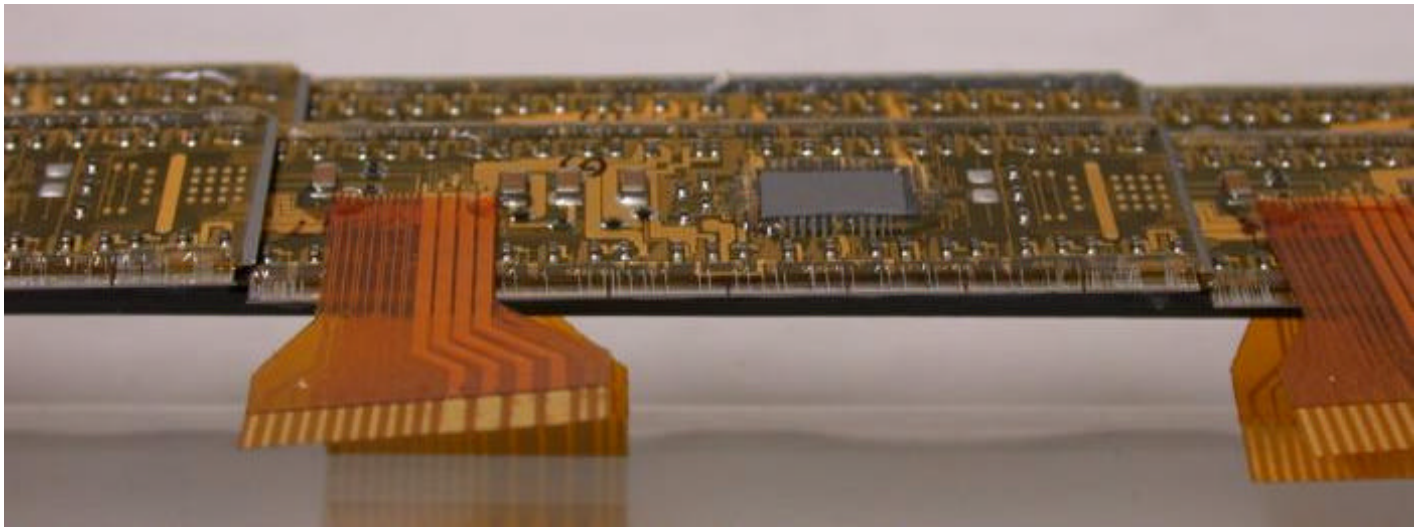
Sector with 3 ‚modules‘

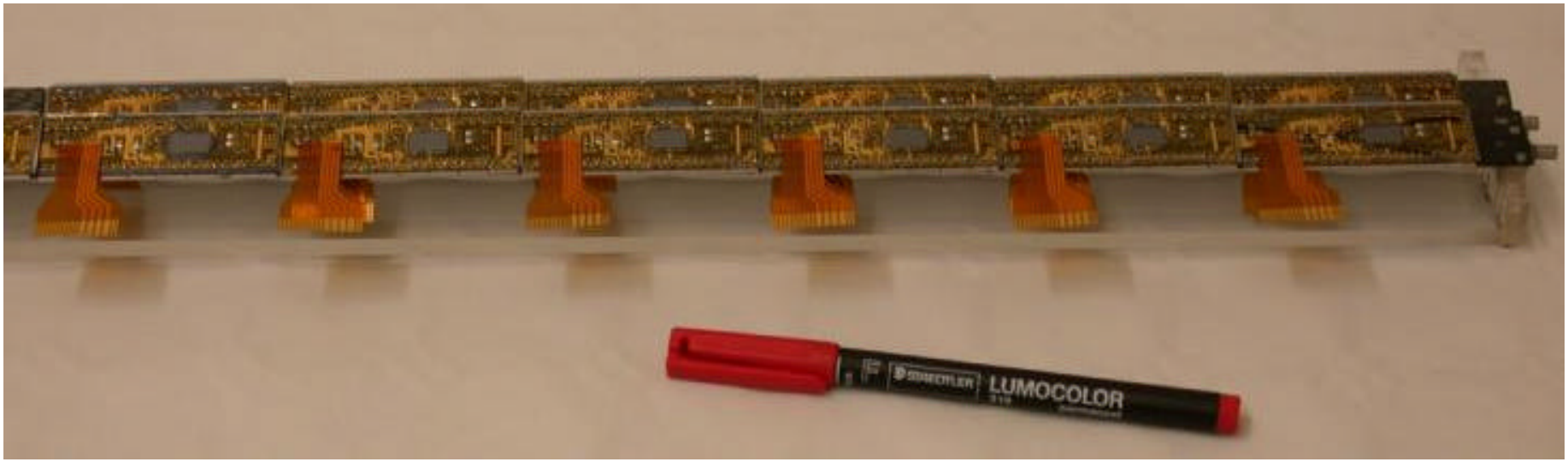


cooling test of full disk (@ LBNL)

Barrels and Staves

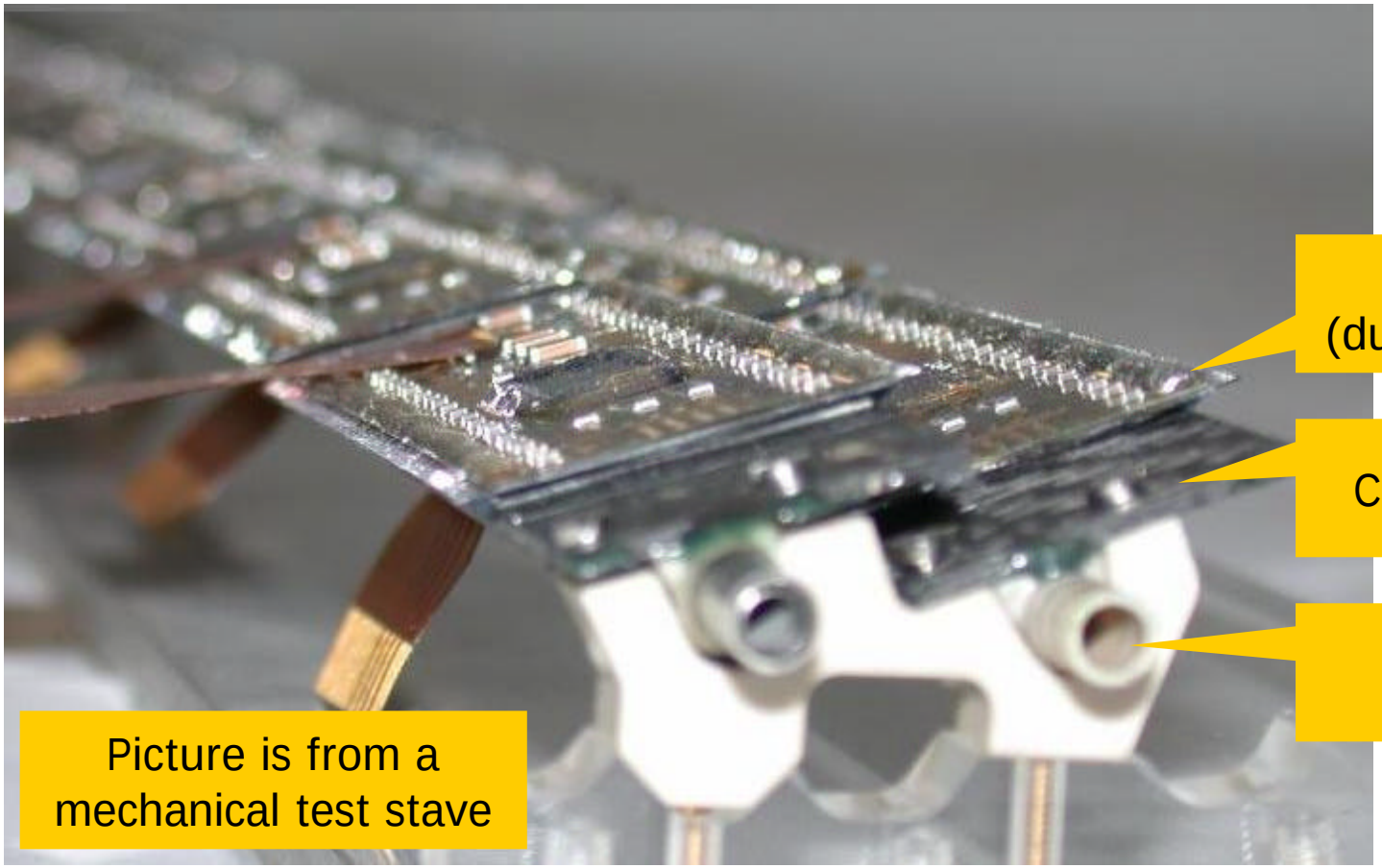
- Barrels consist of staves with 13 modules (shingled for overlap in z direction)





Barrels and Staves

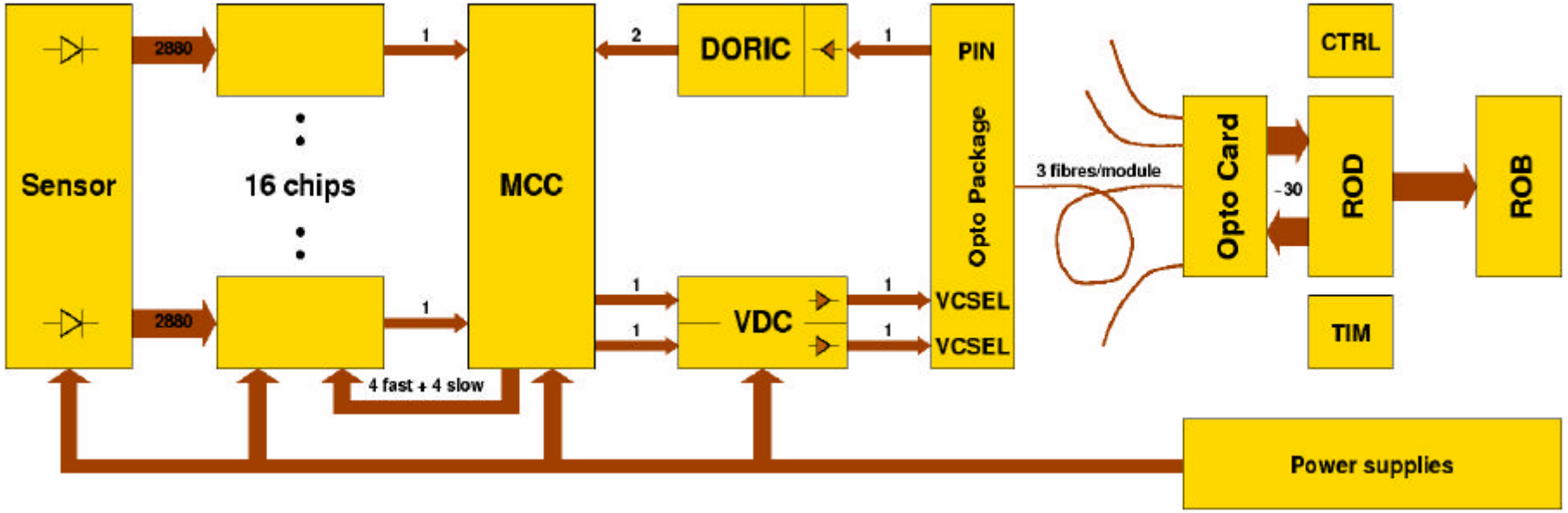
- Stave is a carbon structure with an Al tube for cooling
- Staves are tilted for overlap in phi (+change sharing)
- Production mainly in Germany, Italy, France



Cooling

- Very important
  - Contributes significantly to material budget
  - Limits the power / performance of electronics
  - Detectors must stay below –6°C to limit damage from irradiation (see later)
- ‚binary ice' solution dropped
  - Cooling power is marginal
  - Fail safe operation for leaks in tubes not possible
  - Liquid is too much material
- ATLAS pixel developed evaporative cooling:
  - Cooling by evaporation of fluorinert liquid (C_4F_{10} or C_3F_8) @ -20°C. Needs pumping.
  - Low mass (gas!), small diameter tubes (only small pressure drops)
  - Very large cooling capacity
  - Aluminum tubes must withstand 6 atm if pumping stops and coolant develops its full vapor pressure.
- All components must cope with thermal cycling 25°C $\Leftrightarrow$ -20°C

Electronic Components of the Pixel System



module | end of stave | control room

1 Sensor
16 front end chips (FE)
1 module controller (MCC)

2 VCSEL driver chips (VDC)
1 PIN diode receiver (DORIC)

Optical receivers
Readout Drivers (ROD)
Readout Buffers (ROB)
Timing Control (TIM)
Slow Control, Supplies

The ATLAS Pixel Chip FEI

Short Introduction to ATLAS Pixel

- mechanics, modules and cooling

The Front End Chip FEI

- analog section – block diagram, layout,
- digital readout
- some details

Results

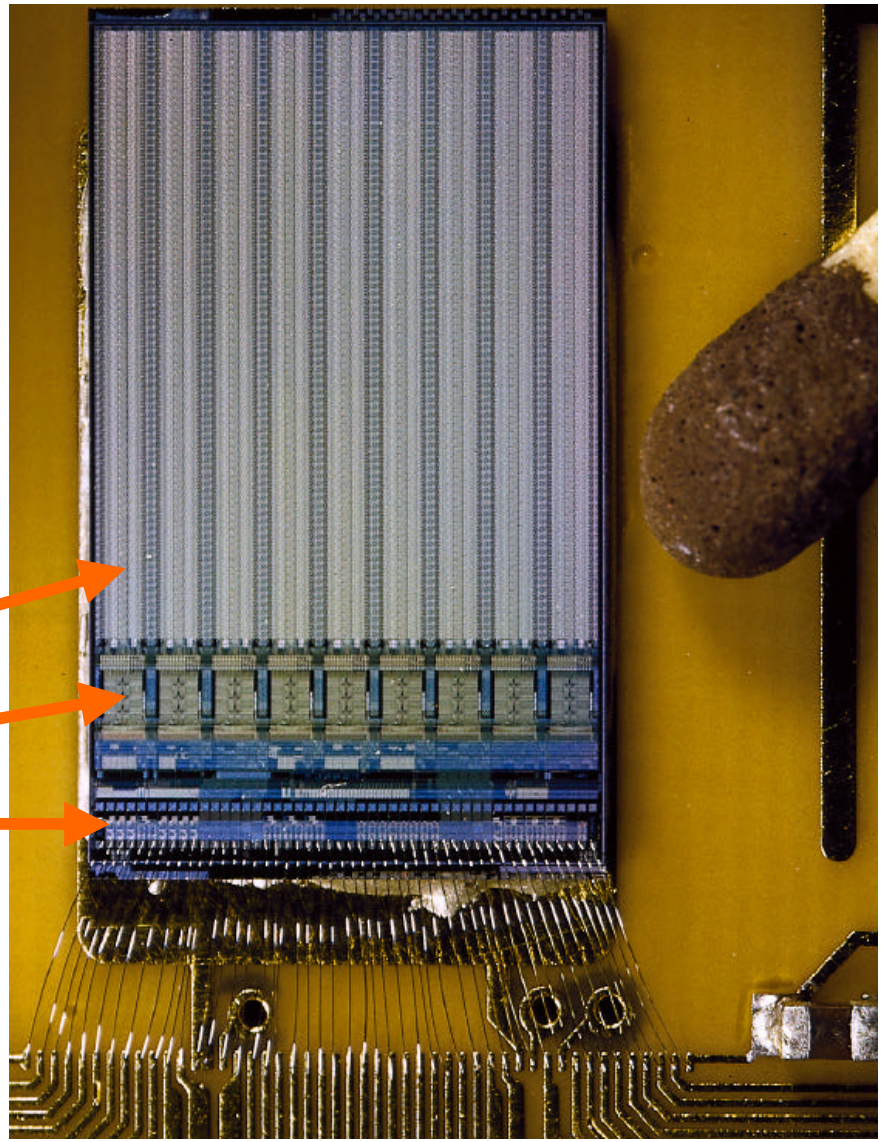
- lab measurements, test beam, irradiation

Summary

The ATLAS Pixel Front End Chip Family

- Chip size: 7.4mm x 11mm
- Pixels: 18 x 160 = 2880
- Pixel size: 50µm x 400µm
- Technologies: 0.8µm CMOS (FEA,FEB)
  0.8µm BiCMOS (FED)
  0.25µm CMOS (FEI)

- Operation at 40 MHz
- Zero suppression in every pixel
- Data buffering until trigger arrives
- Digital Readout (1 bit serial, LVDS)
- Digitized amplitude of every pulse (ToT)
- Serial control, on-chip bias, on-chip charge injection, ...



Schedule and Team

- FED (0.8µm, 2 metal layers, BiCMOS (only CMOS used))
  - Wafers back end of 1999. Design is functional.
  - But: Yield was extreamly poor!
  - Long investigations showed 'shorts' in MOS devices. These lead to fast (100ns) discharge of dynamic nodes (required for design density!)
  - Vendor could not solve the problem ⇒ dropped DMILL end of 2000

- FEI (0.25µm, 5 metal layers, CMOS)
  - Wafers back january 2002. Design is functional.
  - Yield of first run was poor (Numbers are for register tests only so far!)
  - Yield of 2nd batch was worse
  - Yield of new run (same reticle) is good

- Design of both chips
  - Bonn (M. Ackers, P. Fischer, I. Peric et al.)
  - CPPM (L. Blanquart et al.)
  - LBNL (K. Einsweiler, E. Mandeli, R. Marchessini, G. Meddeler et al.)

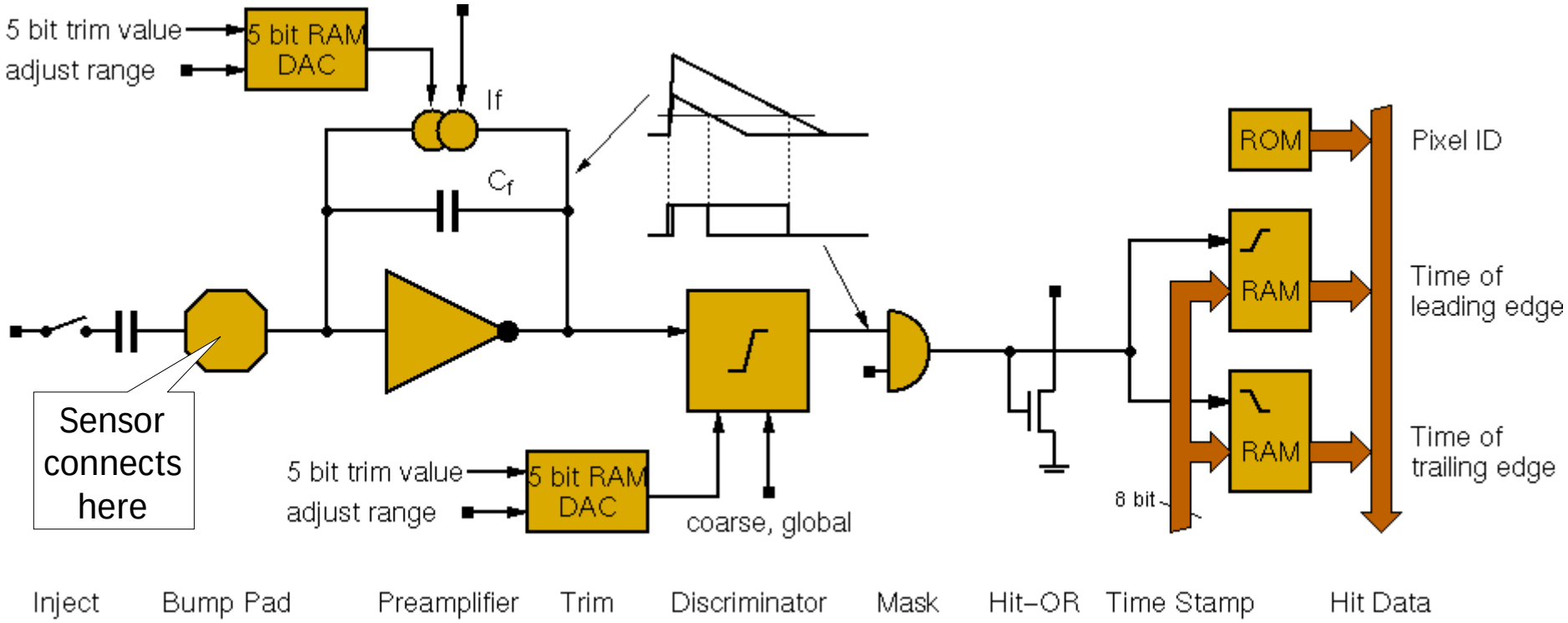
- Test, Testbeam, Irradiation: J. Richardson et al.

Pixel Analog Part

feedback uses constant current
- high stability for fast shaping
- tolerates > 100 nA leakage
- linear decay

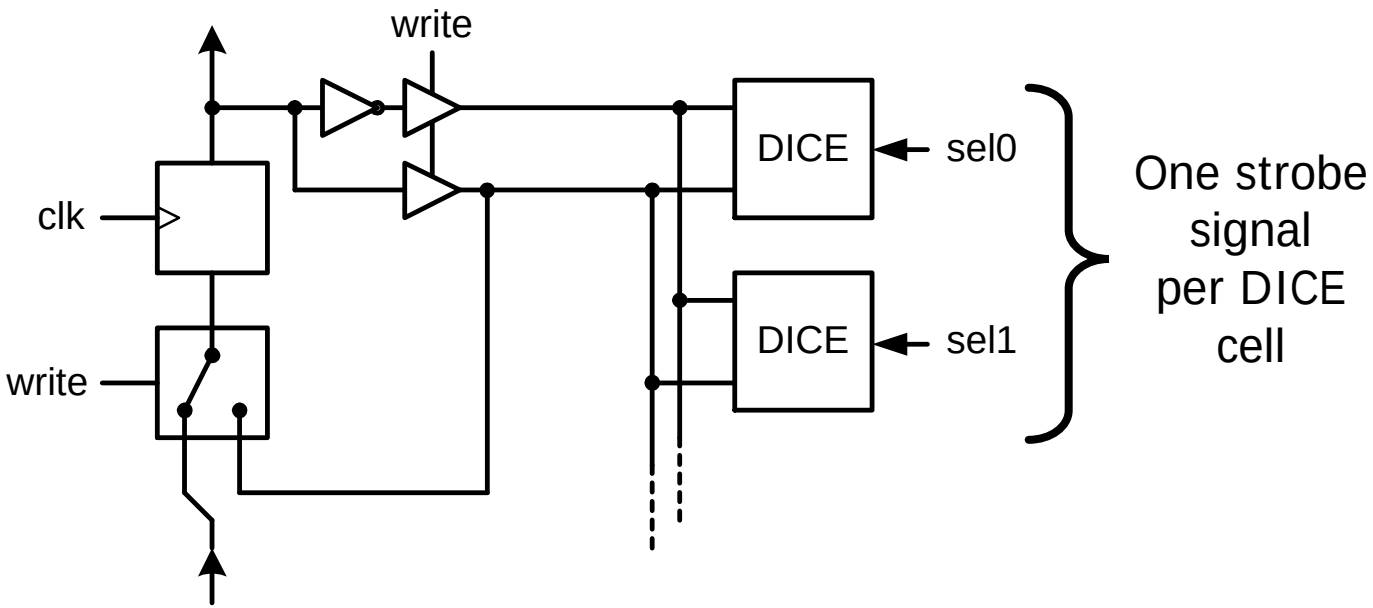
Analog information
- measure width of hit
- works nicely due to linear discharge

Individual adjustment of
- Threshold
- feedback current (FEI)
- ranges are adjustable



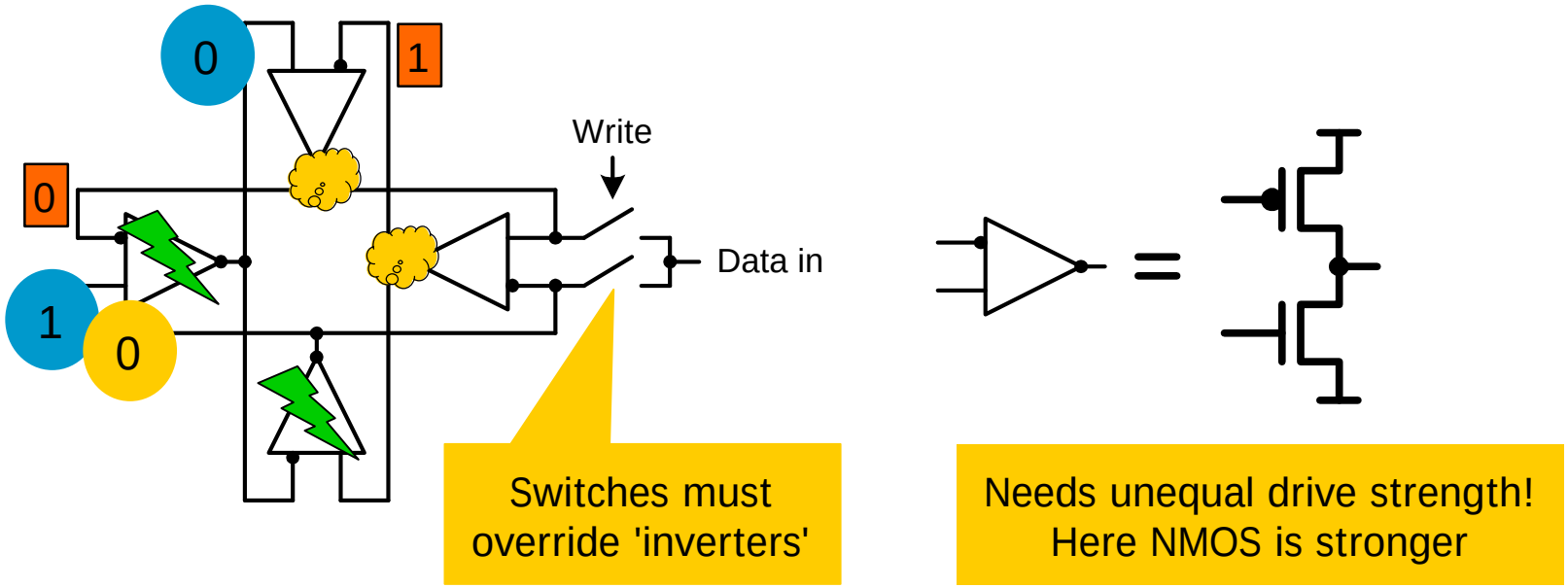
Pixel Control

- 14 control bits per pixel are needed (2x5 bit DAC, inject, mask, kill_amp, en_hitbus)
- They are stored in single-event-upset - tolerant 'DICE' cells
- Write / read is through a shift register
  (readback is important to check for SEU during writing and for chip testability)



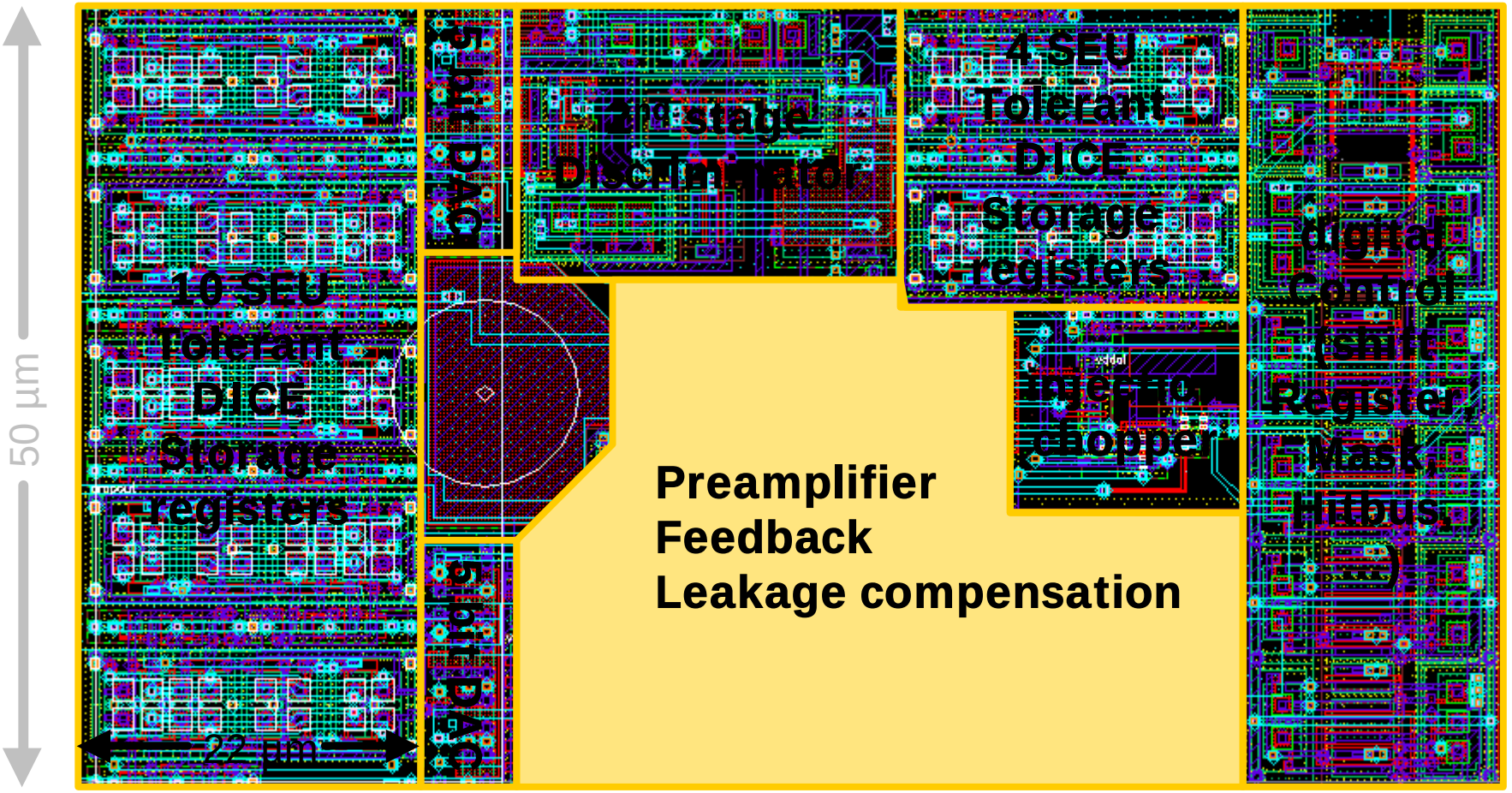
SEU tolerant design

- The 'Dual interlock storage cell' (DICE) cell is a clever latch which needs simultaneous writing to two nodes in order to flip.
- Devices: 8 NMOS, 4 PMOS (no reset)
- Present layout minimizes area. The 2 redundant nodes are not widely seperated

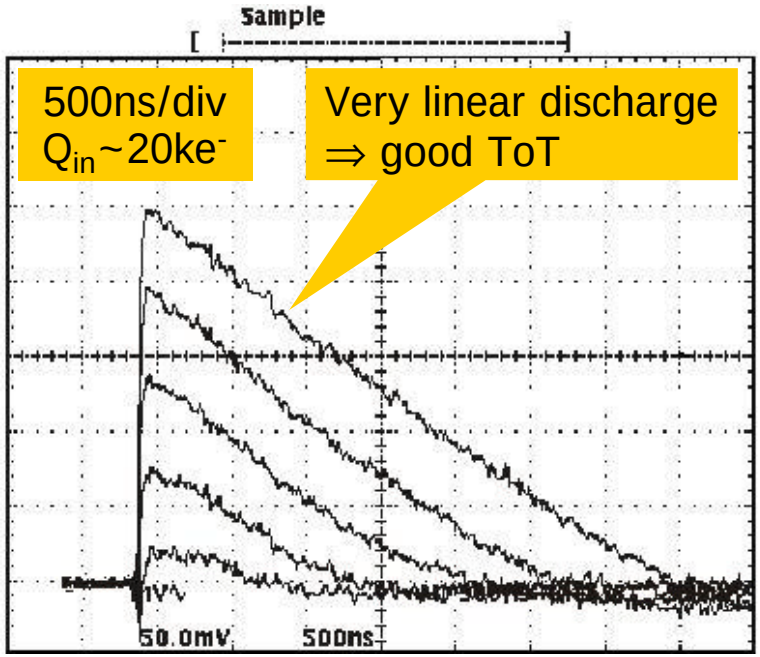


(Calin, Nicolaidis, Velazco, IEEE Trans. Nucl. Sci., Vol.43, No.6, 1996)

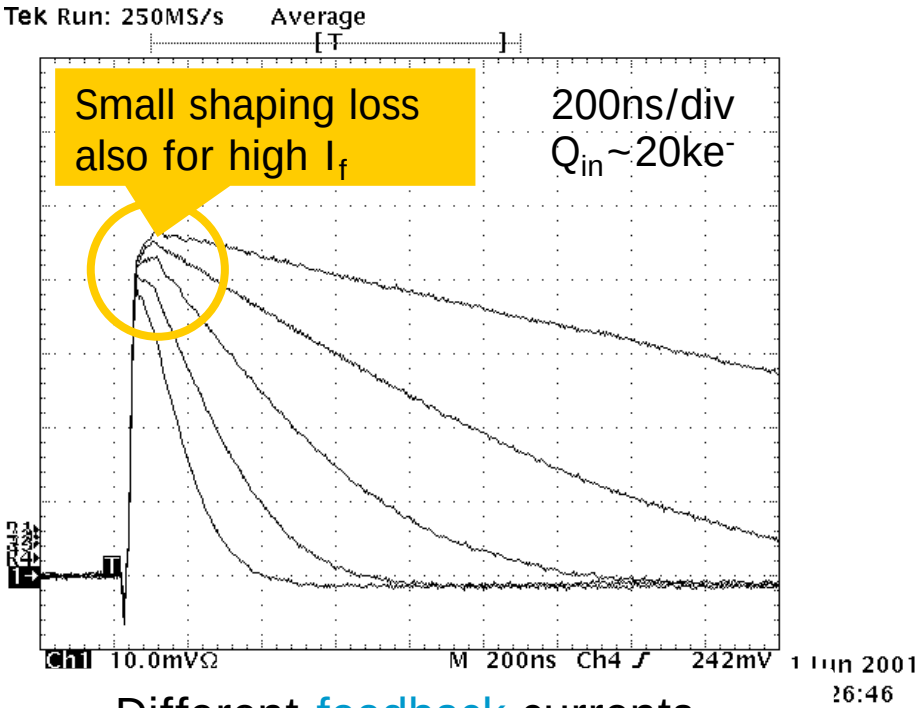
Layout of Analog Part + Control



Preamplifier Output Pulses



Different injected charges
(~5000 – 25000 e$^-$)

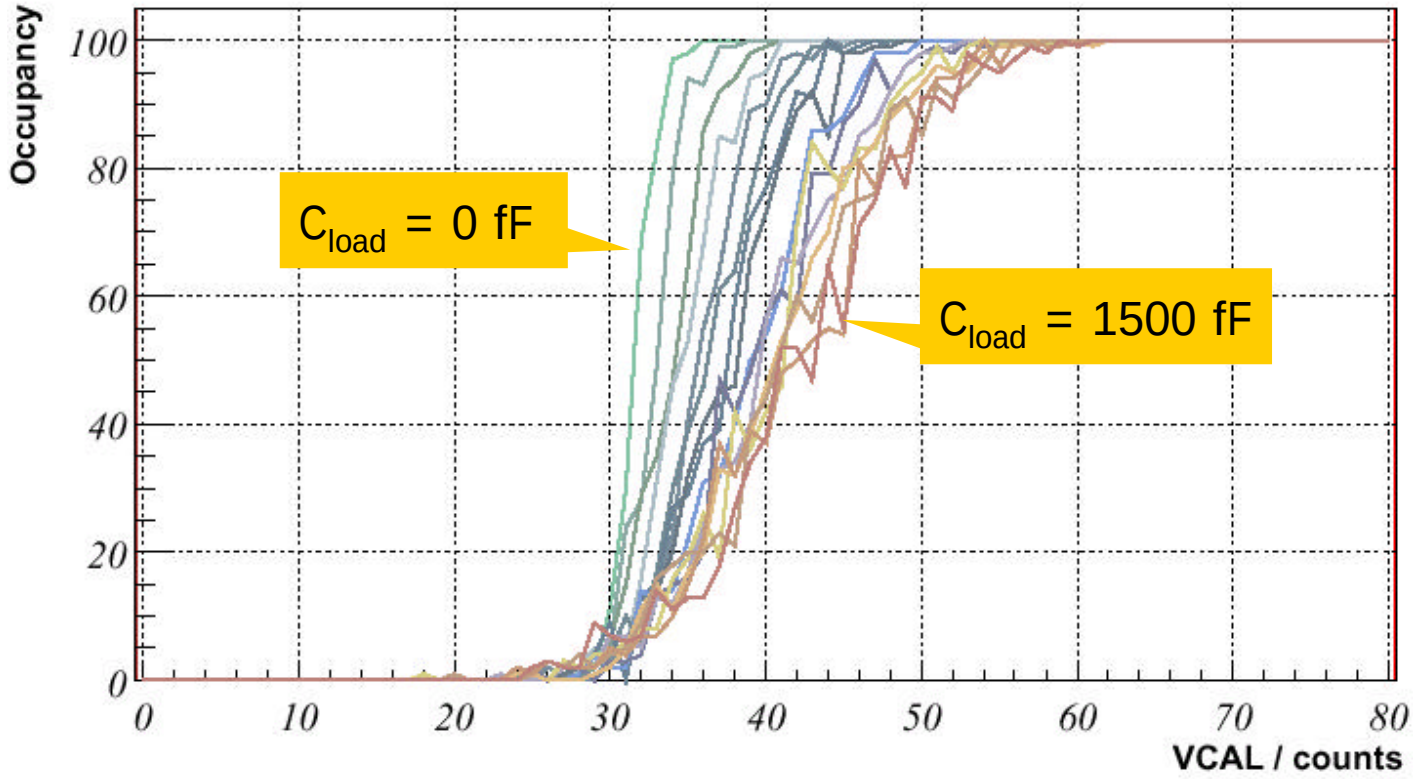


Different feedback currents
(~ 1nA – 20nA)

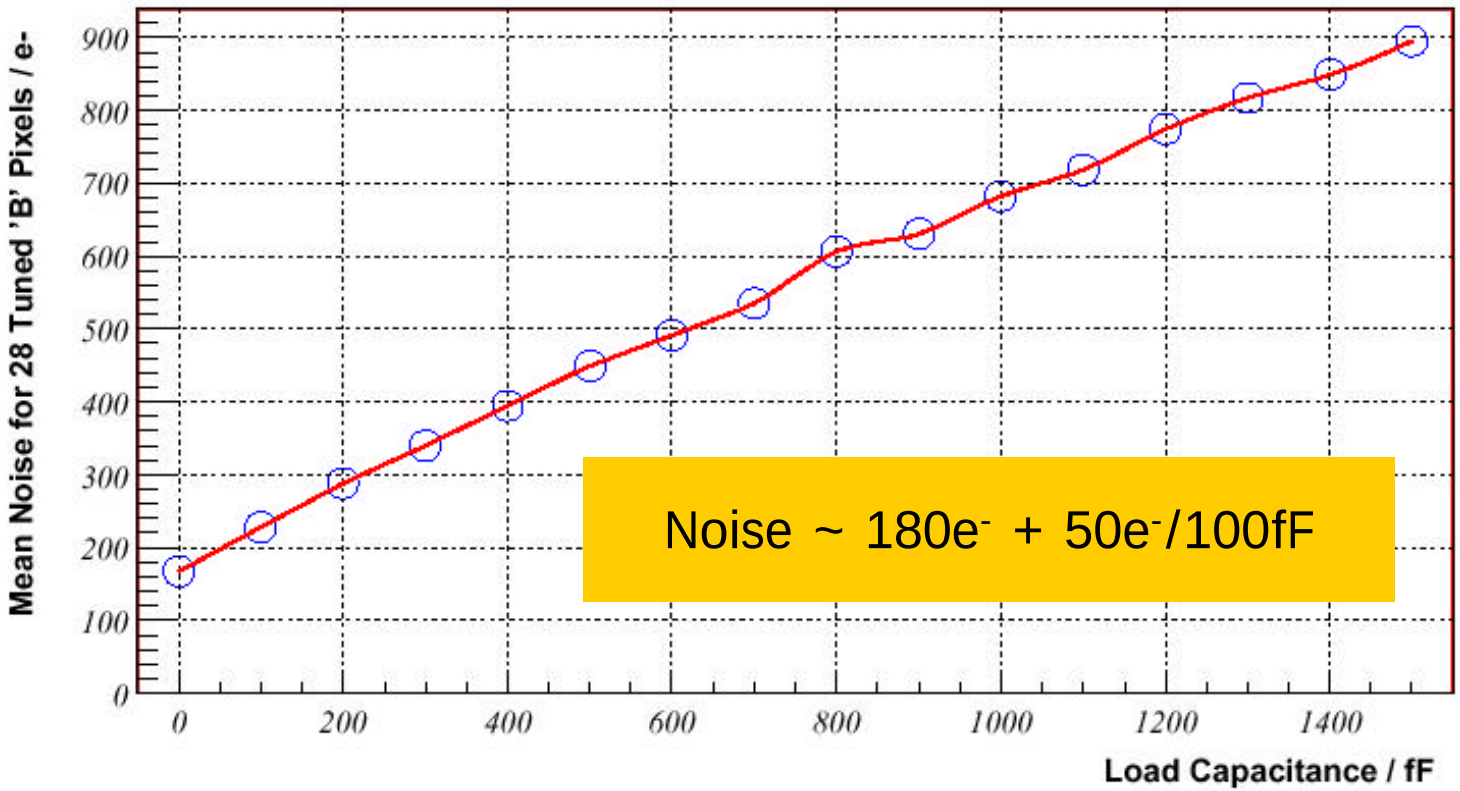
- Pulses measured through on-chip buffer

Noise vs. capacitive Load

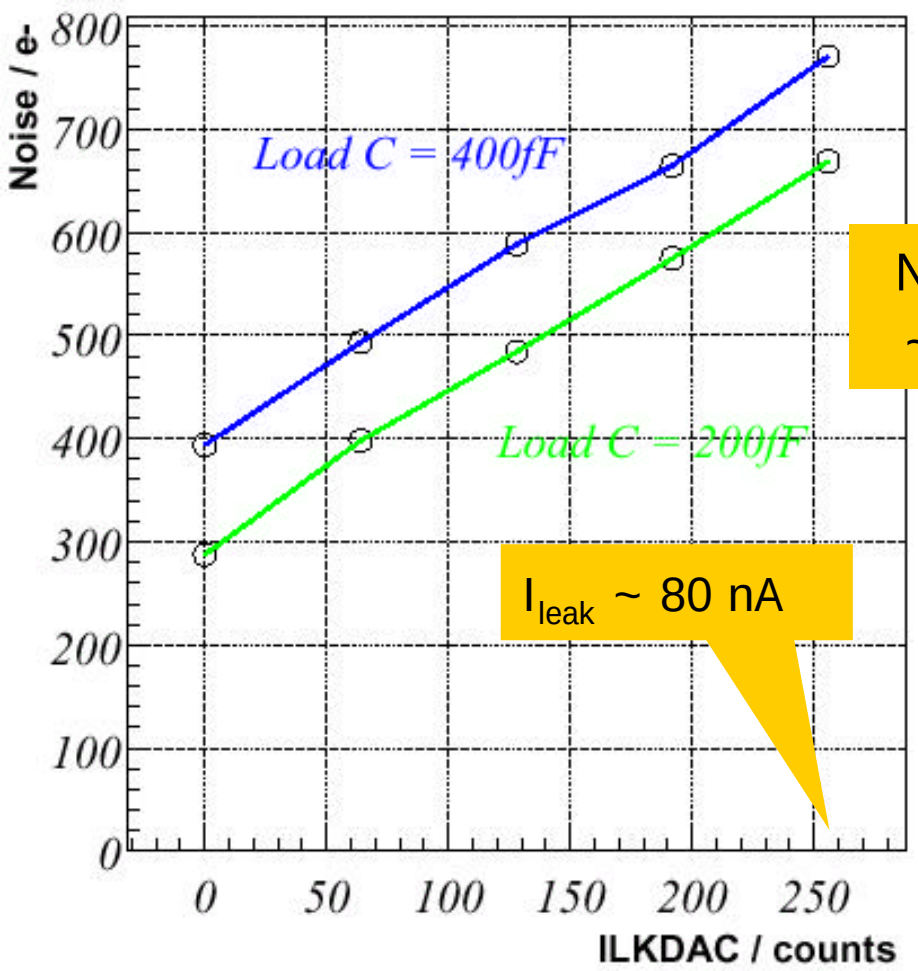
- Measured on a test chip (from same run)
- Test chip has programmable, calibrated load capacitors on preamplifier inputs
- Measurements use internal injection chopper (consistent with external injection)



Noise vs. capacitive Load



Noise vs. Sensor Leakage Current



Noise increase
~ 50e$^-$ / 10nA

I_{leak} ~ 80 nA

- Measured on test chip which has current sources at preamplifier inputs

Time Stamp Data Readout

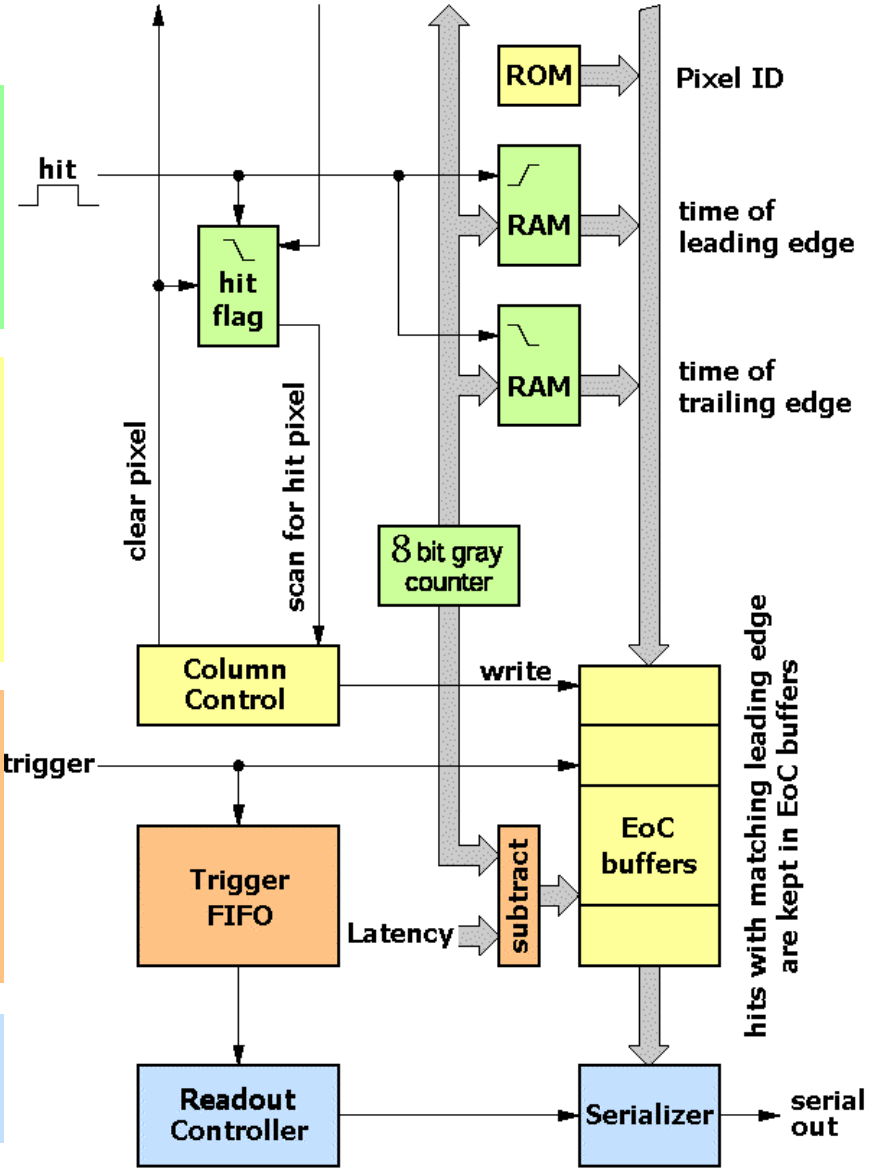
4 simultaneous tasks are running permanently:

- A time stamp (8 bit Gray Code) is distributed to all pixels
- When a pixel is hit, the time of rising and trailing edges are stored in the pixel

- The hit is flagged to the periphery with a fast asynchronous scan
- Time information and pixel number are written into a buffer pool (common to a column pair)
- The hit in the pixel is cleared

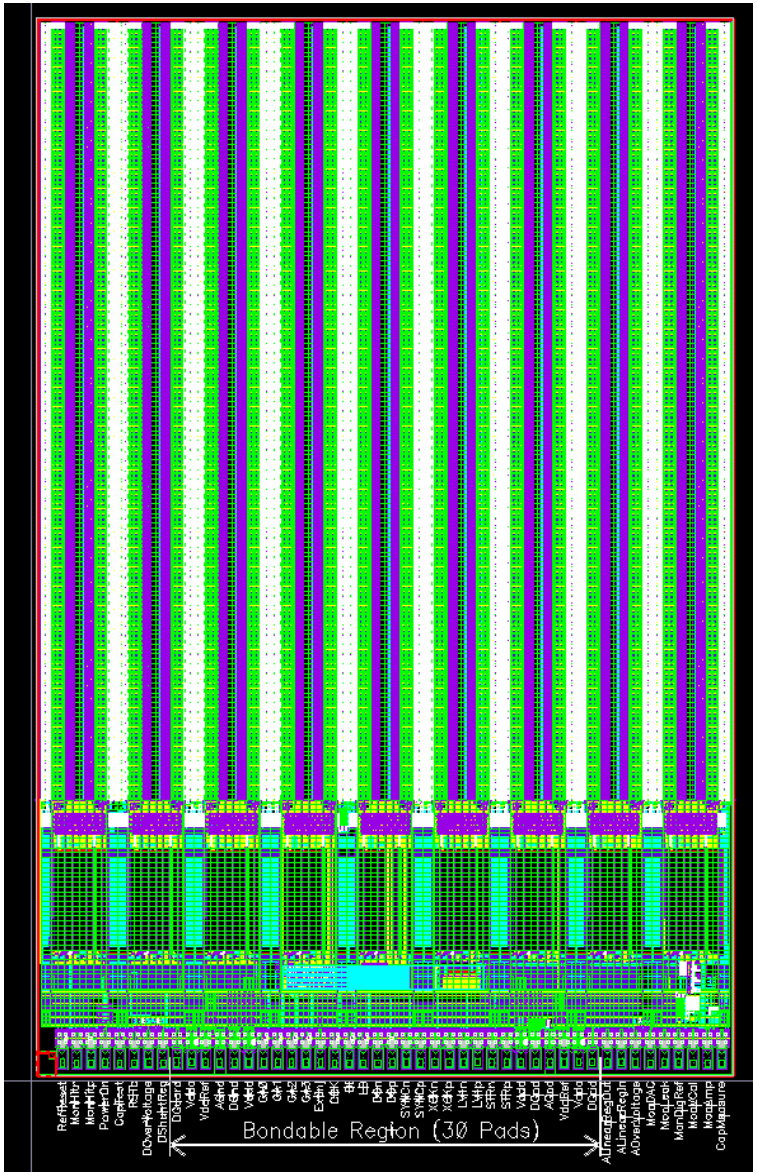
- If a trigger arrives, the time of the hit (leading edge data) is compared to the time for hits associated to this trigger. Valid hits are flagged, older hits are deleted.
- The trigger is queued in a FIFO

- All valid hits of a trigger are sent out serially. All triggers in the FIFO are processed.



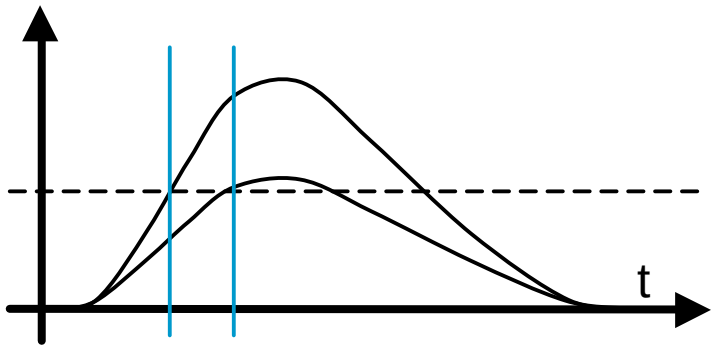
Other features

- Design uses radiation tolerant design technique
- Only 30 bond pads required on module
  (2 x 6 power, 4(+4) slow control, 5 fast LVDS)
- We have now 64 EoC buffers
- Built-in testability:
  - MUX access to all bias DACs
  - Digital injection of arbitrary hit patterns
  - readback of all registers
  - Injection chopper on chip with high/low mode
- Sensor leakage current can be measured in every pixel with on-chip ADC
- Have ~6nF decoupling capacitors on chip
- Supply currents are
  I_{dig}~ 62 mA @ 2V, I_{analog}~ 50 mA @ 1.6V



Digital Time Walk Correction

- We must associate an event to a single bunch crossing (25 ns)
- Problem:
  - small signals just above threshold fire the disciminator late – 'time walk'
  - hit is lost if added delay > 25ns

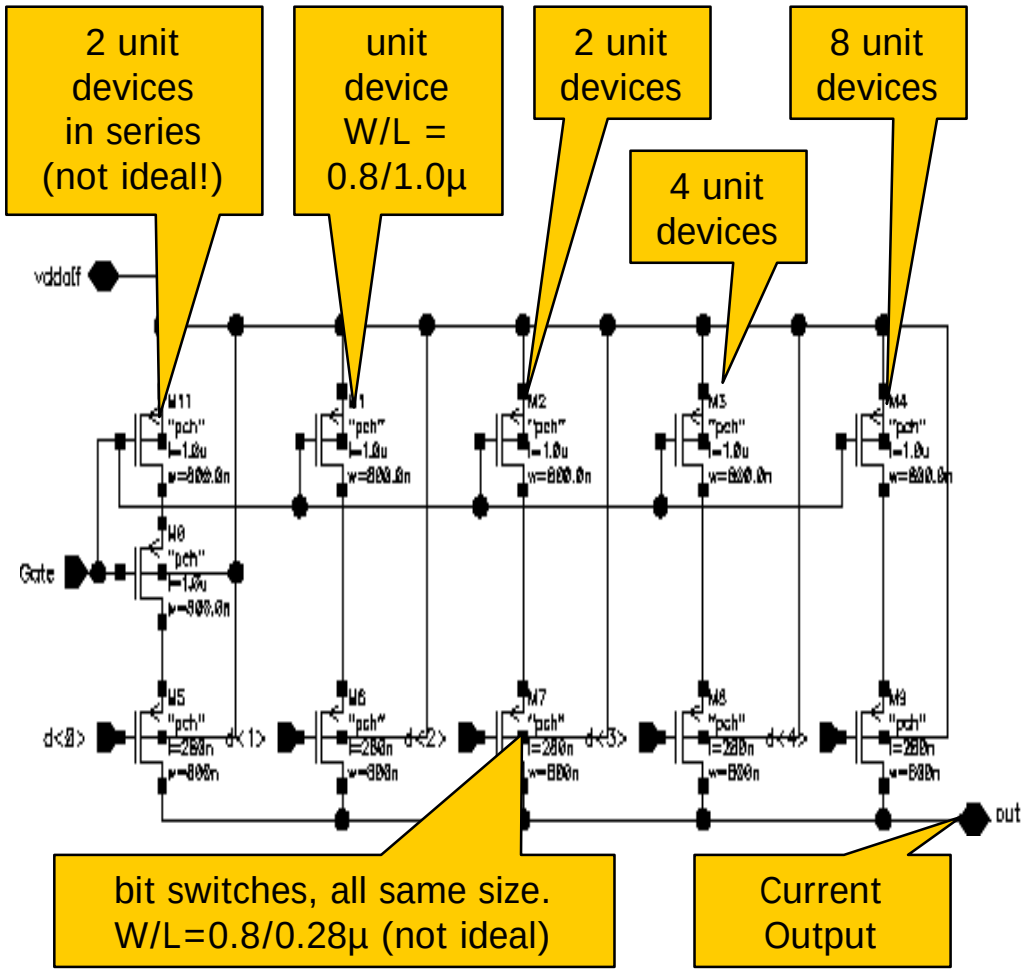


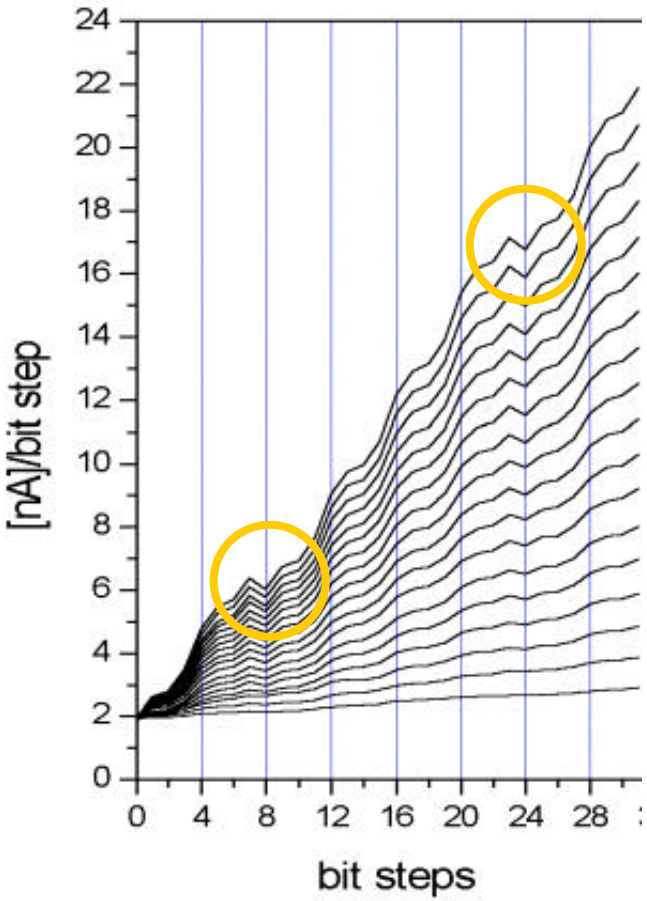
- Proposed solution:
  - Use ToT amplitude measurement to correct time stamp of hits with small amplitude by 1
  - This 'global' ToT cut requires trimming of ToTs in every pixel (5 bit DAC)
- Circuit works as expected. Performance on full chips/modules needs to be studied.

Some details: 5 bit pixel trim DACs

- Simple circuit:
  Scaled PMOS devices + switches

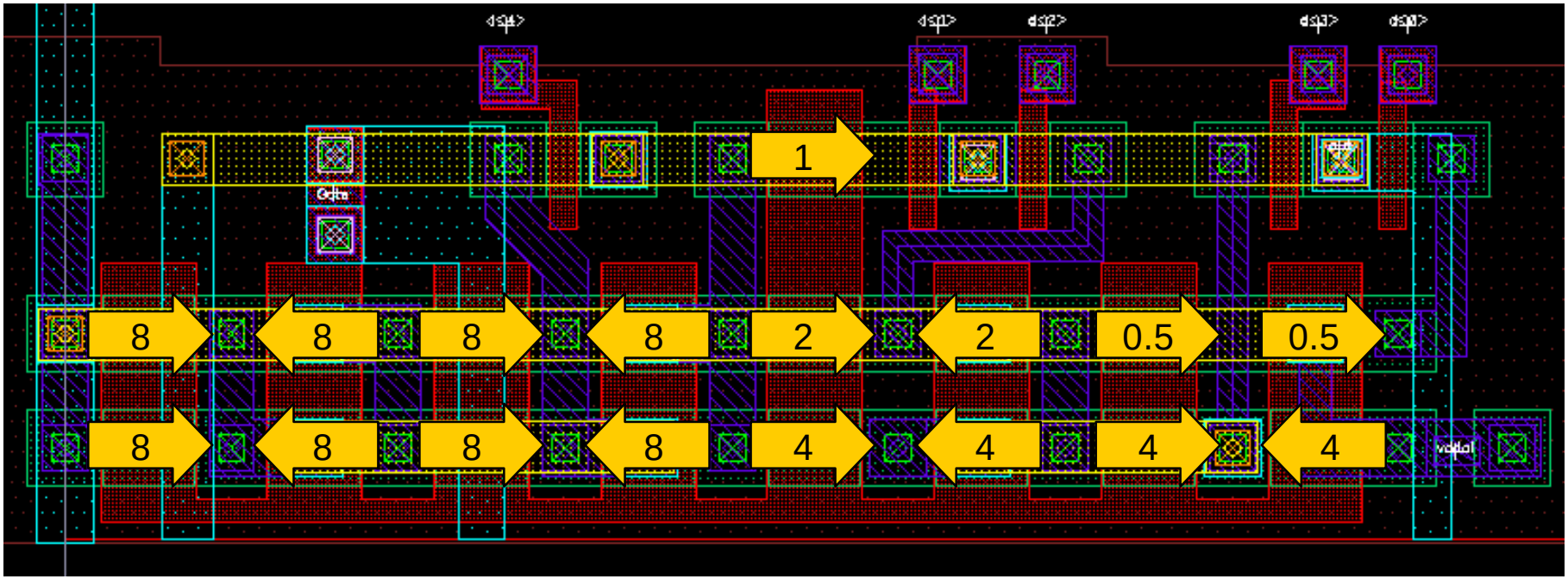
- Problem:
  Nonlinearities at 7⇒8 and 23⇒24





5 bit pixel trim DAC layout

- Layout balances current flow direction in multiple transistors



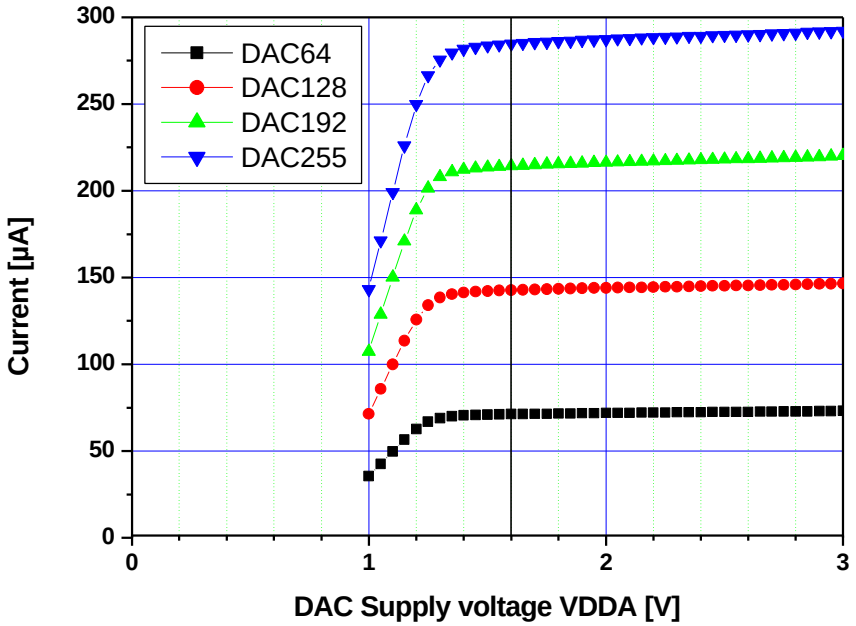
- Non-linearity is explained by large up/down current difference: Assume lower MOS have current a, upper MOS have current b (b<a)
  - Step at 7 ⇒ 8: 3.5b ⇒ 4a Nonlinearity of 4*(a-b)
  - Step at 15 ⇒16: 3.5b+4a ⇒ 4b+4a ok!
  - Step at 23 ⇒24: 7.5b+4a ⇒ 8b+4a Nonlinearity!

⇒ Matching of devices with different surrounding is very bad !

Global 8 bit DAC

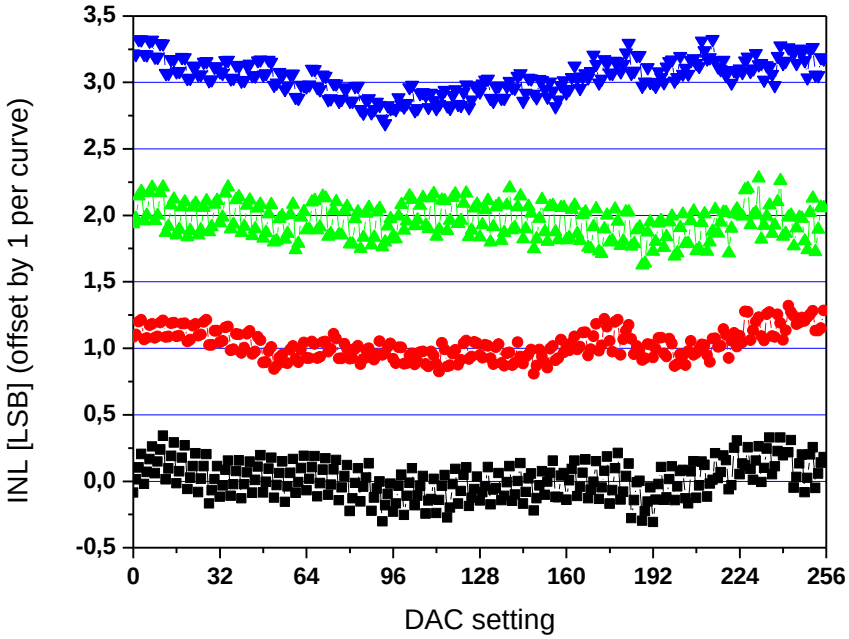
- Uses 64 unit current sources in a 8 x 8 matrix, the 2 LSBs are down scaled sources
- Used for global biases and charge injection (9bit)

I_{out} vs. Supply voltage



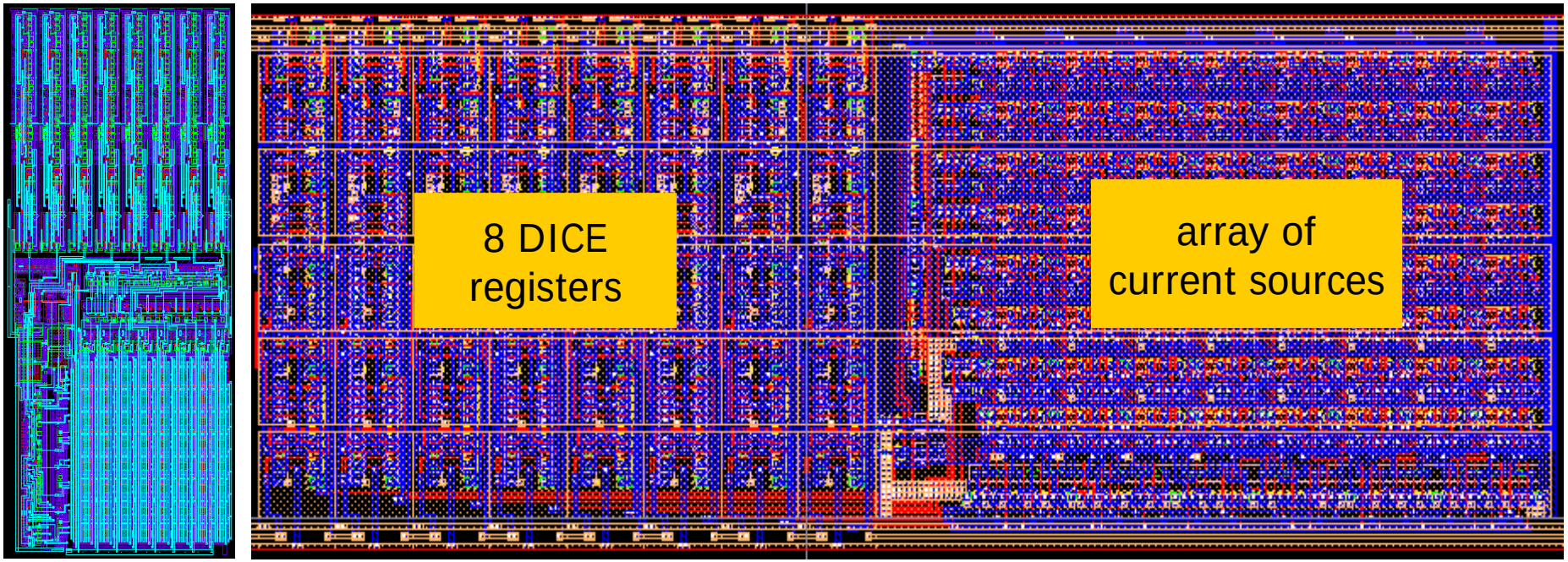
Operation ok at VDDA = 1.4 V

Integral Nonlinearity (4 DACs)



INL < 0.5 LSB – true 8 bit

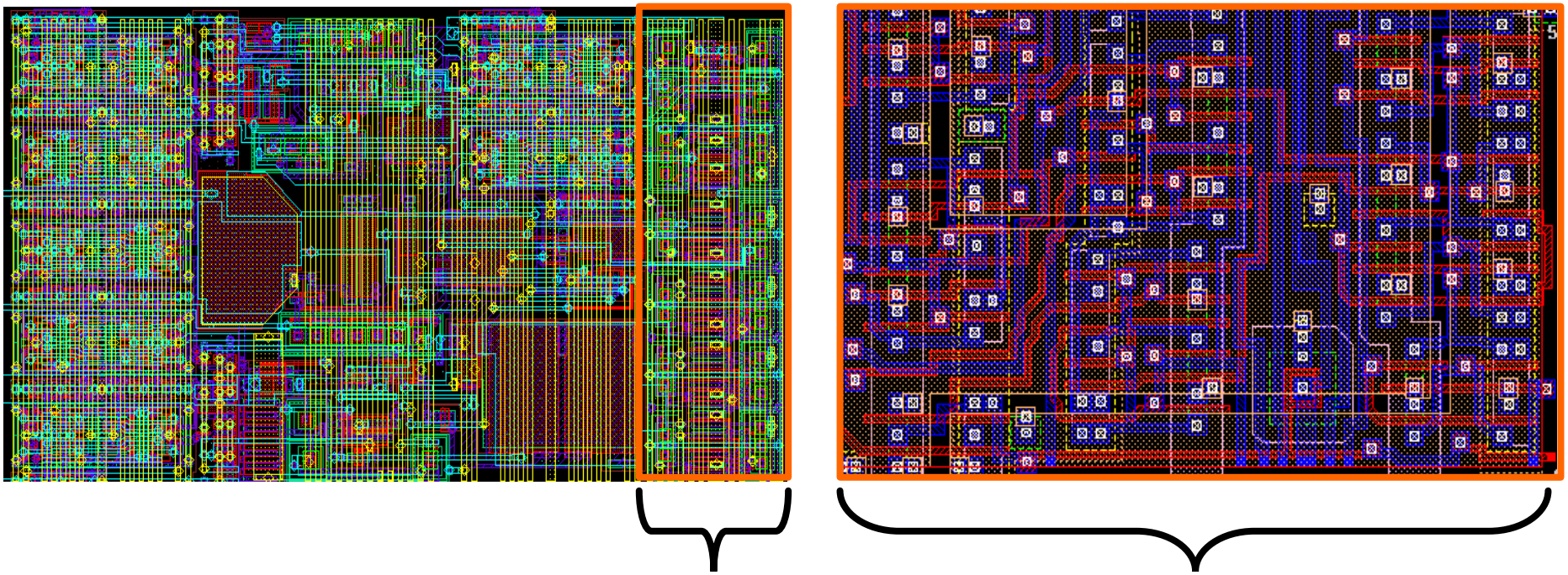
Layout comparison 0.8µm Û 0.25µm: 8 bit DAC



0.25µm 80x200 µm²	DMILL 0.8µm 500x200 µm²

- gain x 6 in mixed mode full custom layout

Layout comparison 0.8µm ⇔ 0.25µm: Pixel Control



0.25µm, 3 metals used:
63 devices, 16x50 µm²
< 1 day work

DMILL, 2 metals:
59 devices, 90x50 µm²
> 1 week work

Gain x 6 in density (full custom digital) with much less layout effort

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Short Introduction to ATLAS Pixel

- mechanics, modules and cooling

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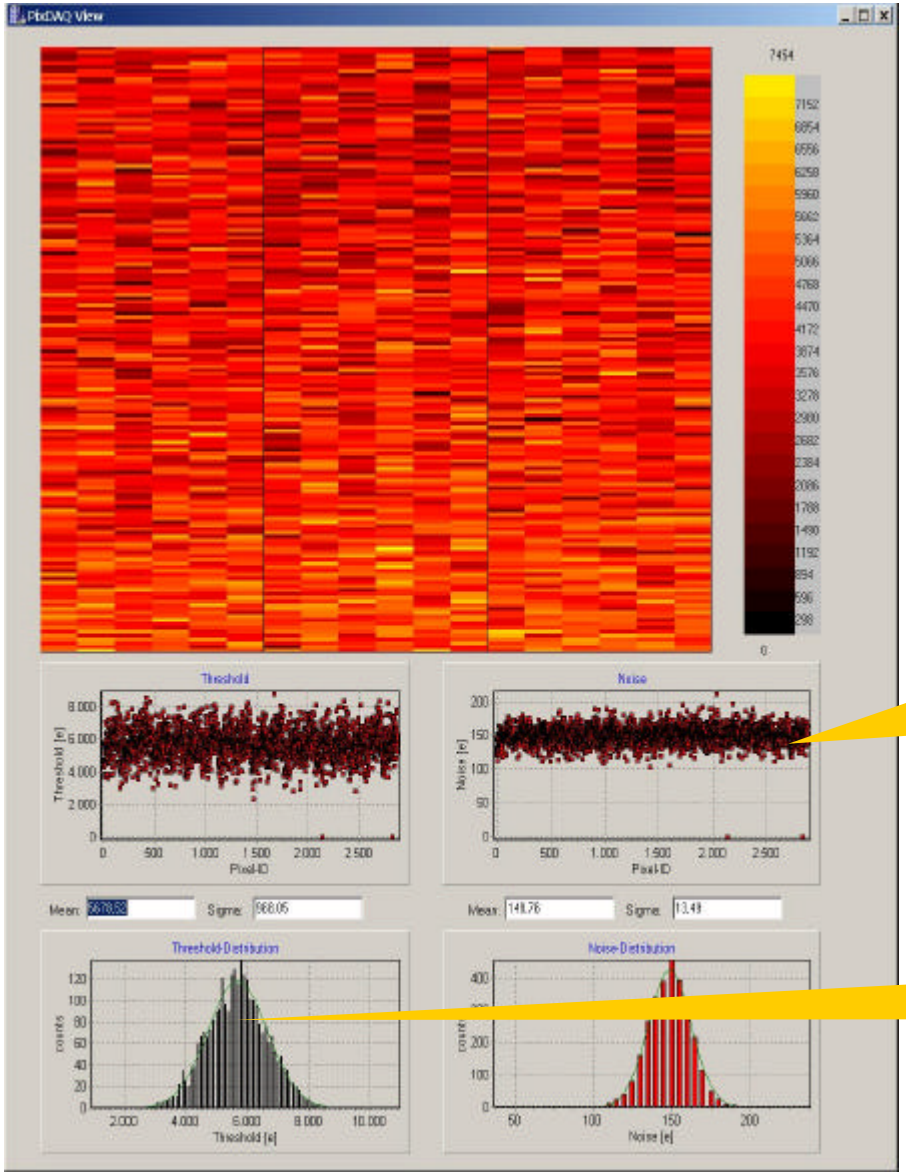
- analog section – block diagram, layout,
- digital readout
- some details

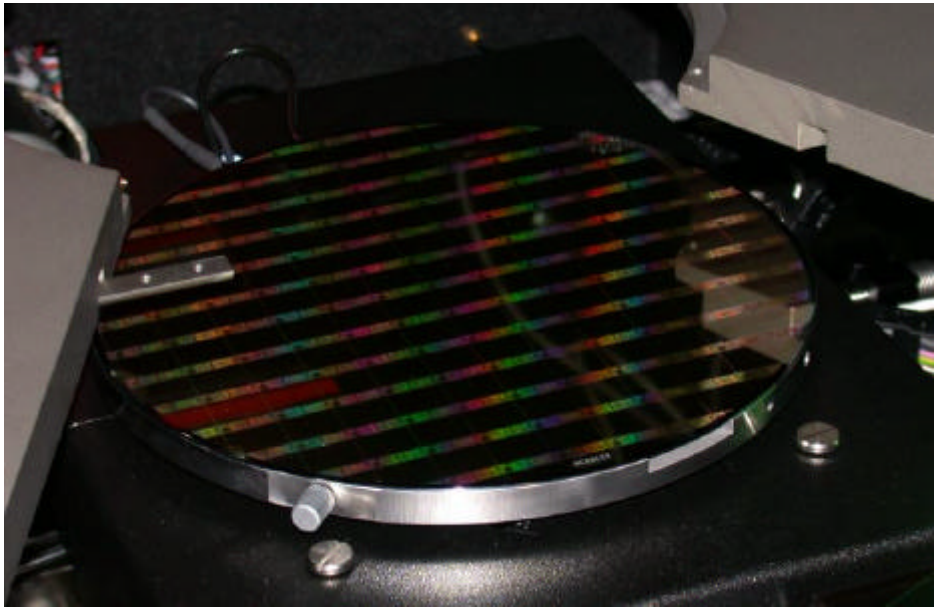
Results

- lab measurements, test beam, irradiation

Summary

Wafer tests – noise and thresholds

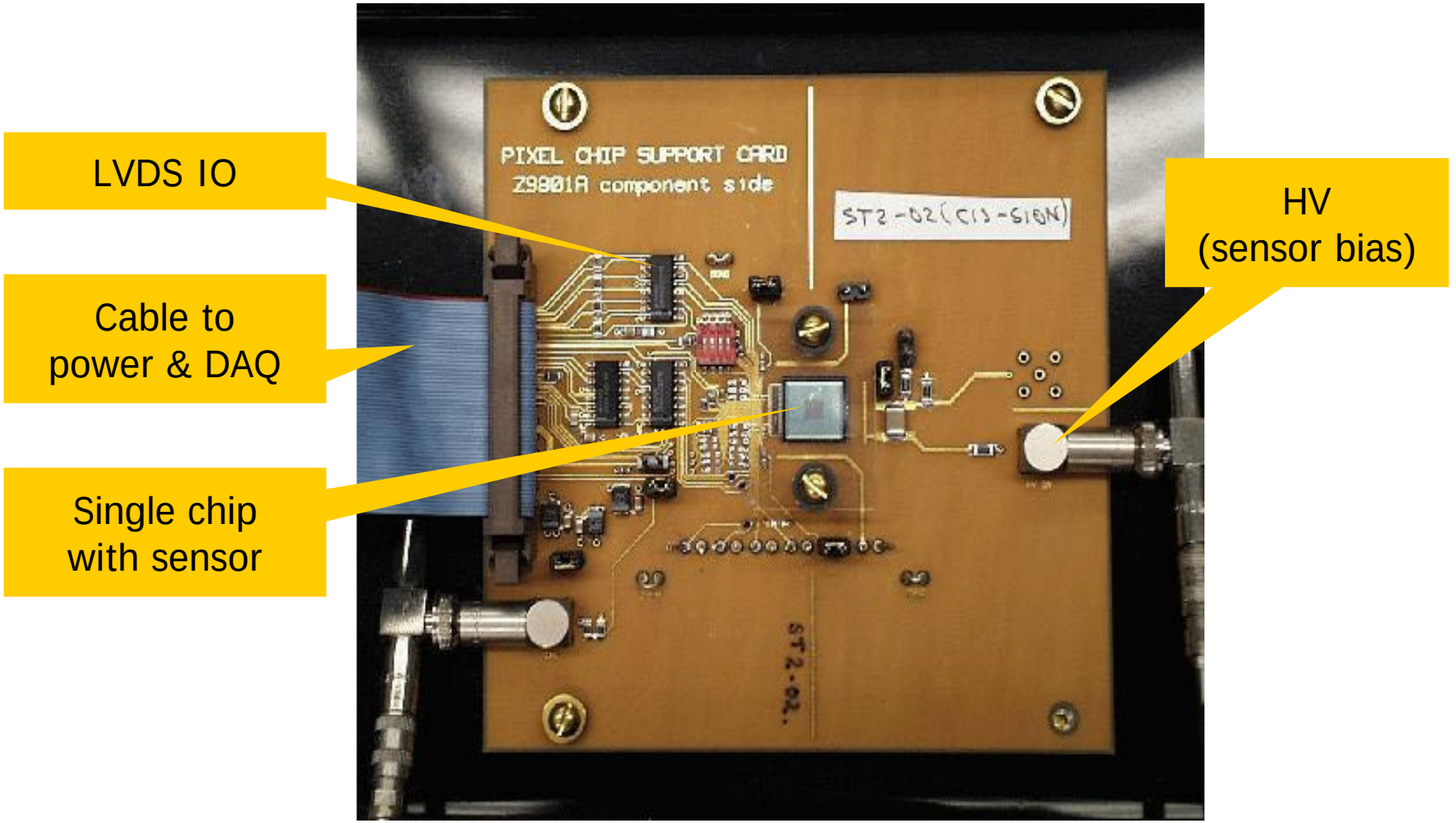




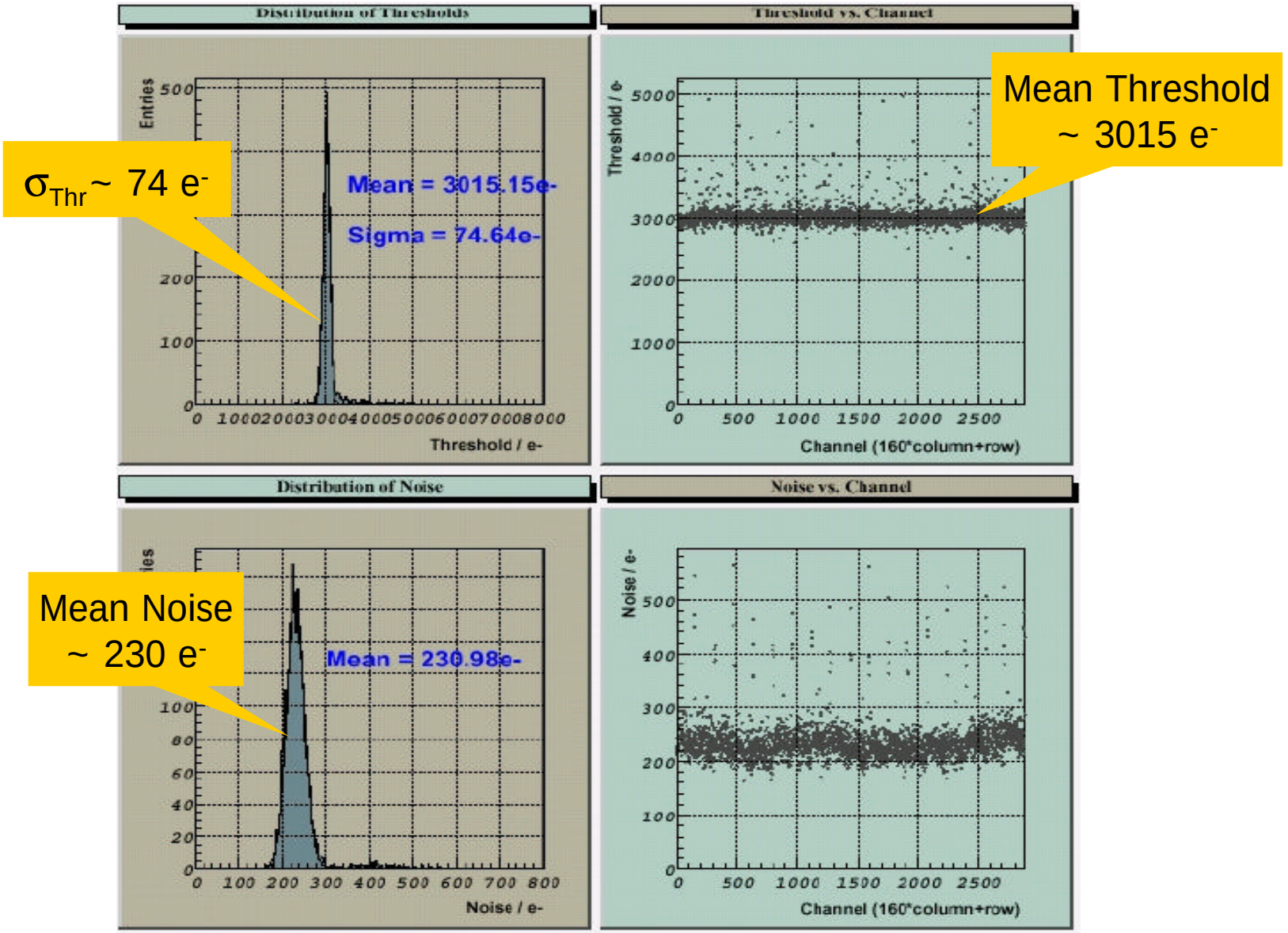
Noise 150 e$^-$
Same as on test chip !!

Untuned threshold
dispersion ~ 900 e$^-$

Single Chip with Sensor



Threshold and Noise after tune (FEI with Sensor)

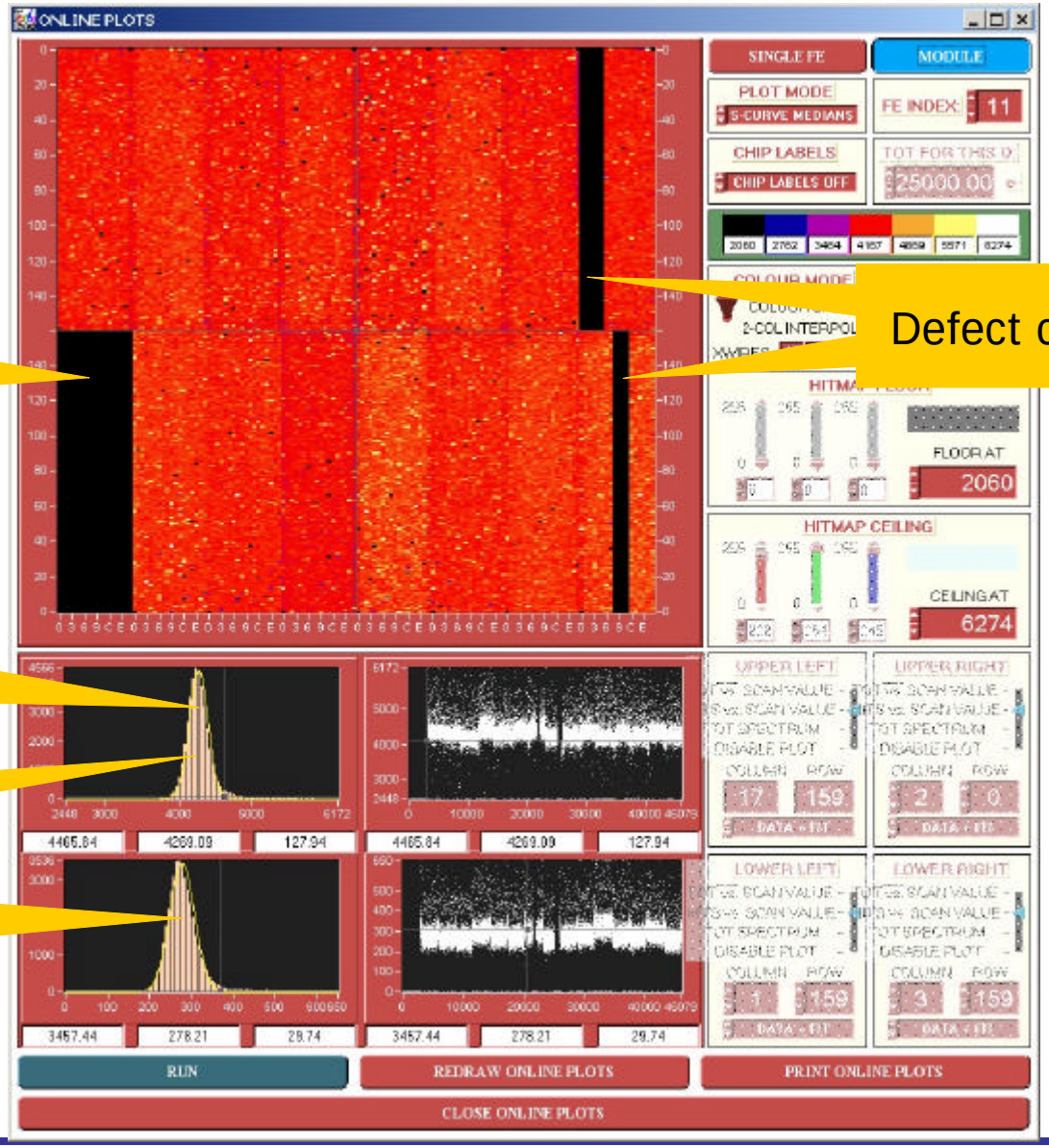


σ_{Thr} ~ 74 e$^-$

Mean Threshold ~ 3015 e$^-$

Mean Noise ~ 230 e$^-$

Full tuned FEI Module (Chips from 1st batch)



Bad chip

Defect columns

Mean Threshold
~ 4250 e^-

σ_{Thr} ~ 130 e^-

Mean Noise
~ 280 e^-

Testbeam

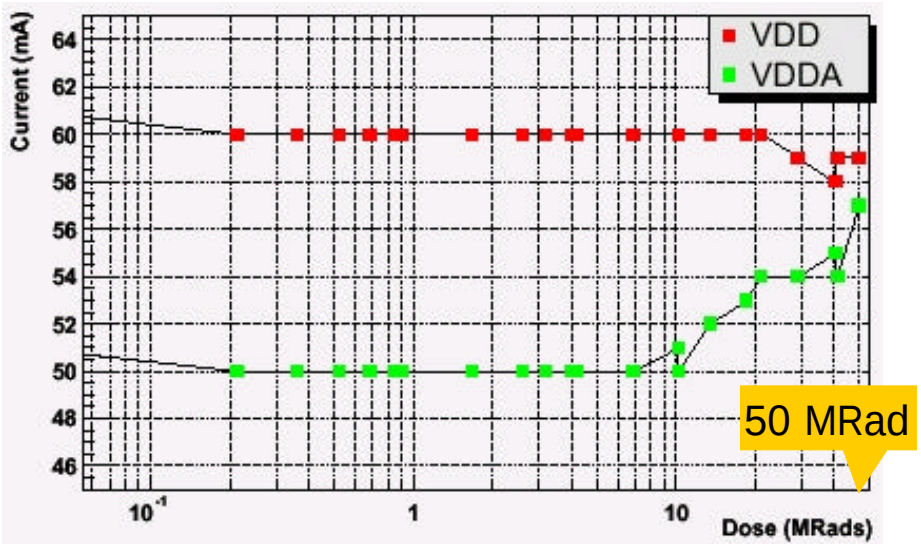
- 3 FEI Modules have been studied in a testbeam at CERN during the last weeks.
- New beam telescope & new software give us 10000 Events per spill!
- In total, 20 Millionen Events x 3 modules have been recorded

- Analysis is still ongoing

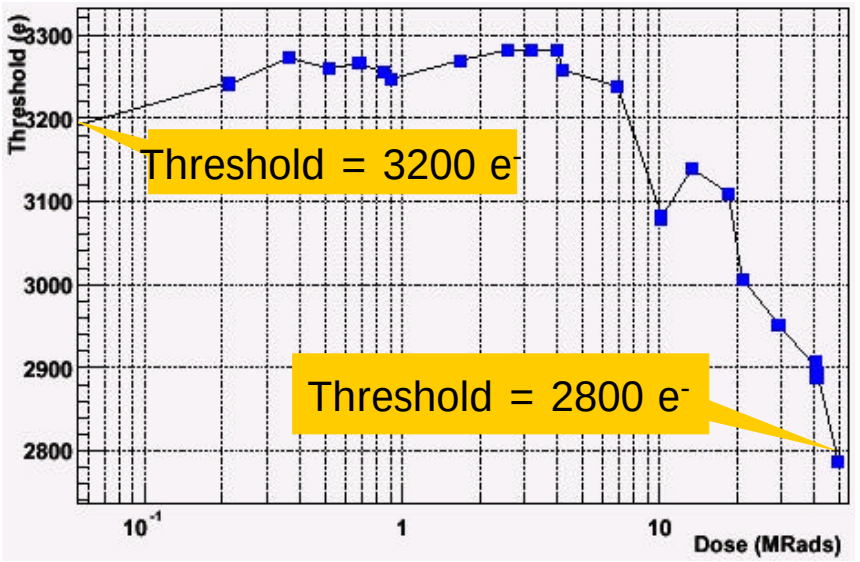
- Found no surprises so far. Resolution seems to be as before: σ_{all} = 13-15µm in short (50µm) pixel direction.

Radiation hardness studies

- Irradiations have been performed at LBNL (88'' Cyclotron) and at CERN PS
- Dose was up to 50/60 Mrad (This is expected after 10 years of LHC operation)
- The bare chips were operated during irradiation
- Chips are still fully functional after this dose
- Some (preliminary) results:

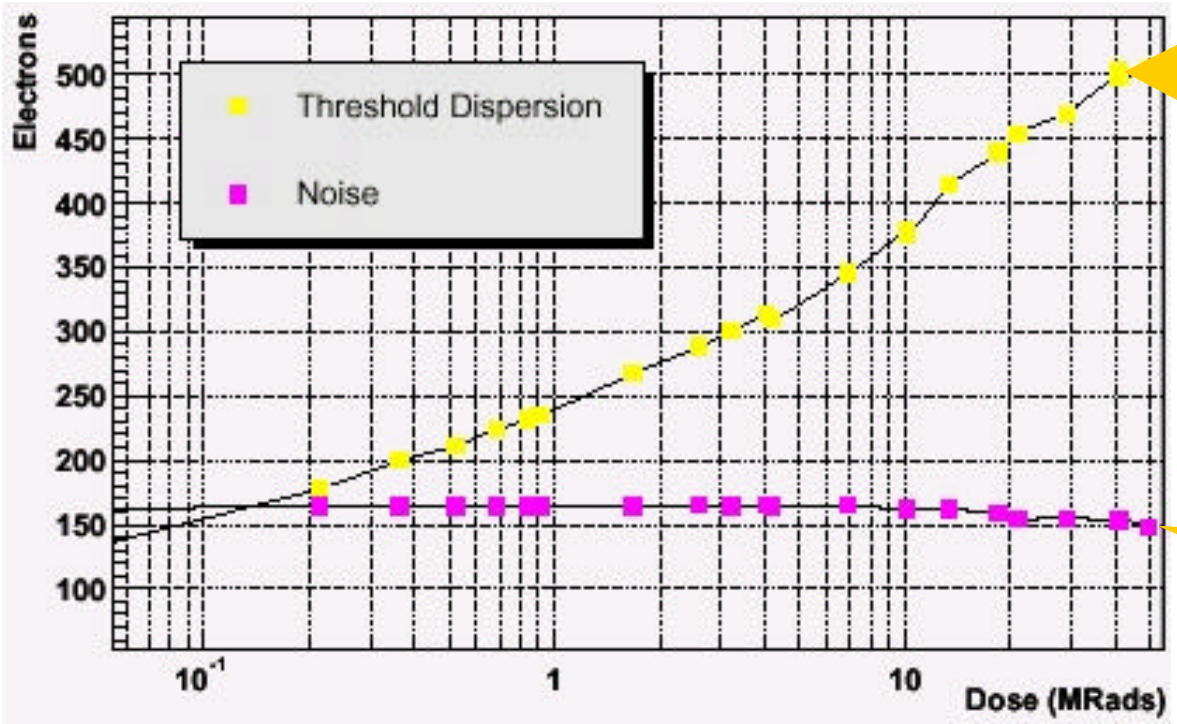


Small change in analog and digital supply currents



Small change in threshold (no change in bias settings!)

Radiation hardness studies



Threshold dispersion on tuned chip increases (chip can be re-tuned)

This radiation-induced Mismatch needs to be understood!

No change in noise !

The ATLAS Pixel Chip FEI

Short Introduction to ATLAS Pixel

- mechanics, modules and cooling

The Front End Chip FEI

- analog section – block diagram, layout,
- digital readout
- some details

Results

- lab measurements, test beam, irradiation

Summary

Summary

- The ATLAS pixel front end chip FEI (0.25µm) functions completely.

- On full modules, we find a Noise < 300e^-, threshold dispersion < 150e^- after tune.
- No problems after irradiation to full ATLAS dose of 50MRad have been found
- Power consumption is below baseline (Iddd ~ 62 mA, Idda ~ 50 mA)
- Chip has many new features
  (On-chip injection chopper with 2 ranges, 2x5 bit trim per pixel, time walk correction, leakage measurement, column mask, SEU tolerant latches, testability,...)

- A slightly improved 'pre-production' design will be submitted end of this year
  - Reduce initial threshold dispersion
  - Improve 5 bit pixel DACs
  - Improve bias distribution (to upper pixels)