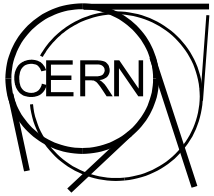


Fast CMOS Transimpedance Amplifier and Comparator circuit for readout of silicon strip detectors at LHC experiments

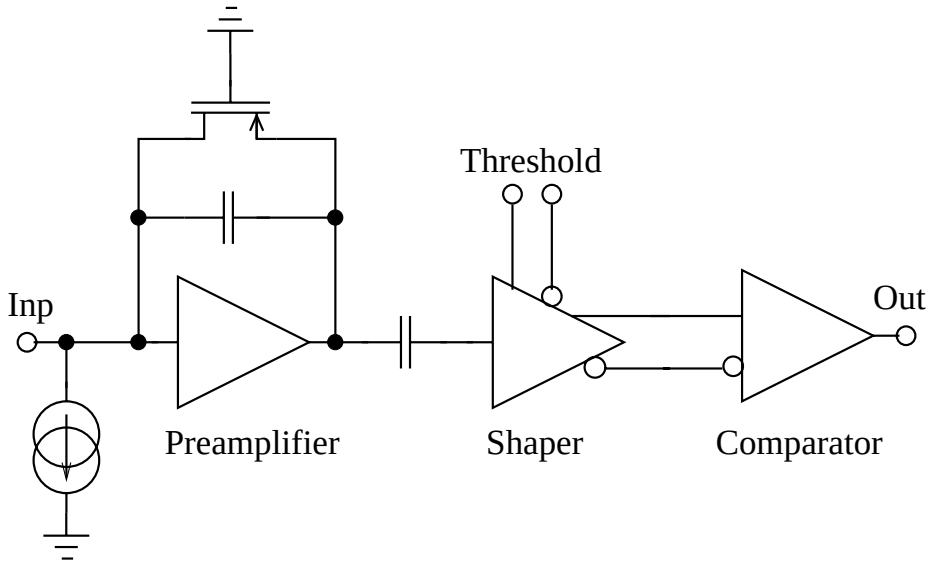
Jan Kaplon - CERN

Wladek Dabrowski - FPN/UMM Cracow
Pepe Bernabeu – IFIC Valencia
Carlos Lacasta – IFIC Valencia
Robert Szczygiel - INP Cracow

Motivations

- ➔ Check the feasibility of the designing of the fast amplifier/comparator FE optimised for long strip SSD in CMOS 0.25µm technology
- ➔ Design follows the specifications for readout chip for ATLAS SCT
  - → Detector capacitance in the range of 20pF (30pF max)
  - → ENC in the range of 1500e- for 20pF input capacitance
  - → 20ns peaking time
  - → time walk for 1.2 – 10fC signal → <16ns (1fC threshold)
  - → matching of the comparator → better than 5% of 1fC signal (sigma spread)

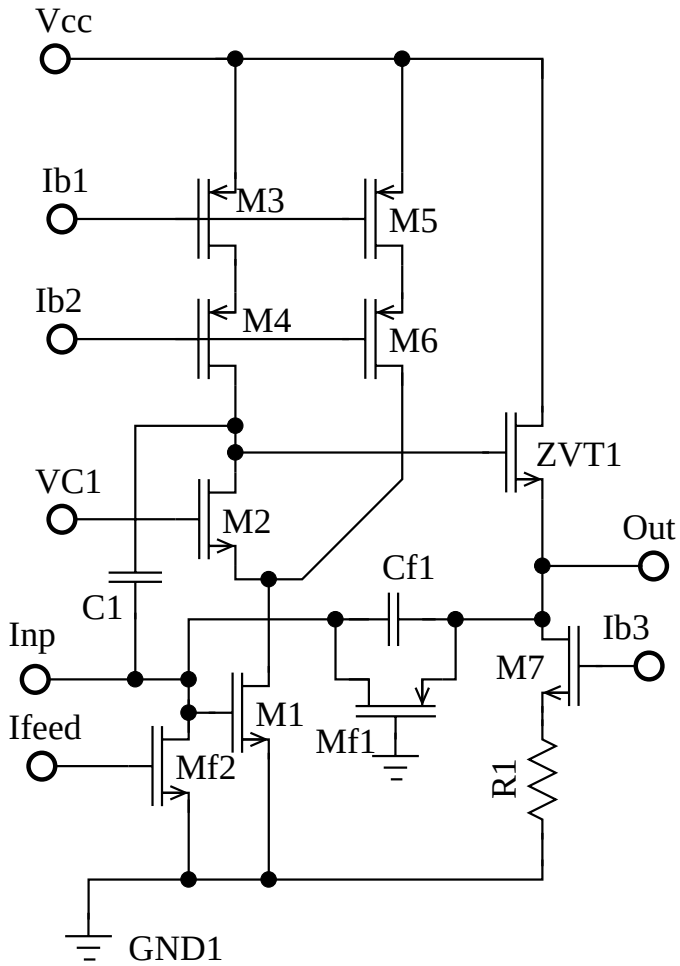
Architecture of the Front-End channel

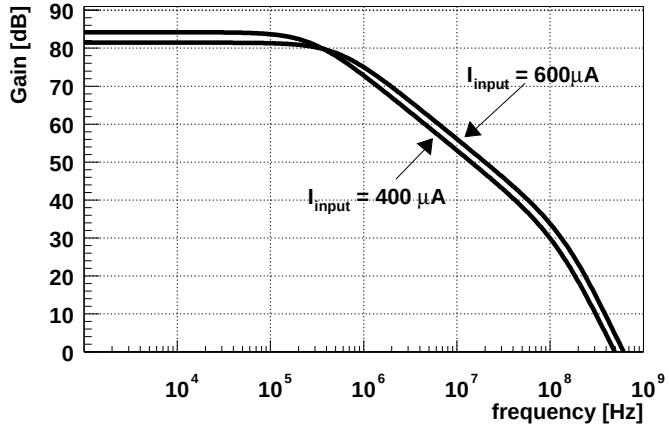


One channel comprises three AC coupled blocks:
- fast, transimpedance preamplifier (12ns peaking time)
- shaper (peaking time 20ns)
- differential discriminator

Why AC?
- limiting the matching problem to the differential discriminator
- improving robustness of the design against low frequency drifts (1/f noise, low frequency interferences)
- Improving the PSRR of the circuit in low frequency range
- relatively easy layout (42µm pitch)

Architecture of the Preamplifier

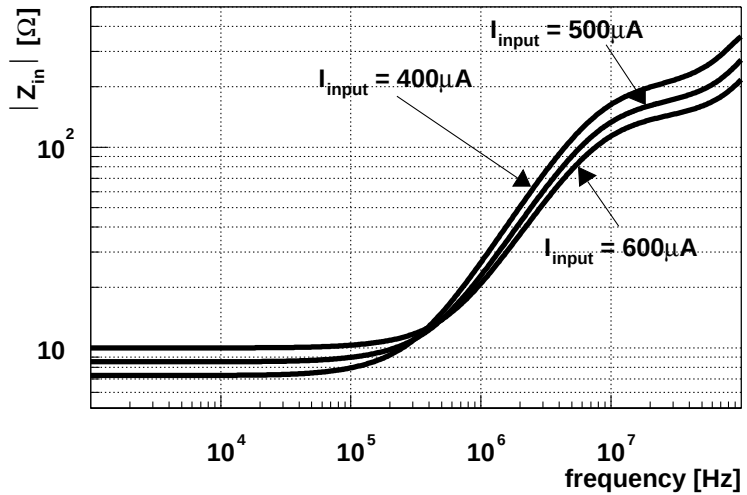


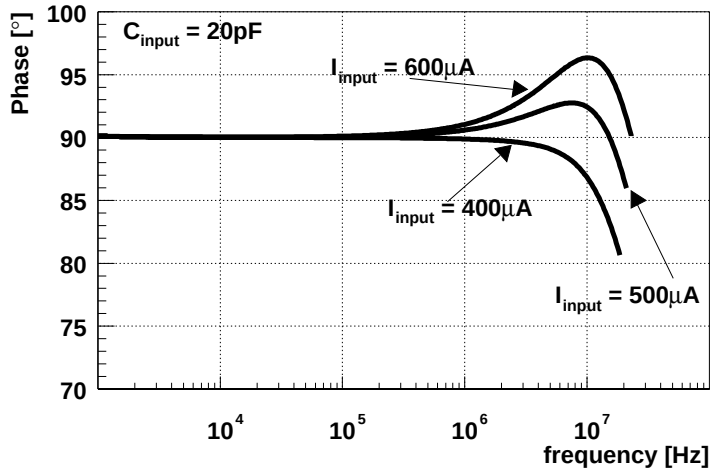


Bandwidth ➔ ~600MHz
Open Loop Gain ➔ ~83dB

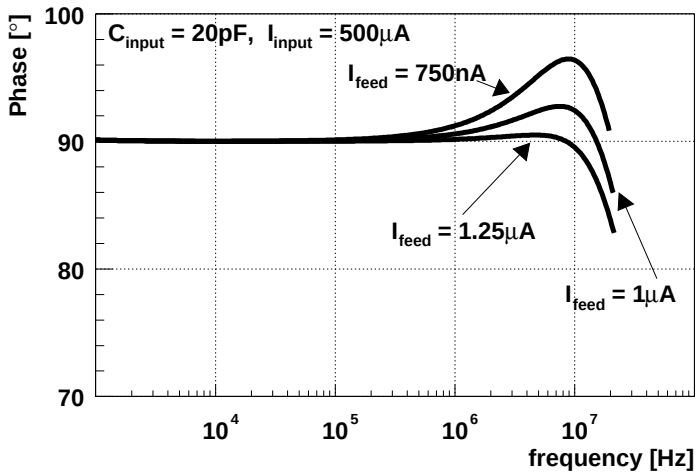
Cascode amplifier with active feedback
Input transistor M1 ➔ 3000µm/0.5µm
Bias ➔ 400 - 700µA (equivalent to 9 -16mS)
Feedback current ➔ 700nA – 1.6µA
(Rfeed → 150 – 75kOhm)

AC characteristic of the Preamplifier



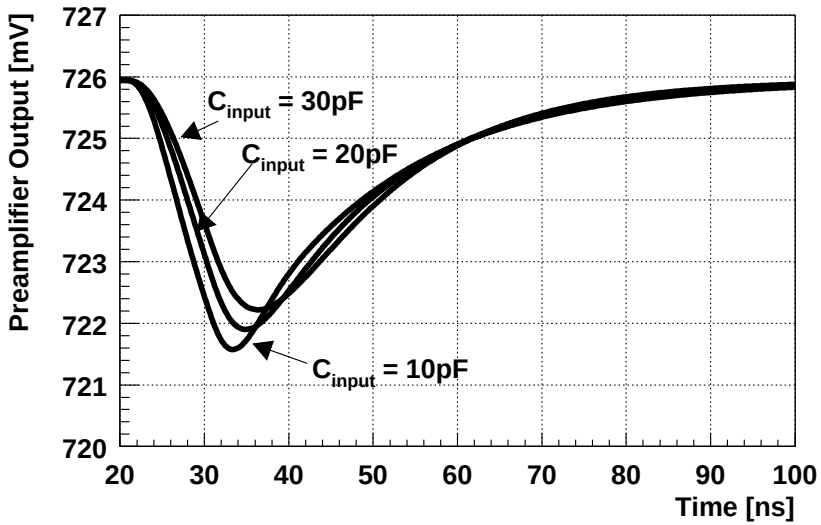


Input resistance ➔ 100 – 150 Ohm at 10MHz



Phase margin ➔ better than 80°
➔ adjustable with Ifeed

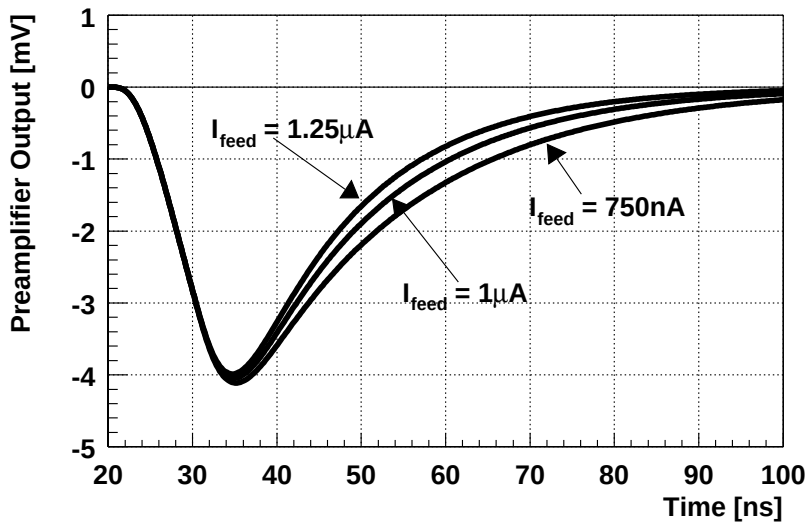
Preamplifier responses to 1fC



Responses for various Cdetector.

Feedback current ➔ 1μA
Input current ➔ 550μA

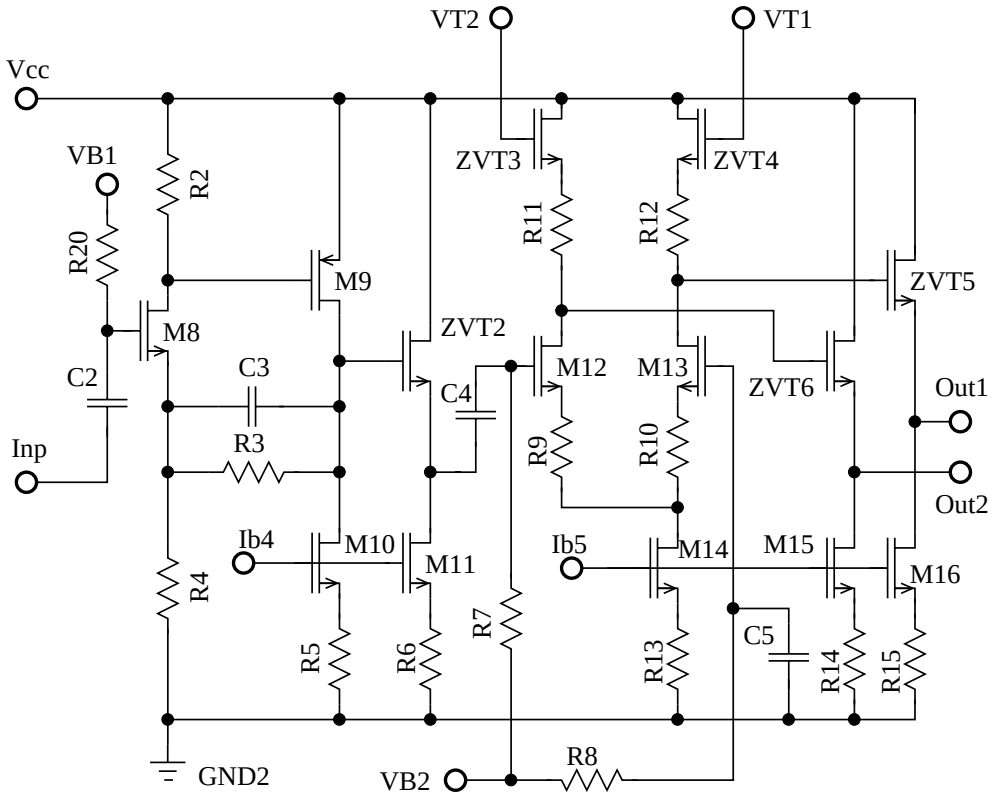
Peaking time ➔ 12 –14ns
Gain ➔ ~4mV/fC



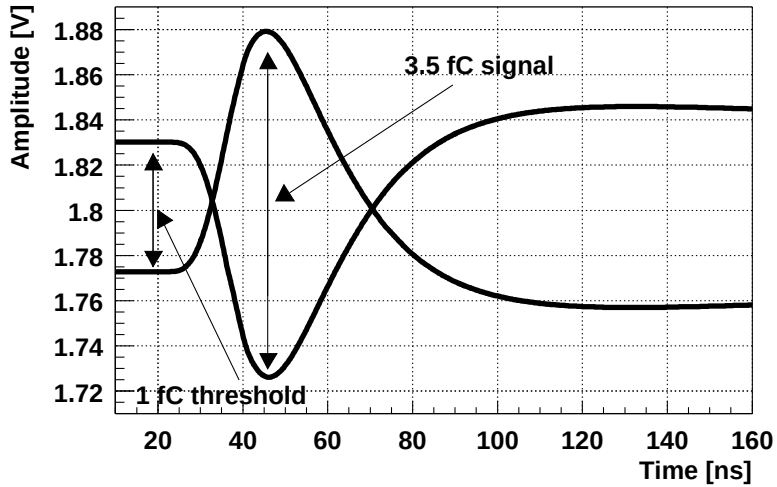
Responses for various feedback currents.

Input capacitance ➔ 20pF
Input current ➔ 550μA

Architecture of the Shaper stage

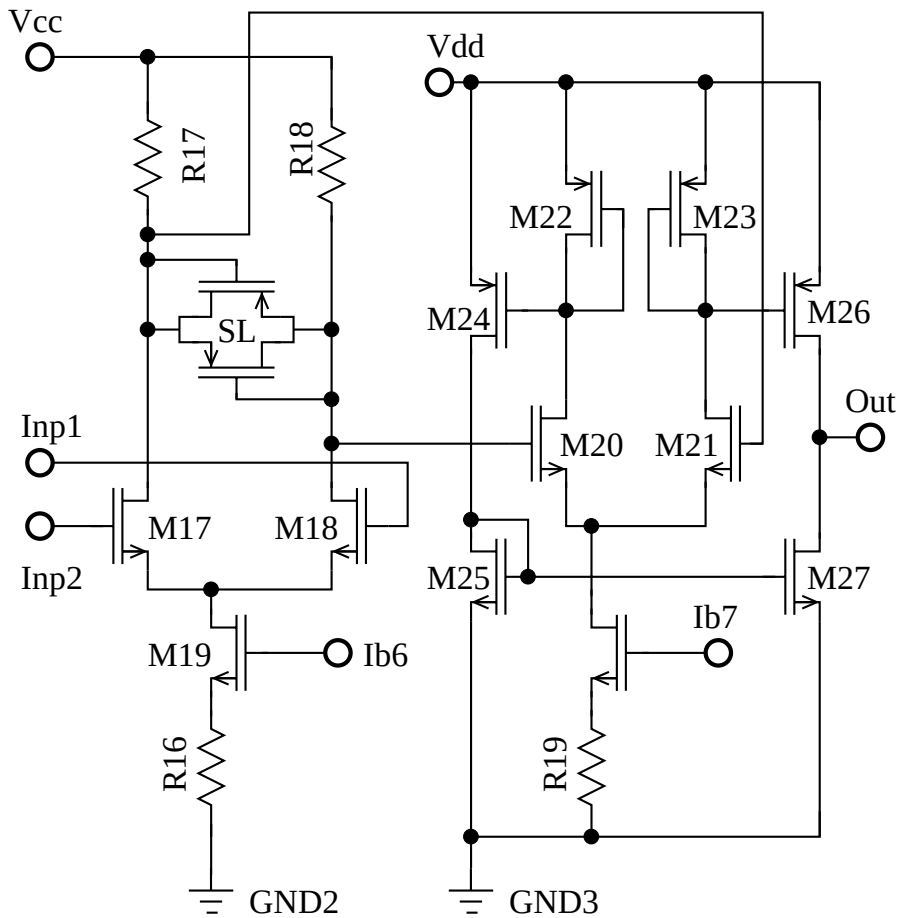


Schematic diagram of the shaper stage.
Pulse gain ➔ ~15 V/V (60mV/fC with preamp)
Peaking time ➔ 20ns

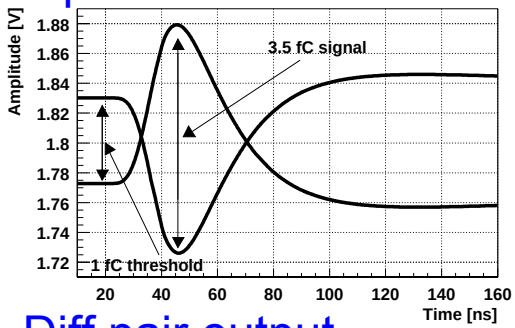


Response to 3.5fC charge seen at the differential output.
The signals are DC separated by the threshold voltage VT2-VT1).

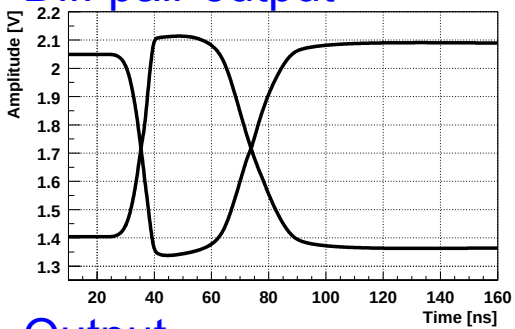
Architecture of the Discriminator



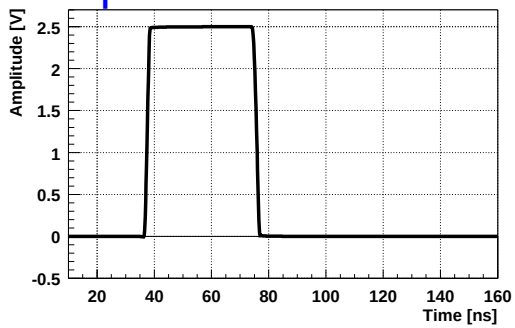
Input



Diff pair output



Output

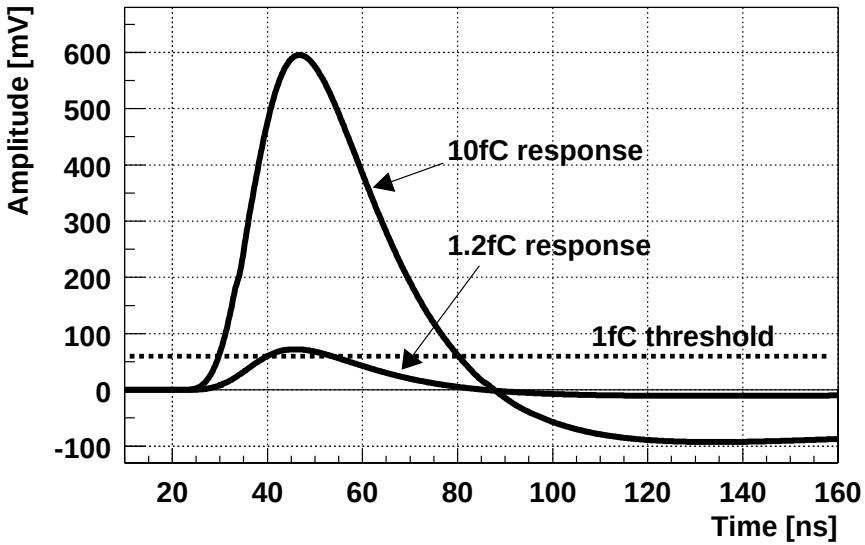


DC gain ➔ ~90dB

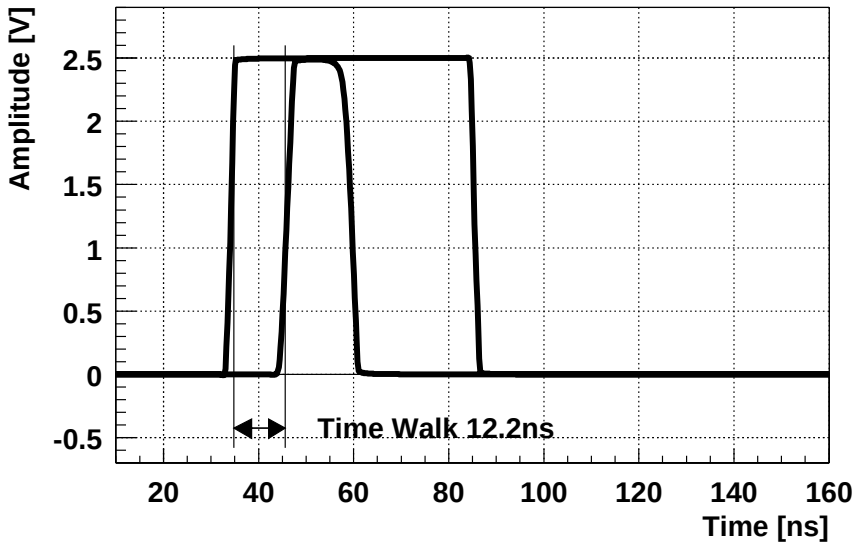
Min overdrive for 20ns pulse ➔ ~3mV (< 1σ noise)

Calculated offset spread (RMS) ➔ 4.5mV

Time walk simulation



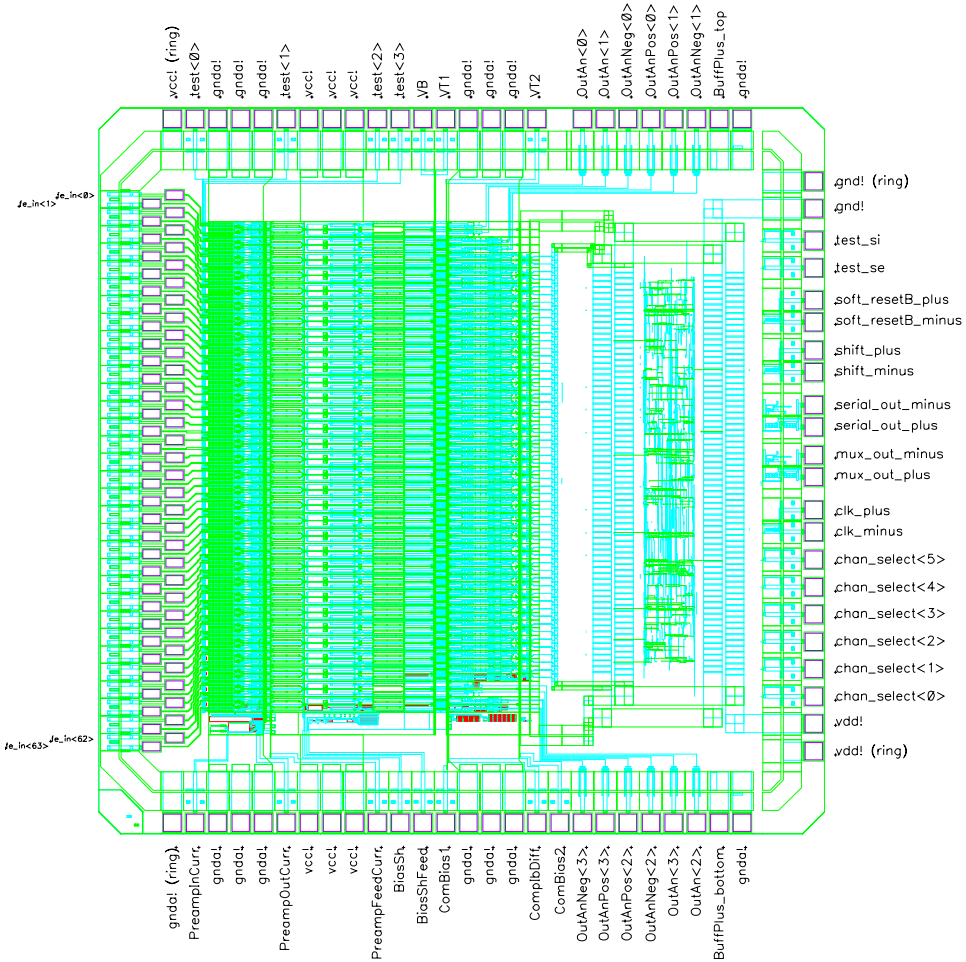
Comparator input



Comparator output

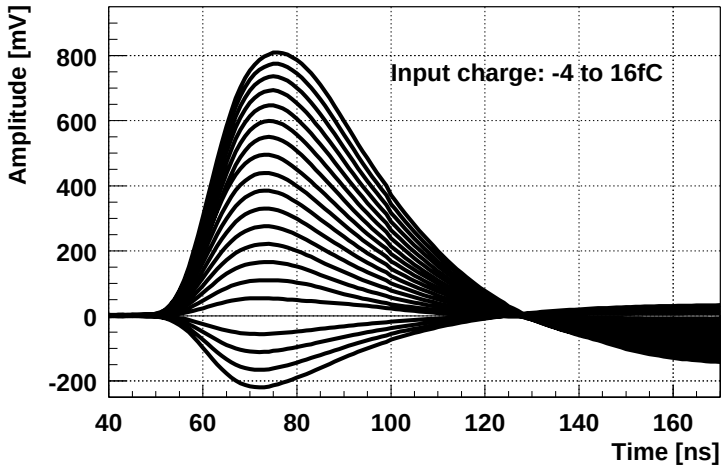
Time walk defined as the difference of comparator response delays for input charges of 1.2fC and 10fC with threshold set to 1fC.

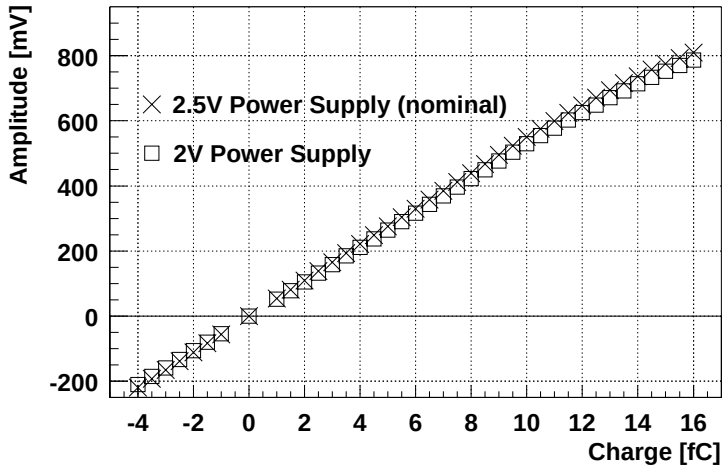
Layout and testability



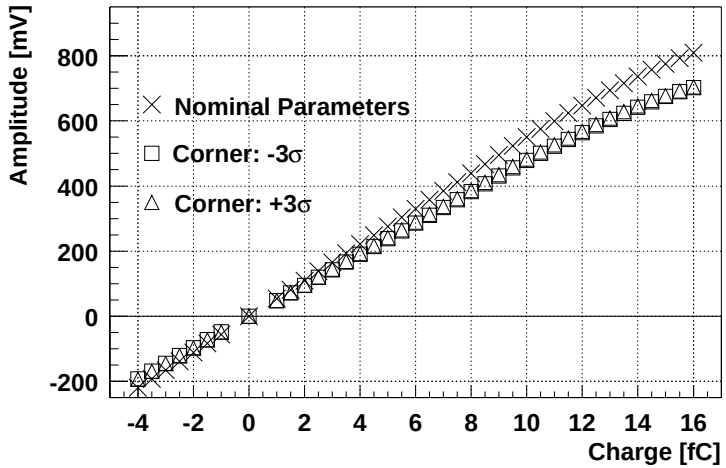
1. 56 full channels including preamplifier, shaper and comparator – readout via serial output register
2. 8 analogue test channels including preamplifier, shaper and comparator input stage – readout directly via output buffers
3. Biases and threshold voltage - external
4. Four calibration lines distributing input signals every fourth channel
5. Chip area – 4 x 4mm^2, dimensions of the channel – 42µm x 2mm

Response of the analogue chain

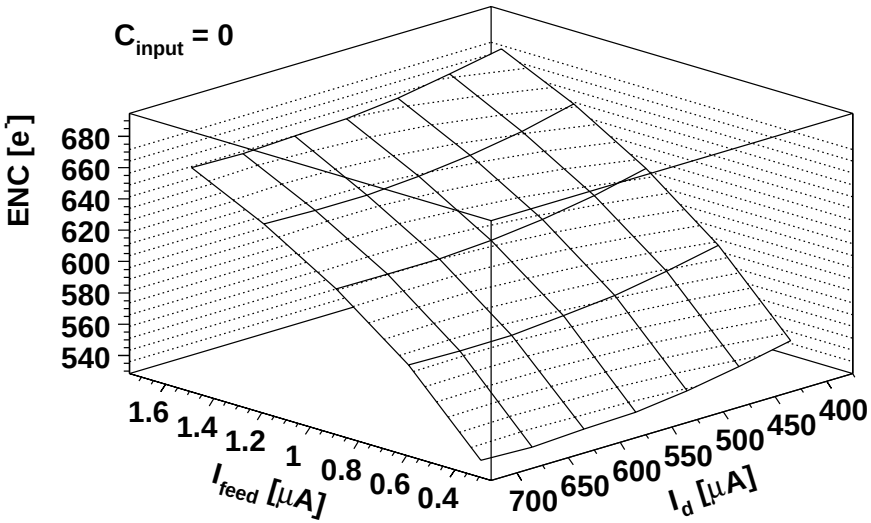


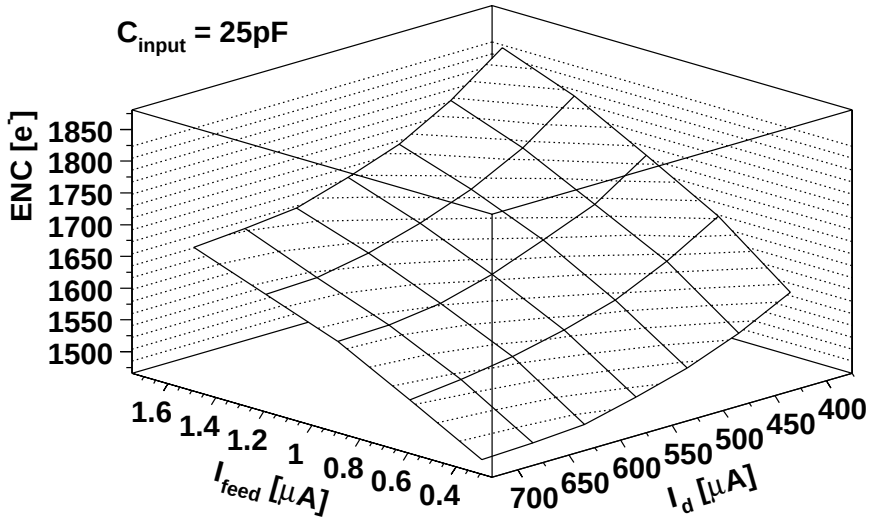


Peaking time ➔ 20ns, semigaussian
Gain ➔ ~55mV/fC
Dynamic range ➔ 0 – 12fC
Linearity ➔ better than 5% inside the dynamic range and limited power supply and extreme corners of technology



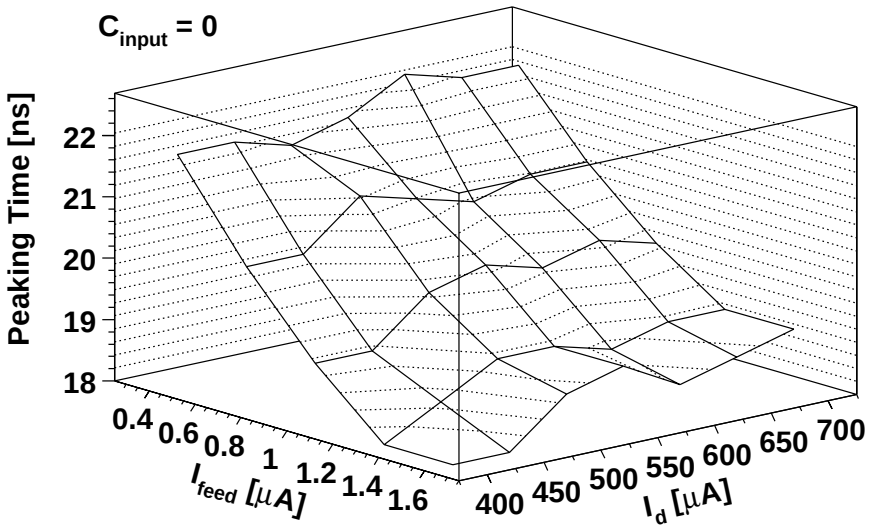
Single analogue channel - ENC

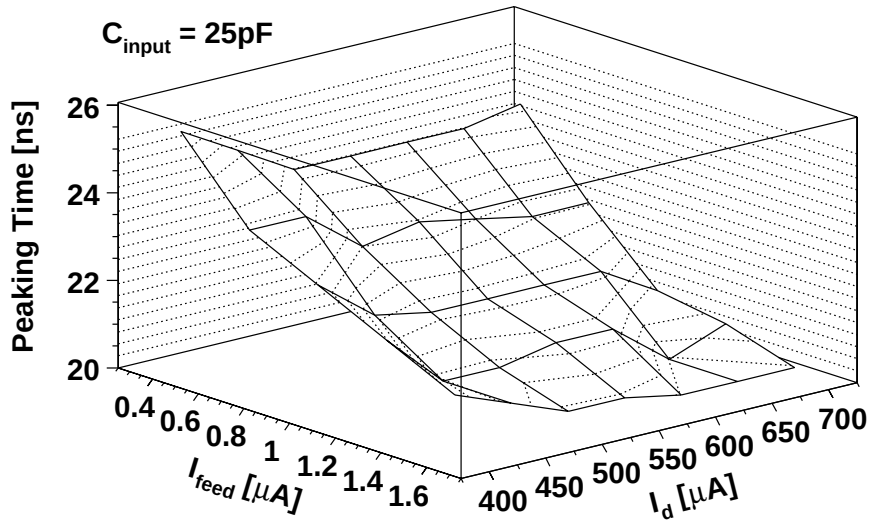




ENC of the analogue channel as a function of feedback and input bias current.

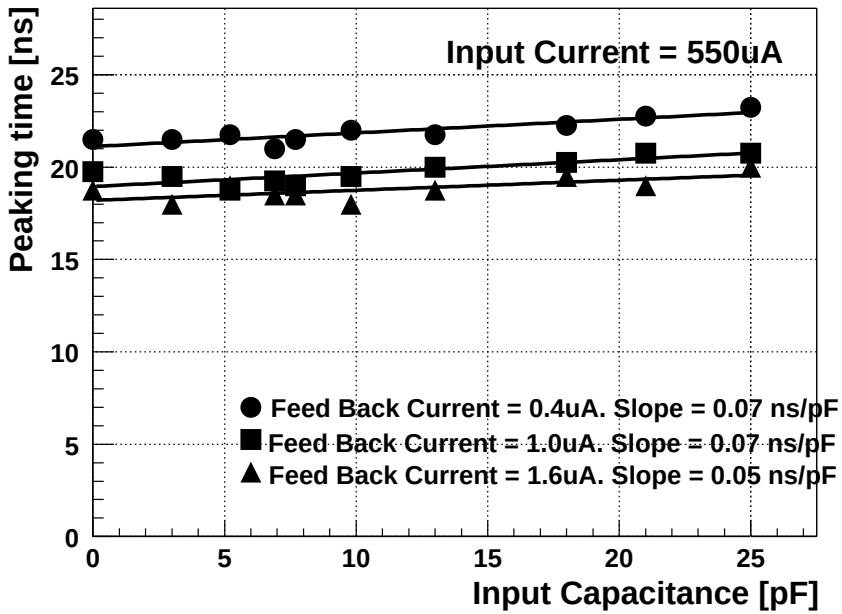
Single analogue channel – Peaking Time

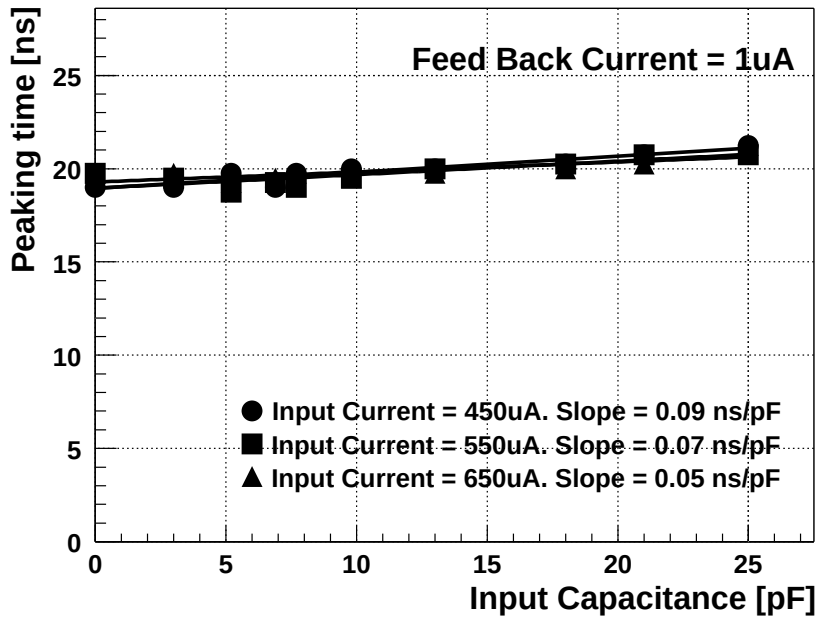




Peaking time as a function of feedback and input bias current.

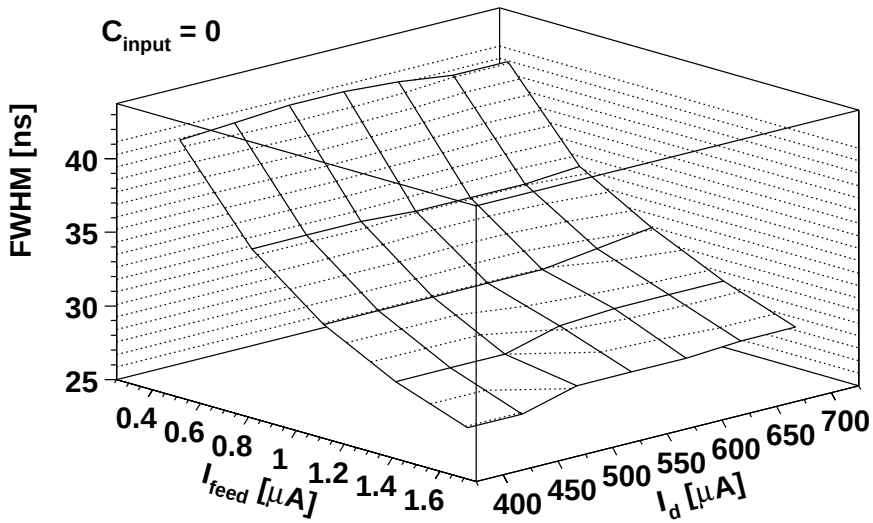
Single channel – Peaking Time vs. input capacitance

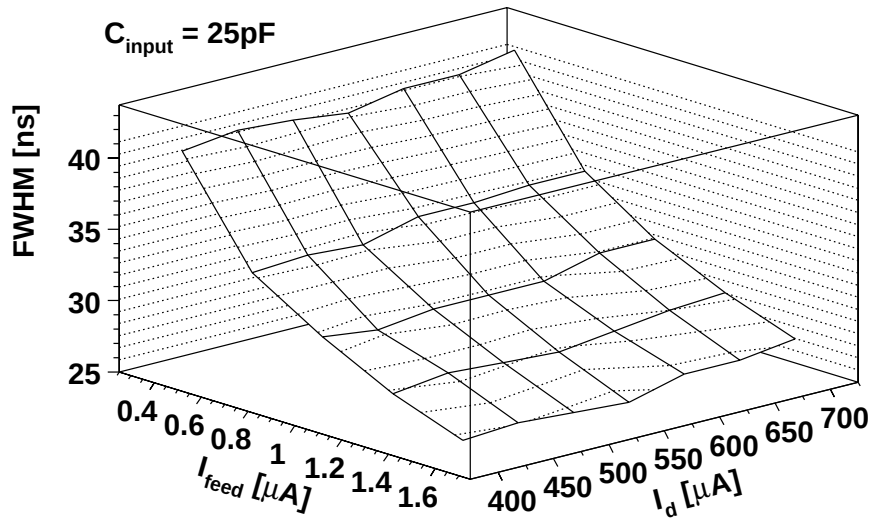




Peaking time as a function of input capacitance for different feedback and input bias currents.

Single analogue channel – FWHM

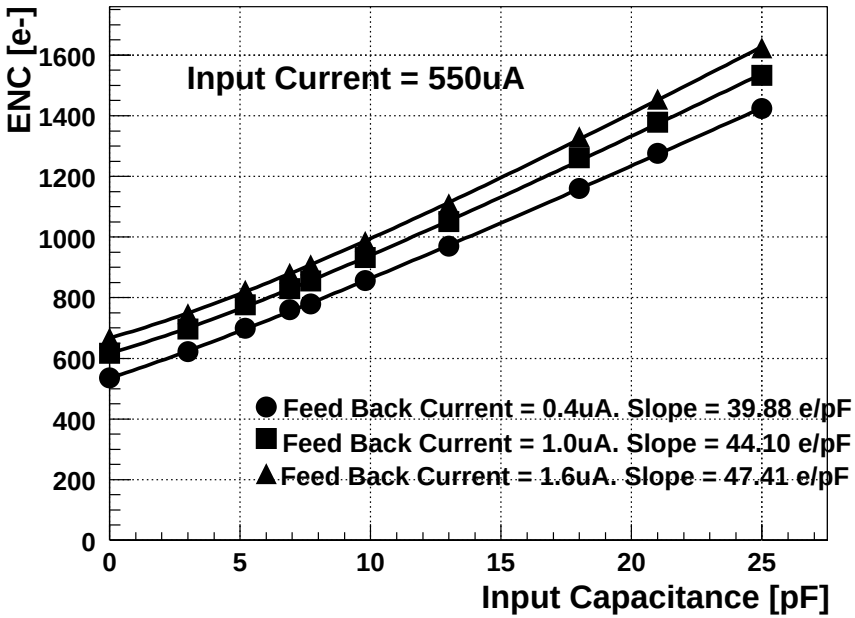


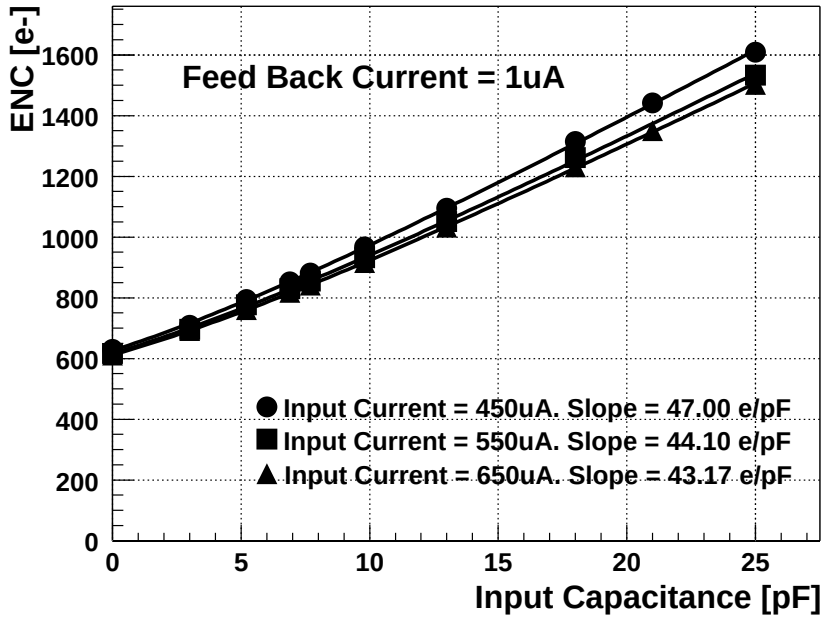


FWHM as a function of feedback and input bias current.

FWHM for ideal CR-RC3 ➔ 1.38 × Peaking Time

Single channel - Noise slope





ENC as a function of input capacitance for different feedback and input bias currents.

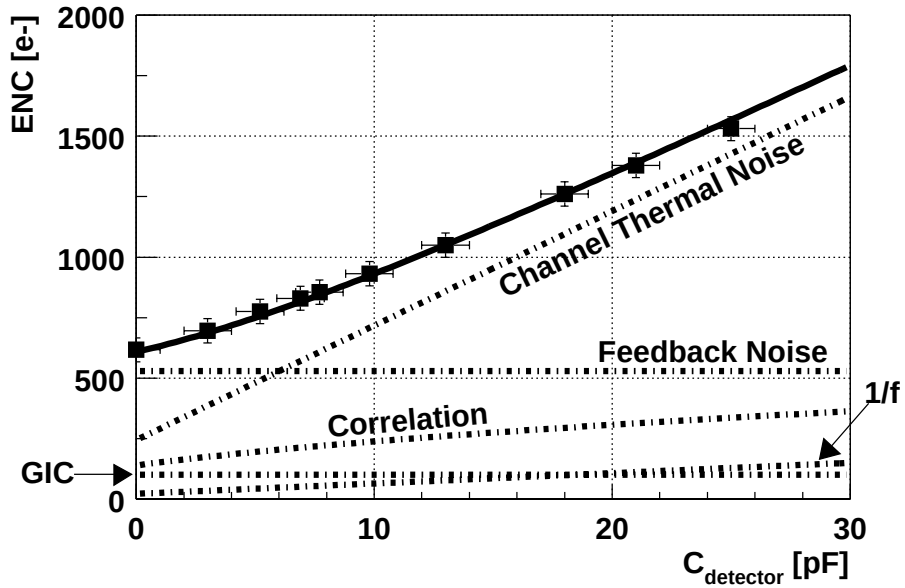
Estimation of the noise performance

Components:

➔ Channel thermal noise
➔ GIC noise
➔ Correlation term GIC ⇔ thermal noise
➔ Flicker noise

Assumptions:

➔ Γ excess noise factor → 1.3
➔ n slope factor → 1.45
➔ Type of the filter → CR-RC3
➔ EKV modelling of gm, γ and intrinsic capacitances of the transistors vs. the inversion order



Comparison for Iinput 550µA and Ifeed1µA:
Markers ➔ measurement
Lines ➔ calculation
Good agreement except for the parallel noise contribution:
➔ predicted value 400e- vs. 500e- measured

Noise performance of the active feedback

Components:

➔ Channel thermal noise

➔ Flicker noise (not filtered in ideal CR-RC filter - but thanks to AC coupling between stages)

Observation:

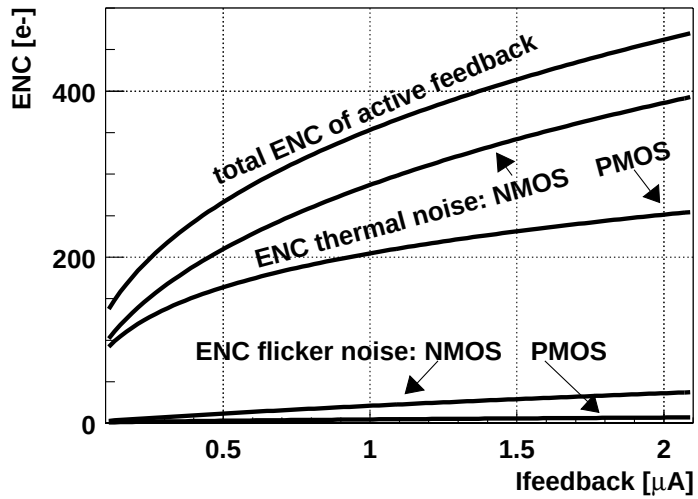
➔ ENC related to the active feedback almost twice higher comparing to classical passive feedback built with resistor of equivalent value

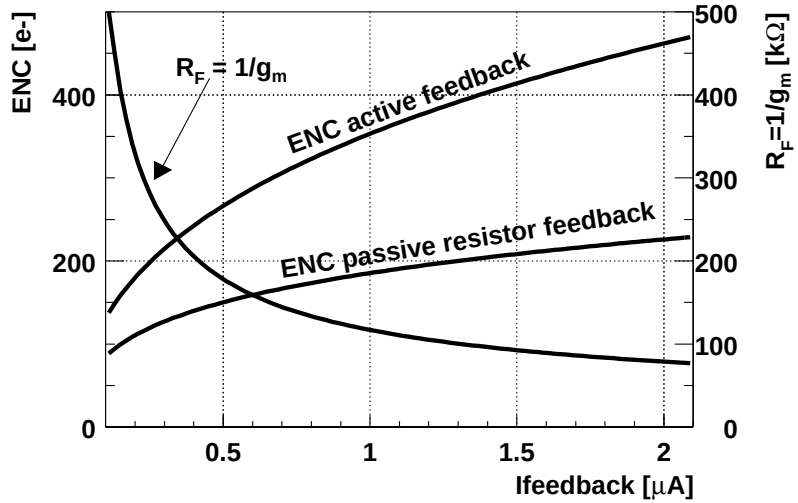
➔ still not a problem for capacitance detector above 10pF

Advantage of the active feedback:

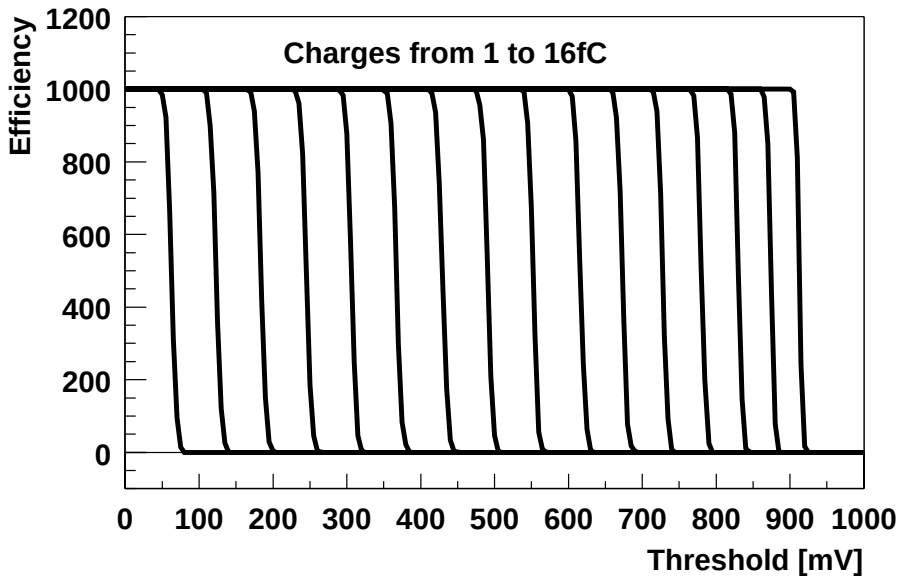
➔ Small feedback devices – higher bandwidth and preamplifier gain

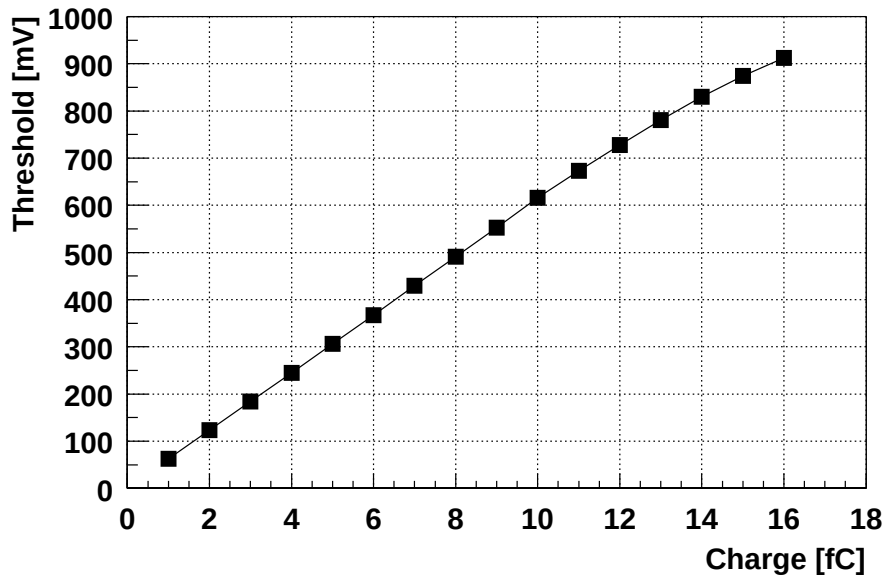
➔ Possibility of adjusting a phase margin and the Peaking Time





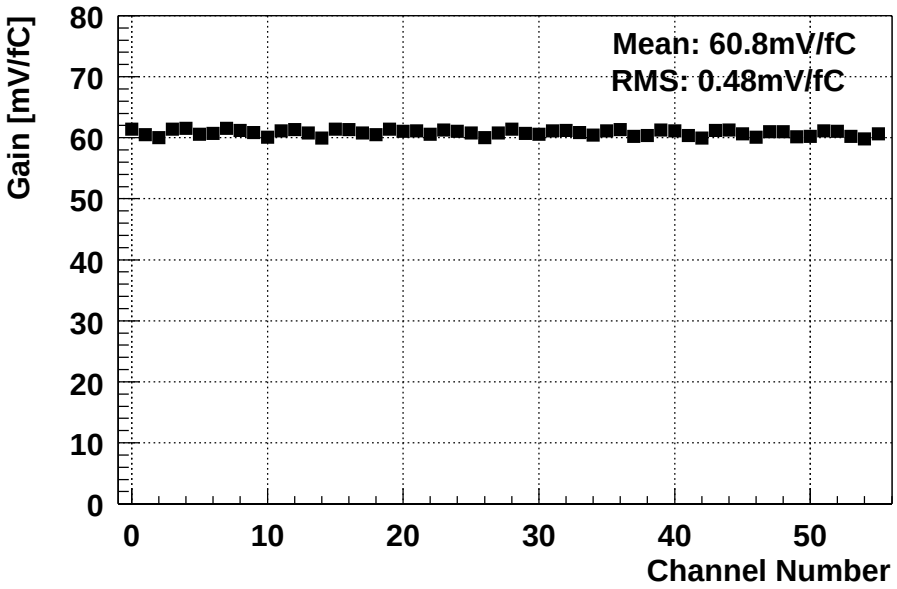
Full chain measurements

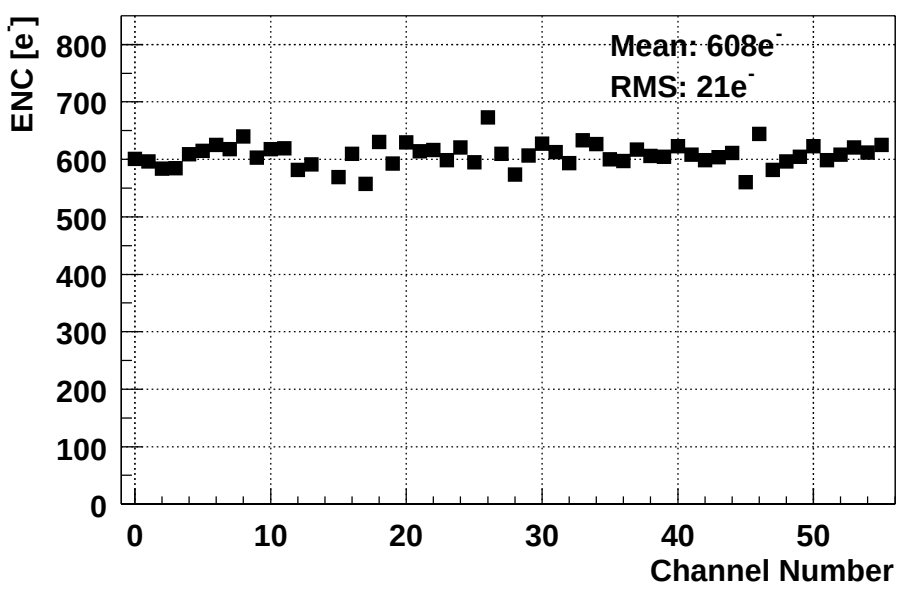




Threshold scans and response curve in one channel of the chip measured for Ipreamp=550μA and Ifeedback=1μA.

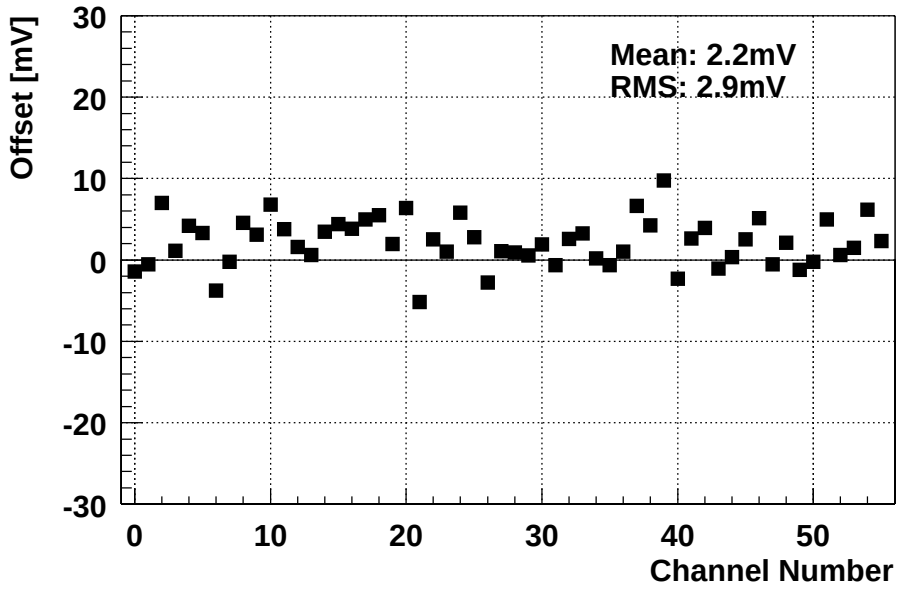
Full chain measurements – Gain and ENC

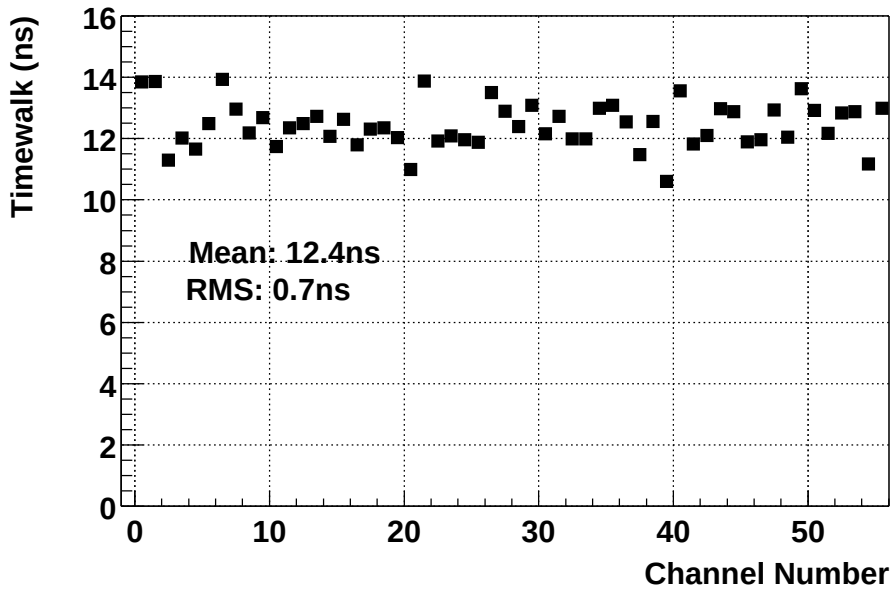




Distribution of channel gains and ENC in one chip (56 channels) measured for Ipreamp=550µA and Ifeedback=1µA.
Good agreement with analogue measuerements.

Full chain measurements – Offset and Time Walk



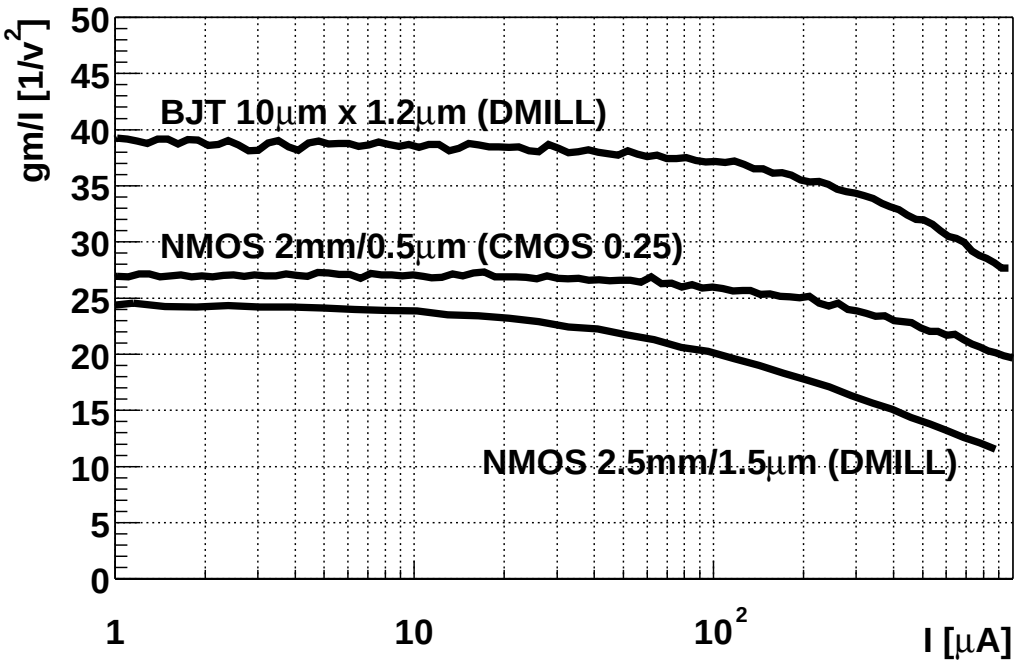


Distribution of comparator offsets (~3mV) and time walks (~12.5ns) in one chip (56 channels) measured for Ipreamp=550μA and Ifeedback=1μA.

Summary of results

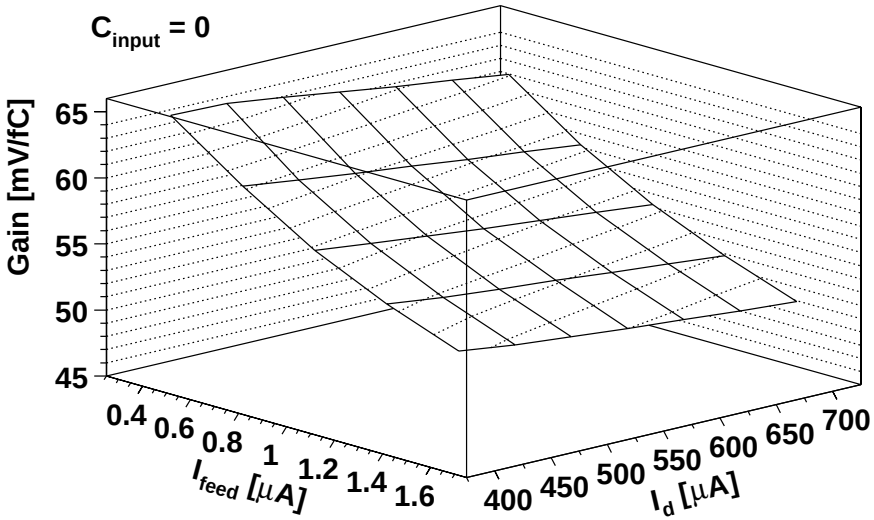
1. Functionality in wide range of biases (currents and power supply) and technology corner parameters (±3σ)
2. Gain ➔ ~55mV/fC ±5mV/fC (function of bias), good linearity up to 12fC signal (for all possible corner parameters and limited power supply)
3. Peaking time ➔ 20ns ±2ns (adjustable with feedback current)
4. ENC for Cinput 25pF ➔ 1400 –1600e- (function of bias)
5. Input resistance ➔ in the range of 100 Ohm at 10MHz
6. Very high uniformity of gain (0.8% RMS)
7. Small variation of offsets ➔ 3mV RMS (5% of 1fC) → no channels “outside distribution”
8. Small variation of ENC ➔ 3% RMS
9. Time walk of premp/shaper/comparator ➔ ~12.5ns (measured at 1fC threshold between 1.2 and 10fC signals)
10. Analogue power consumption at nominal biases (550µA input) ➔ 2.4mW/channel (0.95µA)
11. 10Mrad of X-Ray ➔ no visible effects

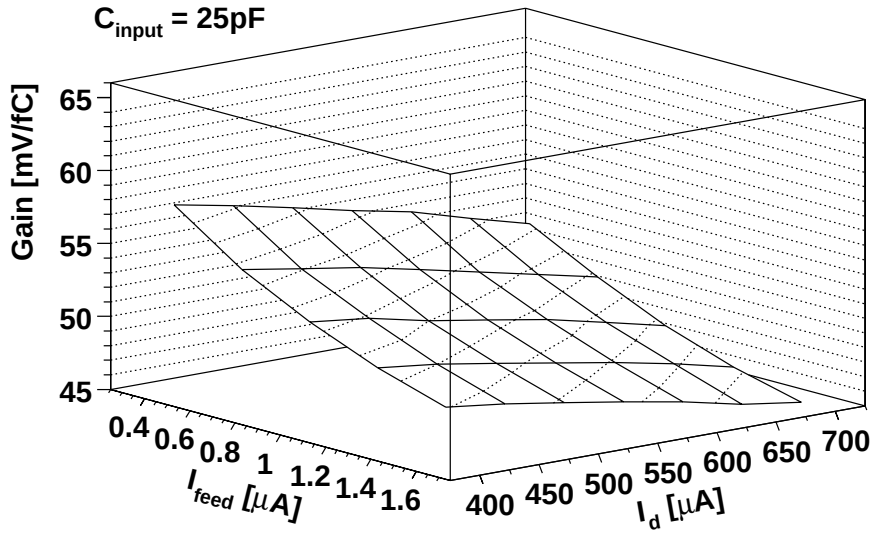
Addendum: Transconductance of BJT and NMOS transistors - remainder



Gm/I for MOS in weak inversion n-times lower than for BJT
n → slope factor → ~1.45 for IBM

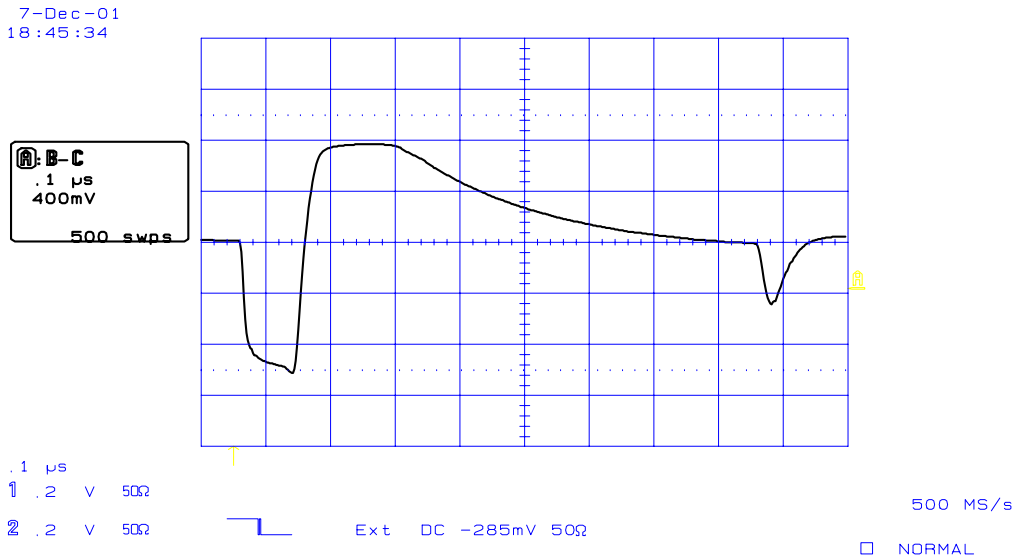
Addendum: Single analogue channel - Gain





Gain of the analogue channel as a function of feedback and input bias current.

Addendum: Response to overdrive



100fC and 10fC signal separated by 800ns distance seen at the input of the comparator.

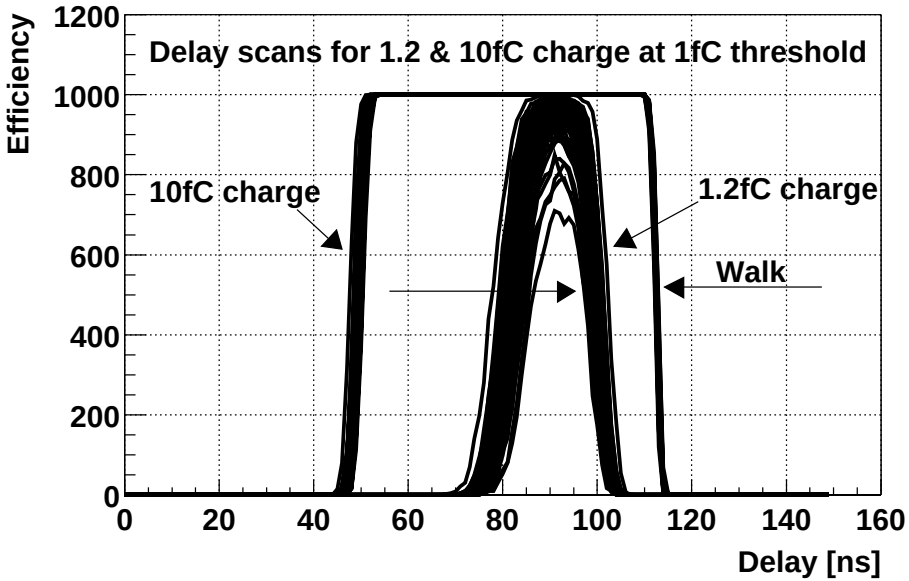
Addendum: Components contributing to final spread of the comparator offset

- Offset spread of the NMOS input pair amplified by the gain of stage (~2.5V/V)
- Offset spread of the transistors used in the threshold circuit, buffers and comparator stage
- Voltage mismatch due to resistor matching (RMS from foundry data → 0.5%)

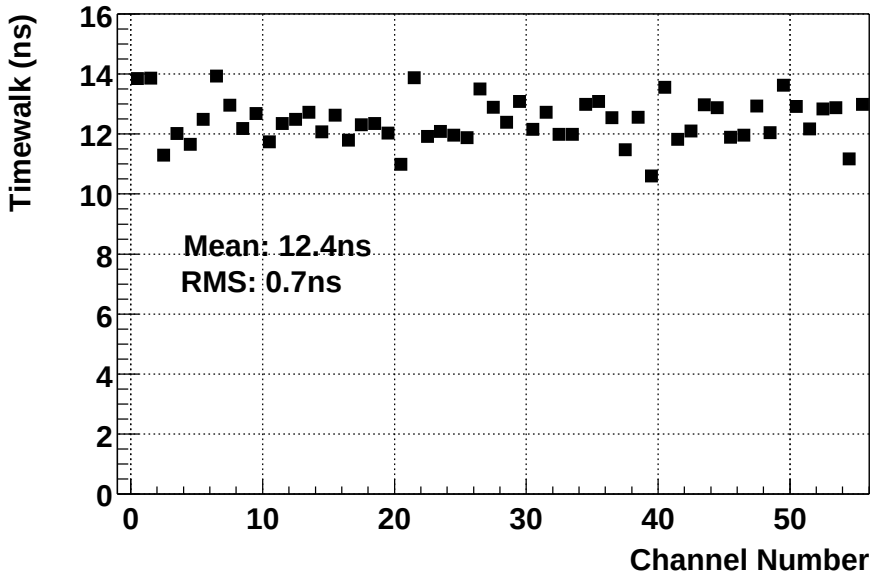
For 1 mV sigma offset of Vt for all transistor pairs and for nominal bias of
2 × 30 µA in the input stage:

$$\sigma_{Vt} = \sqrt{(1 \cdot 2.5)^2 + (1.4 \cdot 0.5e^{-2} \cdot 14.7e^{3} \cdot 30e^{-6} \cdot 1e^{3})^2 + 3 \cdot 1^2} = \sqrt{6.25 + 9.6 + 3} \cong 4.5mV$$

Addendum: Time Walk measurement



Time walk defined as the difference of comparator response delays for input charges of 1.2fC and 10fC at 1fC threshold.



Distribution of time walks (~12.5ns) in one chip (56 channels) measured for Ipreamp=550µA and Ifeedback=1µA.

Addendum:Current and power consumption

Current at nominal bias condition: (Iinput + 400uA) x 128
For Iinput = 550uA (10mS transconductance): 0.95mA/channel (2.4mW/channel)

For one 128 channel chip: 310mW (121mA)
For 12 chip module: 3.7W (1.45A)