Realization and Test of a 0.25μm Rad-Hard Chip for ALICE ITS Data Acquisition Chain

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Abstract

CARLOS 2.0 is a second version of a chip that is part of the data acquisition chain for the ALICE ITS experiment. The first version of the chip has been implemented on Alcatel 0.35μm CMOS digital technology and included 8 8-bit channels. Conversely this second version deals just with two 8-bit channels to increase fault-tolerance during future tests and actual data acquisition. Moreover this version has been implemented using the CERN developed digital library of enclosed gate transistors. This is a rad-hard library developed within RD49 project. The prototype works well and it is going to be applied for ALICE ITS 2002 test beams.

I. INTRODUCTION

The paper explains the design and the realization of a small size digital Rad-Hard chip submitted at CERN multi-project run Multi-Project-Wafer-6 in November 2001. The design is a part of the Large Hadron Collider (LHC) A Large Ion Collider Experiment (ALICE) experiment [1], [2] at CERN and, particularly, is a device oriented to a electronic front-end board for the Inner Tracking System (ITS) data acquisition. The chip has been designed in VHDL language and implemented in 0.25μm CMOS 3-metal Rad-Hard CERN v1.0.2 digital library. It is composed of 10k gates, 84 I/O pads out of the 100 total pads, it is clocked at 40MHz, it is pad-limited and the whole die area is 4x4 mm^2.

II. TECHNOLOGICAL CHOICE

The effects of radiations on electronics circuits can be divided in total dose effects and single event effects [3], [4]. Total dose modifies the thresholds of MOS transistors and increases leakage currents while single event effects can trigger latch-up phenomena or can change the value of digital bits. Single event upset can be a problem especially when occurring in the digital control logic and can be prevented by layout techniques or by redundancy in the system. On the other hand radiation tolerant layouts have area penalties. It can be estimated that in a given technology a minimum size inverter with radiation tolerant layout is 70% bigger than the corresponding inverter with standard layout. The radiation dose which will be received in ALICE by the readout electronics will be quite low, below 100 Krad in 10 years. This value is probably below the limit of what a standard technology can afford; however conservative considerations suggest the use of radiation tolerant techniques for critical parts of the circuit. These techniques have been proven to work up to 30 MRad and allow a lower area penalty and lower cost compared with the radiation hard processes. This is why the library chosen for the implementation of the design presented in the papers is the 0.25 μm technology with standard cells designed at CERN to be radiation tolerant. The prototype is named CARLOS 2.0 since it is a second version of a first chip designed in standard 0.35 μm CMOS Alcatel technology [5].

III. READOUT ARCHITECTURE

The system requirements for the Silicon Drift Detector (SDD) readout system derive from both the features of the detector and the ALICE experiment in general. The amount of data generated by the SDD is very large: each half detector has 256 anodes and for each anode 256 time samples have to be taken in order to cover the full drift length. The data outgoing from two half detectors are read by one 2-channel CARLOS 2.0 chip. The electronics is inserted on a board in a radiation environment. The whole acquisition system electronics performs analog data acquisition, A/D conversion, buffering, data compression and interfacing to the ALICE data acquisition system. The data compression and interfacing task is carried out by CARLOS 2.0 chip. Each chip reads two 8-bit input data, is synchronized with an external trigger device and writes a 16-bit output word at 40MHz. Indeed, CARLOS 2.0 mainly contains a simple encoding for each channel and the data are packed into a 15-bit barrel-shifter. Then a further bit is added to indicate if the data are dummy or actual: this leads to a 16-bit output data. After this electronics the data are serialised and transmitted by means of an optical link at 800Mbit/s [6]. CARLOS 2.0 will then be used to acquire data in the test beams and will allow us to build and test the foreseen readout architecture.

IV. CARLOS 2.0

Figure 1 shows CARLOS 2.0 divided into the main blocks. Two identical channels are hosted on the chip each of which is the unit for encoding, packing and storing data. Each channel is composed of the encoder, the barrel and the fifo32x15. The encoder block encodes 8-bit input data in variable length codes from 4 to 10 bits long in a completely loss-less way. This encoding scheme provides a compression on input data based on the knowledge of the statistics of the stream. Locally in time this compressor may even provide an expansion of data that have to be temporarily stored in a FIFO buffer. The barrel is the block packing the 4 to 10 bits variable length codes coming from the encoder block to a fixed length 15-bit word. It makes use of two internal 15-bit registers, and is able to break an input data in two pieces without losing any information: when the first word is put in output the second word is used to store the input data. The barrel latency is 2 clock periods. When the input is the last data belonging to the current event, the current value in the barrel is put in output even if it is not completely full and the not defined bits are put to 0. The fifo32x15 block has the purpose of storing

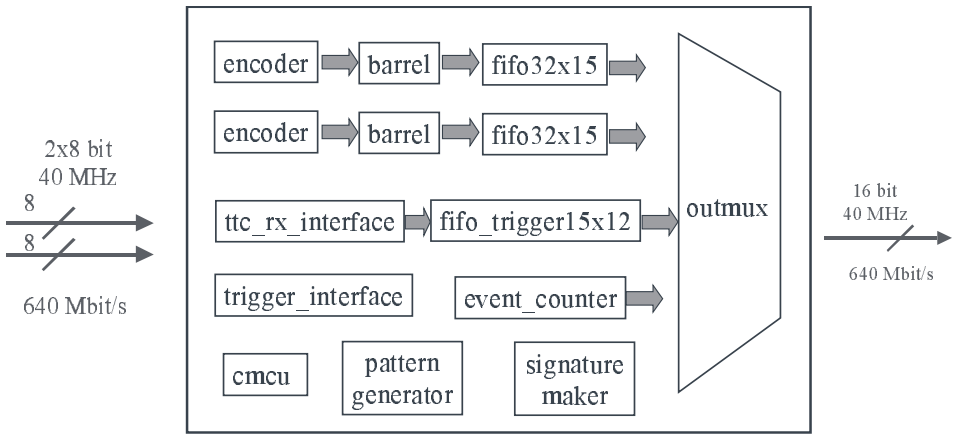

Figure 1: CARLOS 2.0 design blocks

information coming out from the barrel shifter. The output data is fairly allocated 50% of the time to both channels (one clock period each) and since the encoding algorithm can locally, in time, behave as an expansor, data have to be stored before multiplexing. The fifo32x15 is a synchronous flip-flop based FIFO. The ttc-rx-interface block receives trigger information from an external trigger device while the fifo-trigger15x12 block is logically equivalent to the fifo32x15 block except for what concerns dimensions: its size is 15x12 words. This is necessary for storing bunch counter and event counter information concerning 5 consecutive accepted events. When CARLOS 2.0 is ready to send a data packet in output, the first 3 trigger words are read and sent to the outmux block. The event-counter block is a counter triggered by outmux block when an event has been completely transmitted and a new one can be accepted. This count number is used both in the header and in the footer words for a safer transmission protocol. The outmux block is a multiplexing unit for sending alternately in output data coming from the two channels. As soon as data fill the two FIFO blocks the outmux block begins to put in output a packet. The first 3 16-bit words contain event information. Headers are followed by an even number of data words: if a channel has not valid data to send, the MSB is put to 1 and all the other bits are set to 0. The data packet is then concluded with the transmission of two footer words. The trigger-interface block is an interface with an external trigger chip. The Command Mode Control Unit (cmcu) is an internal control unit remotely controlled via the JTAG port. At power-on CARLOS 2.0 is put in an IDLE state in which no calculation is performed. Then it can be put in a RESET-PIPELINE state in which an internal reset signal is asserted and all registers are initialised. The following state is the BIST (Built In Self Test) state in which CARLOS 2.0 runs an internal test. The pattern-generator block is part of the BIST utility implemented on CARLOS 2.0. The BIST [7], [8] provides a set of 200 pseudo-random test vectors at the same time to both processing channels. The signature-maker block performs the signature analysis. In signature analysis, the test responses of a system are compacted into a signature using a linear feedback shift register (LFSR). Then the signature of the device under test is compared with the expected signature. If they both match, the device is declared fault free, otherwise it is declared faulty. Since several thousands of test responses are compacted into a few bits of signature by a LFSR, there is an information loss. As a result some faulty devices may have the same correct signature. The signature register implemented on CARLOS 2.0 is 16 bits wide, so the probability of aliasing is 2^{-16}.

Figure 2 shows a picture of the final layout of CARLOS 2.0 as it has been sent to the foundry. It is a 4x4mm square pad-limited chip with 100 pads, it contains 10 Kgates and is packaged on a PGA100.

V. DESIGN FLOW FOR CERN DESIGN KIT

The digital design flow is normally very easy and straightforward. Conversely, in this case, the task has not been obvious since the design kit has been provided with Verilog models for the cells. Here is presented, step by step, what it has been done for going ahead with the back-end design. Since there was a previously designed VHDL code, it was required a VHDL-to-Verilog conversion to simulate the netlist with the timing characterization. Figure 3 shows the main steps that have been carried out to convert, simulate and

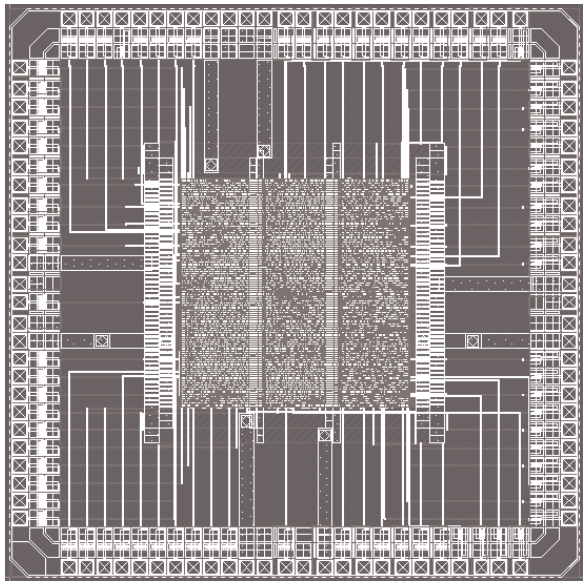

Figure 2: CARLOS 2.0 layout

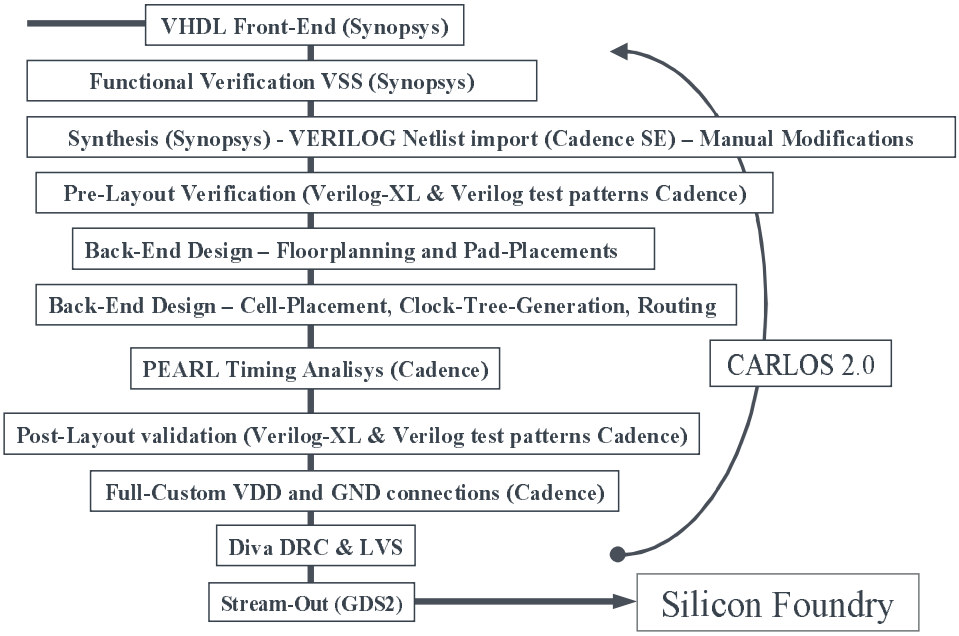

Figure 3: CARLOS 2.0 design flow

realize a digital ASIC with the CERN 0.25 μm CMOS rad-hard technology starting from a VHDL code/netlist. After having performed a functional verification, for example by means of Synopsys VSS simulator, the design is synthesized by Synopsys. Then the netlist is saved in a Verilog format for making it compatible with Cadence Silicon Ensemble place and route tool. At this stage even some manual modifications can be done like, for example, buffer insertions. The design can be imported in Cadence for a simulation of the synthesized verilog netlist by means of VerilogXL tool but this is just a pre-layout verification. After that the back-end design begins. First it includes the pad placement and the global floorplanning. Then follow the cell placement, the clock tree generation by means of the Cadence CTGEN tool and the routing. At this point a (PEARL) static timing analysis is executed before going to the post-layout simulation. This step requires both Standard Delay Format (SDF) file to include parasitic capacitors and a new extracted Verilog netlist which includes the added clock tree. At this point the netlist is different from the previously imported one. Thus, this new netlist, together with the parasitics, can be simulated by means of the same stimuli used during the pre-layout simulation. Finally a power supply connection is to be made manually and the design is ready to be analysed by DRC and LVS tools. It should be noted that the LVS tool does not compare the initial VHDL design since it has been modified by the clock tree generator tool.

VI. CARLOS 2.0 TESTS

The CARLOS 2.0 tests have been designed before by means of a PCB dedicated to test purposes only. The PCB together with the testing instruments are shown in Figure 4. So a two-layers PCB has been designed to provide I/O signals by means of strip-line connectors and by inserting the PGA100 packaged chip on a ZIF socket. These chips derive from different silicon wafers and have been randomly selected. The chips have been stressed up to 80 MHz while for higher clock frequencies they begin to fail. In addition, even though the CARLOS 2.0 layout has been done with separated core and periphery power supply pads, the test have been executed with 2.5V for both powers. Moreover, at required 40MHz clock frequency the chips work with an average power consumption of 75mW.

The very first test performed on CARLOS 2.0 has been to stimulate it with the same test vectors used for the post-layout simulation. The pattern generator provided a 4 k-word testbench containing the JTAG configuration and two 1-kword events. Then data obtained using the logic analyzer have been processed using the C program written with the purpose to reconstruct the inputs values starting from actual CARLOS 2.0 outputs: in other words the C program performs the inverse function than the one performed by the CARLOS chip. As a second step the C program compares actual input values to reconstructed inputs and draws a list of errors in case there is a mismatch between the two data sets. This software tool automated the job of checking if the results of CARLOS 2.0 are good or not.

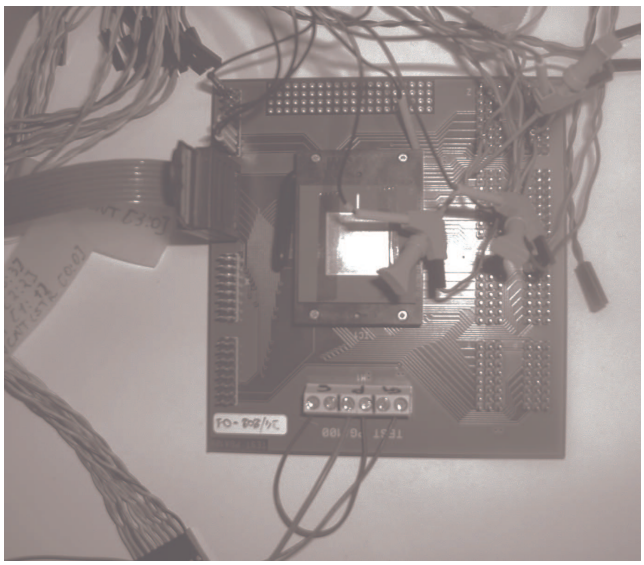

Figure 4: CARLOS 2.0 chip under test

Running the 4 k-word testbench on the 20 packaged chips the following results have been obtained:

- 11 chips are perfectly working;
- 8 chips do not work at all (they drop 30 mA even when not clocked);
- 1 chip contains only one of the two processing channels perfectly working, while the other gives bad results.

The second test on the 20 chips concerned the BIST, that is run and controlled using the JTAG port. The BIST on CARLOS 2.0 has been designed to show the result of the test on the output pin *tdo* with the code FF when successful and 55 when the test fails. 11 chips out of 20 passed the BIST, while 9 exited with the 55 code. This test proves that the BIST gives the same results as the more complete test did before. Even if 20 chips do not allow to get statistical results, the BIST might be chosen as a very simple and reliable test in order to select working from failing chips, before any other test. Other testbenches have been used to stimulate CARLOS 2.0 are 48k-word events with random generated values, with gaussian generated values and with data coming from test beam. Repetitive tests have also been run on the 11 selected chips with good results.

VII. DAQ BOARD

As a first prototype, in order to acquire data coming out from CARLOS 2.0 using the Data Detector Link (DDL), it has been designed a receiver test board (CARLOS-rx) with the purpose of connecting it directly to CARLOS 2.0 on one side and to the Source Interface Unit (SIU) or its simulator card (SIMU) on the other side. CARLOS_rx, as shown in Figure 5, is a 4-layer board containing the Xilinx FPGA XC3195A-09, some stripe connectors on the left side in order to acquire data from CARLOS 2.0 outputs, 4 bus transceivers with 3-state outputs and an 80-pin high density connector on the right for the connection to the SIMU [9] or the SIU itself [10]. The SIMU is a tool designed by the CERN/DAQ group to ease the integration of the ALICE Front-End Electronics (FEE) with the DDL. Its interface connector towards CARLOS_rx is equal to the one hosted on the SIU, so that the two boards are completely interchangeable.

The prototype chain with the SIMU board has been successfully tested in Bologna for what concerns the opening of a transaction and the transfer to the SIMU of the same 1k-word events used for the test of CARLOS 2.0 itself. Then it has been substituted the SIMU board with the complete DDL chain (see Figure 6). This test has been carried out at CERN by connecting a pattern generator to the inputs of the present processing chain: the CARLOS chip, the CARLOS_rx board, the SIU, the optical fibre, the Desitination Interface Unit (DIU) and PC acquisition board (pRORC). After opening a transaction via software on the Linux PC hosting the pRORC, the pattern generator begins to send data to the chain and, after processing, the data have been collected on the PC. In the test run, 83k events have been acquired using the DDL on PC. Collected data, then, have been compared to expected data giving evidence of no error at all on the complete data acquisition chain. This test shows that CARLOS 2.0 outputs can easily be acquired using a simple FPGA-based board and the DDL.

VIII. CONCLUSION

The chip has been implemented using CERN library 0.25 μm CMOS technology employing radiation tolerant layout. CARLOS 2.0 is our prototype tailored to fit in the ALICE ITS readout architecture. Taking into account that the CERN 0.25 μm library contains a small number of standard cells and they are not so well characterized as commercial ones, it has been decided to try and test first the new design flow and the new technology. The chip has been sent to the foundry in November 2001 and have been tested starting from February 2002. A specific PCB has been designed for the test task; it contains the connectors for probing the ASIC with a pattern generator and a logic state analyser. The chip is inserted on the PCB using a ZIF socket. This allows us to test the 20 packaged samples out of the total amount of bare chips we have from the foundry. The test phase has shown that 12 out of 20 chips under test work well. Nevertheless it is planned to redesign a new version of the chip by adding extra features. This will not substantially increase the chip area since it is pad-limited and should be close to the final version of the chip for the ALICE ITS experiment.

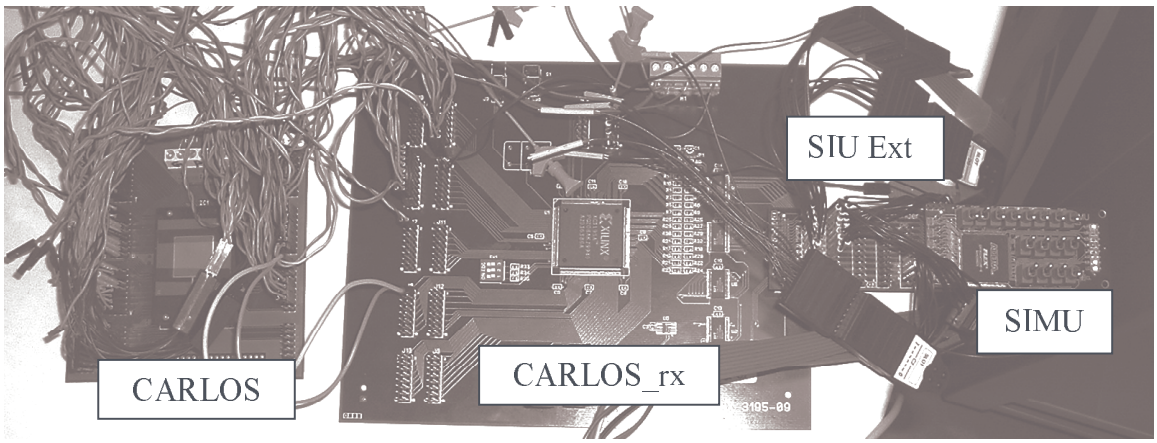

Figure 5: Test of the chain CARLOS, CARLOS-rx, SIU Ext and SIMU board in Bologna

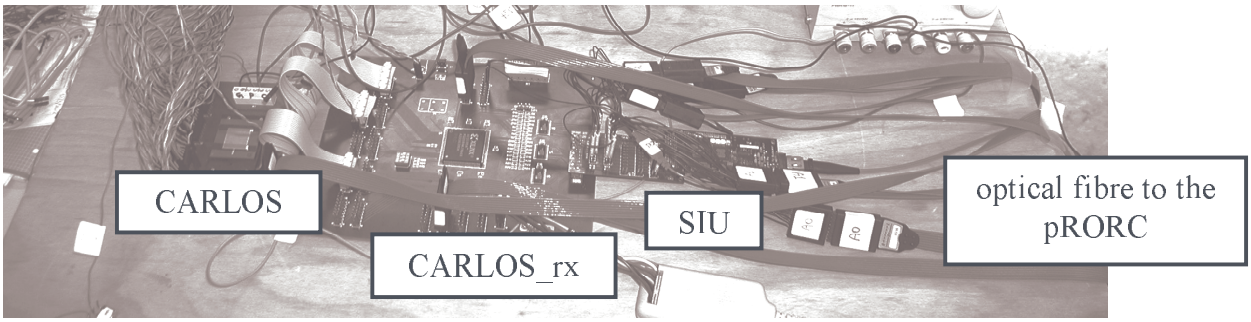

Figure 6: Testing the chain CARLOS, CARLOS_rx, SIU, DIU and pRORC at CERN

IX. ACKNOWLEDGEMENTS

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X. REFERENCES

[1] ALICE Collaboration, "Technical Proposal for A Large Ion Collider Experiment at the CERN LHC", December 1995, CERN/LHCC/95-71.

[2] CERN/LHCC 99-12 ALICE TDR 4, 18 June 1999.

[3] E. Crescio, D. Nouais, P. Cerello, "A detailed study of charge diffusion and its effect on spatial resolution in Silicon Drift Detectors", September 2001, ALICE-INT-2001-09.

[4] F. Faccio, K. Kloukinas, G. Magazzu, A. Marchioro, "SEU effects in registers and in a Dual-Ported Static RAM designed in a 0.25 µm CMOS technology for applications in the LHC", Fifth Workshop on Electronics for LHC Experiments, September 20-24, 1999, pages 571-575.

[5] G. Mazza, et al.," Test results of the ALICE electronic readout prototypes" LEB 2000, 6th Workshop on Electronics for LHC Experiments, Cracow PL, 11-15 Sep. 2000, (CERN-ALI-00-09)

[6] A. Marchioro et al., "A Radiation Tolerant Gigabit Serializer for LHC Data Transmission", 7th Workshop on Electronics for LHC Experiments, Stockholm, Sweden, 10-14 September 2001

[7] F. Wang, "BIST using pseudorandom test vectors and signature analysis", IEEE 1988 Custom Integrated Circuits Conference, CH2584-1/88/0000-0095.

[8] T.W. Williams, W. Daehn, "Aliasing errors in multiple input signature analysis registers", 1989 IEEE, CH2696-3/89/0000/0338.

[9] AID group, "ALICE Detector Data Link - Users' Guide for the SIU Simulator", CERN internal note, ALICE-INT-1999-03, Edms id. 106742

[10] Gyorgy Rubin, Csaba Soos, "ALICE DDL - Hardware Guide for the front-end Designers", CERN internal note, ALICE-INT-1998-21, Edms id. 112129