# Complementary bipolar application specific analog semicustom array, intended to implement front-end units.

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*Abstract*

The structure of an analog semicustom array, intended to implement front-end electronics ICs on its basis, is considered. The features of this array are: implementation with an inexpensive bipolar process despite containing an equal number of NPN and PNP structures with well matched characteristics, supply voltages from 1.5V to 15V, transistor current gains Bst~100 and unity gain frequencies Ft > 3 GHz at collector currents of (100…300) μA, high- and low-ohmic resistors, MOS capacitors, minimum two variable plating levels available.

Specific circuit diagrams and parameters of the front-end electronics ICs, created on the basis of the considered array, are presented. The results of their tests are given.

## I. INTRODUCTION

During the last few years the author team of the paper has been designing front-end ICs both as application specific ones (in the case of large batches and relatively long terms of manufacture) and as ones, based on preliminary elaborated analog semicustom arrays (in the opposite case). Implementation in both cases was by bipolar process. Some of these ICs and printed boards, based on the latter, were presented at previous workshops on LHC electronics [1,2].

These arrays are application specific in the sense of taking into account the standard structure of the analog channel, processing preliminary the signals of ionising radiation detectors, and may be therefore regarded, as application specific analog semicustom arrays.

The present paper is aimed at describing our new development – the complementary array. It is destined to serve, as a convenient semifinished item, for solving tasks with a moderate number of channels in physical experiments (hundreds -- thousands). That is especially useful at the prototype stage.

## II. FEATURES OF THE ARRAY

The given array was developed with consideration of the demands of multichannel physical experiments on testing a range of prototype solutions under the conditions of financial and temporal stringencies. The following peculiarities of the array came out as result of that consideration:

- implementation with an inexpensive bipolar process (cost comparable with CMOS);
- contents of an equal number of vertical drift NPN and PNP structures with well matched characteristics;
- contents of high- and low-ohmic resistors, MOS capacitors;
- the range of supply voltages from 1.5V to 15V;
- two variable plating levels available;
- its structure (mutual disposition of elements) is optimised for plating the multichannel ICs of the type of amplifier-shaper-discriminator.

Traditionally the bipolar complementary ICs were created on the basis of combining vertical NPN transistors with PNP ones, having either a lateral, or vertical structure with a uniformly doped base, implemented in an N-type epitaxial film. The feature of the elaborated design and processing solution consists in using vertical transistors of both NPN and PNP types with non-uniformly doped bases. That allows to achieve a better matching of complementary transistors, concerning both their static and dynamic parameters. The vertical structure of PNP transistors was implemented by employing a sequence of processing stages, being close to the NPN transistor's creation route and based on P-wells with a $P^+$ buried layer and a $P^+$ contact with the buried layer, intended to reduce the collector bulk resistance.

## III. STRUCTURE OF THE ARRAY

The layout of the array (dimensions 2.4*2.1 $mm^2$) is shown in fig. 1.

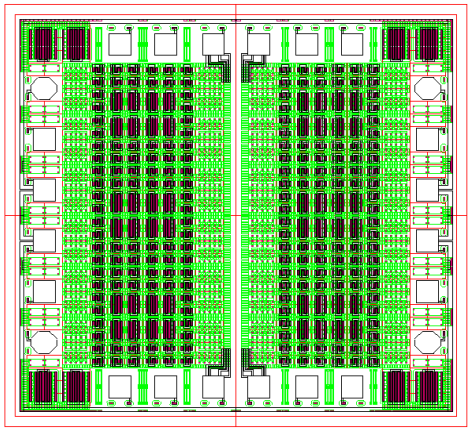

Figure 1: Layout of the complementary array

It has a quadrant symmetry, where each quadrant contains 3 identical cells, shown in fig.2.

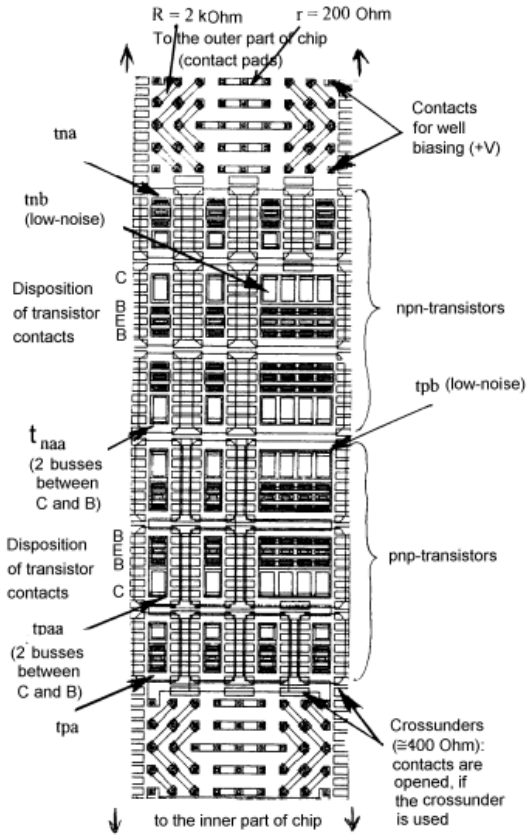


Figure 2: The structure of the analog cell

Each cell contains 20 bipolar transistors (NPN and PNP equally) of two layout varieties. Besides that, each quadrant of chip contains a complementary pair of enlarged transistors. Also each cell contains a set of diffusion resistors and on the peripheral -- four MOS capacitors of 2 pF. The total resistance of the resistors in the active base layer exceeds 1 MOhm, while the one of passive base layer is about 36 kOhm.

Simplified cross-sections of the main standard transistors are shown in the following fig. 3-4., and their basic parameters are presented in table 1.

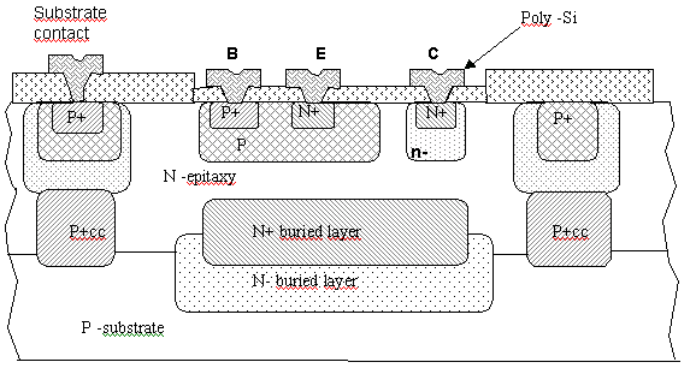


Figure 3: Cross-section of npn transistor

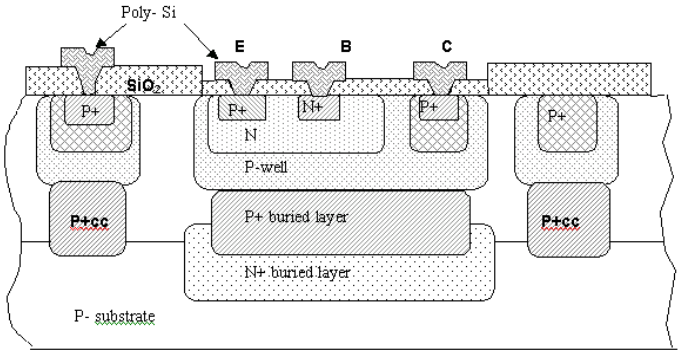


Figure 4: Cross-section of pnp transistor

The transistor design in plan together with the regions for bias routing and crossunders allowed to increase the potential utilization capability of the chip up to 75..90% of total area.

The employed set of resistors allows to implement a practically continuous range of resistors by virtue of their series and shunt connections. The resistances of the basic resistive units were thereat chosen as 200 Ohm and 2 kOhm.

## IV. PLATINGS AND THEIR CHARACTERISTICS

By the time on the basis of the given semicustom array there have been developed and manufactured several analog ICs. Among them are the following:

- transimpeadance preamplifier (gain 50 mV/uA, bandwidth 15 MHz, power consumption 200 mW). That same circuit was tested in the mode of a charge-sensitive amplifier and exhibited a conversion factor of 0.2 V/pCb;

Table 1: Characteristics of the basic types of transistors (tna and tpa)

| Name of characteristic | npn-transistor, type tna | pnp- transistor, type tpa |
|---|---|---|
| Base current gain βN at the collector current Ic≅5 mA, not less then | 120 | 100 |
| Early voltage VA, not less then | 100 V | 80 V |
| Capacitance of base-emitter junction Cbe at Vbe=0, within | 150 fF | 150 fF |
| Capacitance of base-collector junction Cbc at Vbc=0, within | 170 fF | 250 fF |
| Capacitance of collector with substrate Ccs at Vcs=0, within | 450 fF | 550 fF |
| Bulk resistance of base rb , within | 110 Ohm | 160 Ohm |
| Bulk resistance of collector rc , within | 100 Ohm | 120 Ohm |

- high-speed comparator (gain 500, absolute propagation delay < 5 ns, propagation delay variation < 400 ps at dynamic range of 100, offset voltage < 2 mV, input current < 10uA, programmable output logic);
- pulse stretcher of short current signals (pulse durations up to 100ps), including an amplifier (gain factor, controlled in the range from 5 to 10, rise and delay times equalling 3.5ns and 2.2ns correspondingly at an overshoot in transient less than 5%) and a circuit, resetting the charge in the accumulation capacitance (allows to discharge the accumulation capacitance from the level of 1V to the one of 20mV during 1.5ns).

Besides, a number of test platings have been made for the extraction of both static and dynamic SPICE parameters of array elements themselves [3, 4]. Along with solitary elements some special multitransistor test circuits and functional modules are used for solving this problem:

- Operational amplifiers with current and voltage feedbacks;
- Temperature sensors (two versions);
- Wide application differential complementary stages;
- Circuits for determination of transistor base resistance (RB);
- of the parameters TF/CJE of transistors;
- Circuits for determination of the spread of base-emitter voltages ($\Delta U_{BE}$) of transistors;
- Circuits for determination of interelectrode capacitances (CJE, CJC) and collector-substrate capacitance (CJS) of transistors.

The characteristics of these circuits and modules essentially depend on one or more SPICE parameters. The simplest example is the integrator, where the time-defining capacitor is formed by a parallel connection of interelectrode capacitances of several single-type transistors. Such an approach allows to decrease the frequencies, whereat the measurements are carried out, and, accordingly, exclude the influence of stray elements, what is especially important for the extractions of dynamic SPICE parameters. In some cases the averagement of the SPICE parameter, being determined, is simultaneously achieved.

## V. Conclusion

The chip under consideration is a predecessor of the currently developed chip with a greater number of elements and a structure, oriented toward the creation of (8…16)-channel front-end ICs.

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