Design, Prototyping and Testing of the Detector Control System for the ATLAS Endcap Muon Trigger

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Abstract

The TGC detector will be inaccessible during operation due to high radiation levels in the ATLAS cavern. The detector requires a Detector Control System (DCS) to monitor important detector and environmental parameters, calibrate, set and maintain the configuration of FE electronics, and take appropriate corrective action to maintain detector stability and reliable performance.

The TGC DCS system makes full utilization of the intelligence offered by the ATLAS ELMB CAN nodes in order to distribute the control of complex tasks on the front-end nodes. Our hardware and software design, integration and radiation test results are described.

I. INTRODUCTION

The TGC detector will be inaccessible during operation due to high radiation levels in the ATLAS cavern. The detector requires a Detector Control System (DCS) [1] to monitor important detector and environmental parameters, calibrate, set and maintain the configuration of FE electronics, and take appropriate corrective action to maintain detector stability and reliable performance.

The status of all components should be available and user intervention should be possible when/where allowed. The TGC DCS will accept supervisory commands and return the summary status of the TGC subsystem. Additionally the DCS will supply a user interface to allow autonomous operation of the TGC during the construction, testing, commissioning and calibration of the TGC detector.

The TGC DCS will comprise of a central control and configuration PC master, about 1500 micro controller slaves controlling hardware devices such as displacement sensors, temperature sensors, gas pressure and flow, high and low voltage supplies, and data acquisition parameters. The hardware is subject to harsh radiation conditions, posing a challenge to software and hardware design, implementation and testing.

The user interface requires many layers ranging from access by non-expert shift operators, to expert system managers and to developers of particular sub-systems. The hardware effort includes integration of the different sensors in the TGC electronics and design of some special measurement circuits for monitoring purposes. The software effort spans several operating environments: controller PCs, micro controller boards, hardware configuration protocols, etc.

The system we propose is novel in its approach. It places a significant part of the system intelligence in microprocessors right on the detector. This reduces the bandwidth required to transmit data and commands and enables to perform complex tasks with the reliable but slow CAN bus system.

The CAN nodes will configure on-chamber ICs in situ using the JTAG protocol and run autonomous tests on the ICs to ensure their continued reliable functioning. They will also reconfigure or perform tests by instructions from the supervisory control system which is the top of the CAN bus network.

In addition the CAN nodes will also measure and set voltages in the traditional way through DACs and ADCs. The on-chamber DCS includes an autonomous charge measurement circuit which is operated by the CAN node.

A prototype of a fully functional vertical slice of the DCS was tested successfully in integration tests of the TGC electronics at KEK in November 2001. Subsequently we performed radiation tests of the DCS on chamber components, and participated in an integration test at CERN. The system design and test results are described here.

II. System hierarchy and topology

There will be at least one DCS Local Control Station (LCS) per TGC side. The LCS will be located in USA15 near the RODs. Each LCS will have several CAN bus ports and each port drives an independent CAN network. The LCS communicates with the RODs in its partition via the local area network in USA15. The RODs send and receive messages via the LCS. The LCS also controls the HV, gas and LV systems.
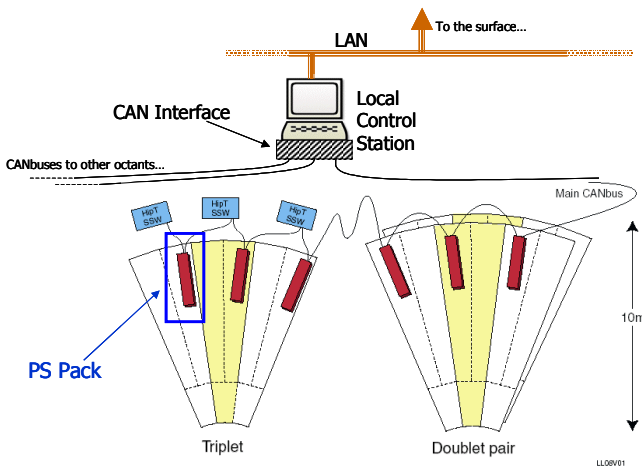

Figure 1: CAN bus layout for doublet pairs and triplets, including the three Hip$_T$/Star Switch crates, for one of 16 octants. Each octant is served by an independent CAN bus controlled by a CAN interface port in the LCS.

There are about 25000 on-chamber DCS channels (not including JTAG configuration), e.g. 353 channels per doublet PSpack [2], distributed over the 3 to 5 meter length of the PSpack. CAN nodes are distributed on the PS boards to service many channels close to their source. The CAN microprocessor has a multiplexed ADC, parallel and serial digital I/O, and a robust differential board-to-board bus, the CAN bus, all on one inexpensive chip. Data can then be transmitted via the CAN bus, implemented as a single cable in the PSpack instead of dedicated lines per channel.

DCS partition boundaries must fall on the DAQ and trigger partition boundaries. This allows a failing section of the detector to be put offline with minimal impact on working sections. The CAN bus cabling must take into account the chamber assembly onto the big wheels.

The above considerations lead us to the following partitioning of the TGC CAN system: A single main CAN bus will service a combined octant of doublet pairs and triplets, plus the octant's three HipT/Star Switch crates, as shown in Figure 1. The Inner TGC station will be serviced by one CAN bus per side. The total number of buses is therefore 9 main

CAN buses per TGC side. Each PSpack will have a "local" CAN bus connected to the main CAN bus of the octant via a repeater and opto-isolator [3]. Since there are three sets per octant, with 17 PS boards per doublet-pair set and 10 PS boards per triplet set, the CAN bus serving an octant has 81 Patch Panel nodes. Additional nodes, three in the Hip$_T$/Star Switch crates and six on the three service Patch Panels make a total of 90 nodes per octant.

Each main bus with its local CAN buses is an independent CAN network. Only the six Service Patch Panel CAN nodes with their transceivers plus the six repeaters and the three crate CAN nodes will be powered from the main CAN bus. The rest are powered locally.

Figure 2 shows the PSpack's local CAN bus and its connection to the main CAN bus. Each main bus will connect on a Service Patch Panel to one CAN node and a "Y"-repeater, which will connect it to the local CAN bus. This repeater opto-isolates the local CAN bus from the main CAN bus in order to comply with the ATLAS grounding rules. It breaks the CAN bus into separate electrical segments with 17 (Doublet PSpack) and 10 (Triplet PSpack) nodes per segment. Each segment appears as a single load on the main CAN bus. The power for the CAN nodes and their transceivers on the local CAN bus will be provided through their host Patch
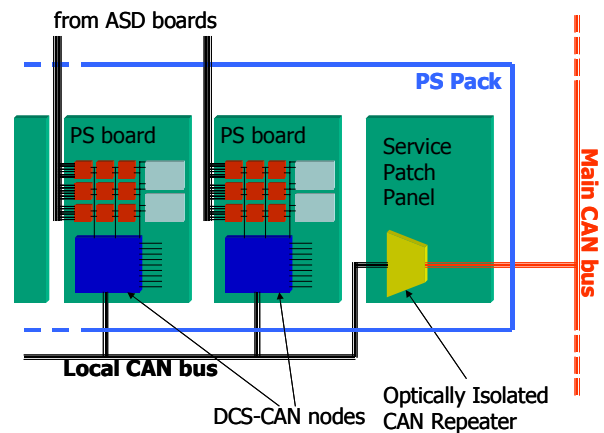

Figure 2: CAN on the PSpack

Panel. The local CAN bus will run along the PS Pack using twisted pair flat cable which will connect to the DCS-PS board.

The CAN node will be the standard ATLAS ELMB [4]. This is a small daughter-board that plugs into the DCS-PS board which in turn plugs into the PS board (or VME carrier board). Since the ELMB does not contain all the functions needed, the extra functions will be placed on the DCS-PS board. The patch panel CAN node must handle up to 16 ADC channels, 8 DAC channels, an I2C interface and two JTAG chains. Figure 3 shows a block diagram of the services the DCS-PS node provides.
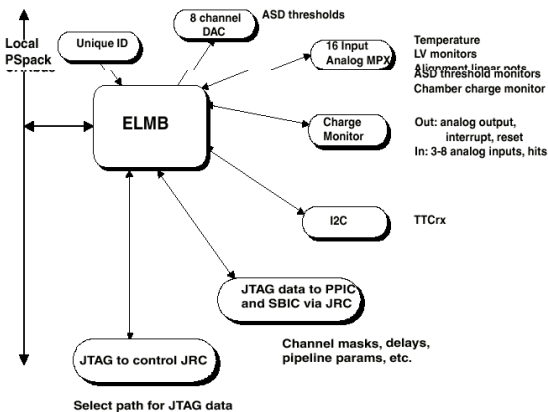
Figure 3: The services provided by the Patch Panel CAN node

The Star Switch and HipT modules are boards in 9U VME crates located on the periphery of the TGC big wheel. There are three such crates per octant as shown in Figure 1. The configuration, control and diagnostic functions for these modules can be performed via the JTAG interface of the on-board ASICs by a CAN node in each crate.

III.   MONITORING

A. Temperature and alignment

Each chamber will have a temperature sensor placed on the Faraday cage, near the ASD board. Each chamber will also have a number of displacement potentiometers to measure changes in its position relative to the neighbouring chambers. The measured changes in position will be used to calculate the chamber alignment.

B. Chamber charge

An analog amplifier output from one wire channel on each chamber is used to monitor the TGC performance. The integral of this signal is a measure of the charge generated by the avalanche at the anode wire. The voltage pulse signal is fed by a quasi-differential coaxial cable to the charge measuring circuit. The analog signals from all the chambers serviced by a Patch Panel are multiplexed by a 4-to-1 differential multiplexer followed by a differential-to-single-ended amplifier and a gated integration stage. The ADC digitises only if there is a minimum ionising particle, MIP, trigger received at the appropriate time relative to the gate. The MIP trigger is obtained from the ASD outputs that correspond to the analog channels. At the output of the gated integrator the voltage level is proportional to the wire charge. This voltage goes to the ADC input.

C. Voltages and thresholds

The three voltages supplied by the low voltage distribution system (+3V, -3V, +3.3V) are monitored at each patch panel.

The -3V is passed through an inverter and its output with the +3V and +3.3V are fed to the ADC. The discriminator thresholds which are generated by a DAC on the patch panel are monitored by a multiplexer and ADC. The circuit is designed to provide a predefined threshold if the DAC or ELMB fails.

IV.   CONFIGURATION OF ON CHAMBER ELECTRONICS

The TGC requires a method for configuring the 22800 ASICs of its on-chamber electronics. In addition to the configuration for triggering and general data acquisition, this system must provide calibration procedures (e.g. for thresholds and timing), verification of correct functioning, and remote diagnosis of on-chamber electronics that is suspected of malfunctioning.

The general requirements for the system include high reliability, radiation tolerance, and compatibility with PSpack and Patch Panel structure and space constraints. It is also important to have a diagnostic pathway to the trigger and DAQ electronics separate from the DAQ pathway. It is efficient to use the DCS system for the configuration of on-chamber electronics. Calculations and tests indicate that the CAN bus used for the DCS system can provide the required bandwidth.

A. How configuration is done

Configurable parameters of the on-chamber electronics include 128 Kbytes of begin-run configuration data: ASD discriminator thresholds, PPIC mask registers, SLB masks etc. There are an additional 70 Kbytes configurable parameters that will not be changed from run to run but only after timing calibrations (e.g. cable delay compensations). They must, however, be verified at frequent intervals, and restored if they have been corrupted by the cavern radiation (see Section 3.2).

We measured the throughput of a CAN bus at 125Kbaud over a 100m cable to be 34Kbit/s. Even this throughput is sufficient to download all 200KB of configuration parameters in a few seconds. In fact, these complete downloads will be rare, since the configuration is stored in non-volatile memory on the ELMB, and most parameters will not change from run to run.

Complete configuration parameter sets will be transmitted as compressed strings of data. Only the configuration data will be sent to the micro controller, which will decompress and download them through the JTAG TAP using a program stored in its Flash memory. When specific parameters are to be downloaded the rate is less important, and they will be transmitted as a command to change parameter i to value x.

The LCS will maintain a configuration database that contains different lists of configuration parameters that can be mixed and matched to build an actual configuration. The LCS will have a complete set of tools that display, add, remove and edit configurations in the database.

B. Single event upset detection and recovery strategy

Radiation in the cavern can cause Single Event Upsets, SEUs, that will corrupt, at some rate, the configuration data and the CAN node memory. ASICs hold 3 copies of the configuration and operate by majority logic. The 3 copies are compared in the ASIC and when a difference is detected an SEU register is set. The SEU flag is periodically monitored by the ELMB (JTAG). When the SEU flag is on, the ELMB reconfigures the ASIC (via JTAG). Until the reconfiguration, the voting logic keeps the ASIC operation correct. The CAN node microprocessor performs a CRC checks of its copy of the configuration string in SRAM. If the check fails, it copies the configuration from its EEPROM or requests a new copy from the LCS.

The CAN node's executable code is in flash memory, which is fairly robust against radiation. The microprocessor will periodically compute and verify a CRC for its flash memory. The flash memory can be reloaded by the LCS via the CANbus. The ELMB contain a mechanism whereby its two processors verify and correct each other's memory. The LCS will also periodically query the ELMB and if it does not respond will download the node programs and re-boot the microprocessor.

D. Calibration and testing in the cavern

Problems in the TGC chambers or electronics will be detected when the online histograms of hits and coincidences show a high occupancy, no occupancy or some other change in some area. Online monitoring will initiate diagnostic routines in the ROD that will identify the suspected modules and channels and perhaps a probable cause. Actions that would be taken as a result of problems include: Verify thresholds, calibrate thresholds, verify masks, diagnose failing channels.

To diagnose failing channels, PPICs or Slave Boards, the ROD crate will indicate which channels and what test patterns need to be run on them. Intelligent test patterns can be generated by the CAN node rather than downloaded.

V. Dcs software

The DCS software is divided into the following components:

The SCADA system (PVSS2) using a common framework developed at CERN. The TGC LCS SCADA application will allow interaction with ATLAS as well as local needs. The TGC LCS will also offer UI for installation, setup, calibration and diagnostics of TGC in stand-alone mode. TGC custom PVSS2 driver allows flexible communications with ELMB. PVSS@ scripts allow control via user interface or by DAQ commands.

LCS communicates with RDAQ using DDC interface. An API for communications has been implemented. The TGC DAQ can control relevant HW parameters through the DCS. The LCS collaborates with the ROD on calibrations and diagnostics

Hardware control software is resident in the CAN node ELMB that communicates with the attached hardware devices using appropriate protocols such as JTAG and I2C. The ELMB receives configuration, control and monitoring commands from the LCS, distributes the commands to the attached devices, assembles responses and transmits them back to LCS. The ELMB also performs routine autonomous monitoring and SEU correction, and predefined tests.

VI. Prototyping and testing the TGC DCS

The first fully functional prototype of the DCS for on chamber electronics (DCS-PS board) was designed, implemented and tested successfully in 2001. Figure 4 shows a photograph of the ELMB on the DCS-PS prototype.
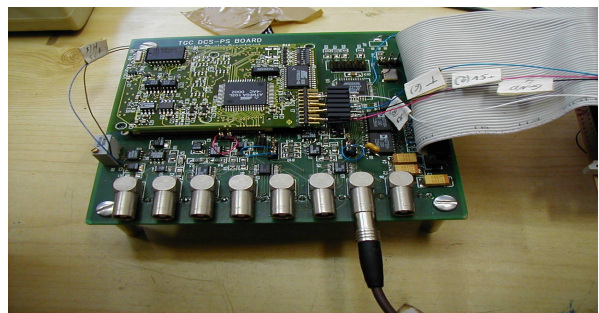

Figure 4: The DCS-PS prototype.

Using this board and a prototype of the PS board provided by the TGC electronics group at KEK a number of integration tests were performed. The TGC DCS components and board were also tested for the effects of a total integrated dose equivalent to 10 running years of LHC running, with a safety factor as required by ATLAS radiation hardness assurance plan.

A. Integration tests

The chamber charge measurement circuit was tested at the TGC cosmic ray test bench at the Technion [5]. The ELMB controls this measurement autonomously; send the finished histogram to the LCS once the required number of hits was recorded. Measurement results while varying ASD thresholds (top) and high voltage settings on the chamber (bottom) are shown in figure 5.
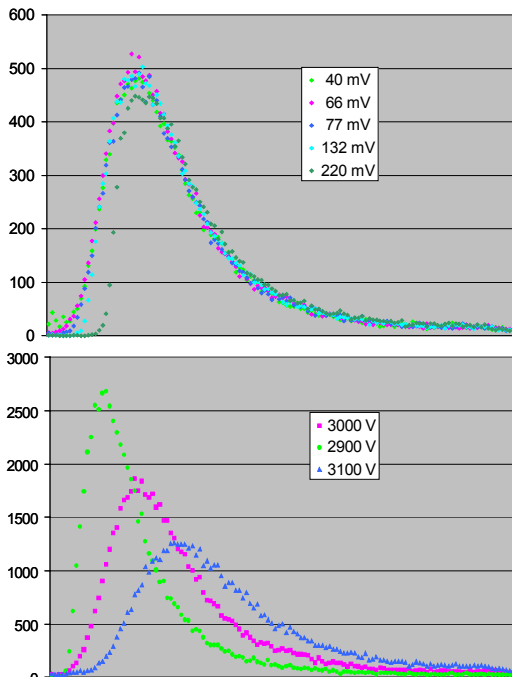
Figure 5: Chamber charge measurement with different ASD thresholds (top) and with different chamber HV

The circuits were radiated by a Co60 source at 0.8 Gray/min. up to a total dose of 220 Gy. The components were monitored by CAN bus and by a dedicated testing system.

The Altera EPM7032AET PLDs used in the CCMC circuits failed, and the temperature sensors exhibited some base line drift. All other components worked well at the end of the test.

A second test concentrated on the components of the DCS-PS card that displayed suspect behaviour in the previous radiation test. Xilinx XCR3032XL PLDs were being checked as an alternative to the Altera PLDs, which have previously failed. The failure of the ALTERA PLDS was confirmed. All other components, including the Xilinx PLDs, worked well after 190-213 GY.

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In November 2001 a TGC electronics slice test was held at KEK, Japan. In this test the full functionality of the DCS-PS board was demonstrated to work well with the PS board electronics designed by the TGC electronics group in Japan.

Among the items tested were: Set ASD threshold through DCS via PS board and maintain it through ELMB reset and reprogramming. Monitor operating parameters (LV, temperature, thresholds). Configuration of on chamber electronics: either a single parameter of an on chamber ASIC or bulk configuration of on-detector components. Capture snapshot of configuration from hardware and test a chain of components by applying test patterns to inputs and reading the response from outputs.

Further tests at CERN in summer 2002 demonstrated RDAQ-LCS integration using DDC [6]. Hardware parameters were set from RDAQ through DCS. On chamber ASIC parameter and thresholds were configured. Bulk configuration of on-detector components for start of run was implemented in an efficient way. The LCS confirmed command completion or failure according to HW response, to allow RDAQ transitions. The RDAQ application displayed hardware parameters read via LCS and DDC application.

B. Radiation testing

In May and July 2002 two total integrated dose radiation tests were preformed on TGC DCS components and boards.

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