The Clock and Control Board for the Cathode Strip Chamber Trigger and DAQ Electronics at the CMS Experiment

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Abstract

The design and functionality of the Clock and Control Board (CCB) for the Cathode Strip Chamber (CSC) peripheral electronics and the Track Finder crate at the CMS experiment are described. The CCB performs interface functions between the Timing, Trigger and Control (TTC) system of the whole experiment and CSC electronic modules located in 9U VME crates on the periphery of the detector and in the underground counting room.

I. INTRODUCTION

The CSC electronic system consists of on-chamber mounted Front End Boards (FEB), electronics on the periphery of the detector, and a Track Finder in the counting room [1]. The Trigger/DAQ electronic system resides in 60 VME crates located on the periphery of the return yoke of the CMS detector and includes: the combined Cathode LCT/Trigger Motherboard cards (TMB), the Data Acquisition Motherboard (DAQMB), the Muon Port Card (MPC) and the CCB. The Track Finder consists of a number of Sector Processors (SP), Muon Sorter (MS) and CCB, all residing in a single crate in the underground counting room.

All elements of the CSC electronics should be synchronized with the LHC operation. The TTC system [2] is based on an optical fan-out system and provides the distribution of the LHC timing reference signal, the first level trigger decisions and its associated bunch and event numbers from one source to about 1000 destinations. The TTC system also allows to adjust the timing of all critical signals. At the lowest levels of the TTC system, the TTCrx ASIC [3] receives control and synchronization information from the central TTC system through the optical cable and outputs recovered TTL-compatible signals in parallel form.

The CCB [4] is built as a 9U*400 mm VME board (A24D16 Slave) that comprises a mezzanine card with the TTCrx ASIC produced by CERN. All communication with other electronic modules is implemented over a custom backplane. The CCB can also simulate all the TTC signals under VME control. Additionally, various TTC signals (such as clock, L1 Accept etc) can be transmitted via the front panel. This option provides great flexibility for various testing modes at the final assembly and testing (FAST) sites where hundreds of the CSC chambers will be tested before installation at the experimental hall.

II. FUNCTIONALITY

The CCB resides on slot 13 in the middle of a 21-slot VME 9U peripheral CSC crate. Other slots in a crate are occupied by the TMB boards (9 or 8 total), DAQ Motherboards (9 or 8 total), MPC (one) and VME Master, that performs the overall crate monitoring and control. Each peripheral crate comprises the electronic modules that serve one sector of CSC chambers. All trigger/DAQ modules in the crate communicate with each other over a custom 20-slot backplane residing below the standard VME64x P1 backplane. The Track Finder crate utilizes the same architecture: 3U standard VME64x backplane and 14-slot custom backplane for communications between 12 SP, MS and CCB. This backplane is different from the peripheral custom backplane, but the CCB slot is designed in such a way, that the same CCB (with slightly reduced functionality due to the lower number of served modules) can be used.

A simplified block diagram and a picture of the CCB board are shown on Figures 1 and 2 respectively. The main components of the board are the TTCrx mezzanine card and another mezzanine card which holds an Altera EPF10K100ABC356 PLD and EPC2

configuration EPROM. The PLD has 274 input/output pins (almost all are used), accepts all signals from/to TTCrx parallel interface, backplane and VME buffers, front panel drivers/receivers, and performs all the main decoding and multiplexing functions.

There are two main operational modes of the CCB, defined under VME control. In "TTC" mode the CCB transmits to custom backplane those clock, signal and decoded commands that arrive from the TTC system via the TTCrx mezzanine card. In "Test" mode the clock can arrive from one of two other sources (an on-board quartz oscillator or a front panel input) while other signals and commands can be sent either under VME control or from the front panel. This mode supports various testing configurations for FAST sites.

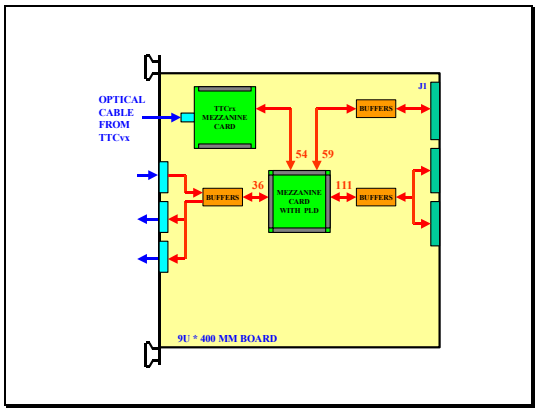

Figure 1: Simplified block diagram of the CCB

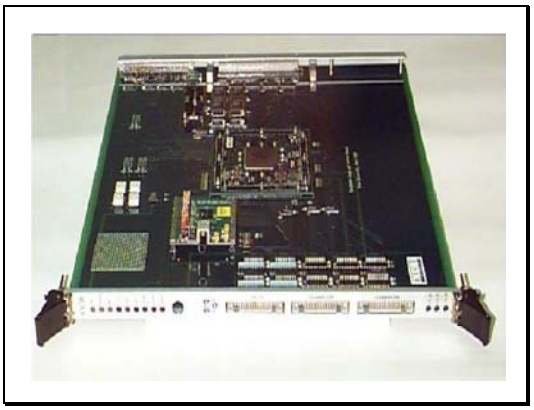

Figure 2: Clock and Control Board

III. Custom Backplane Interface

All the signals distributed over the custom backplane can be categorized in three different groups (Table 1): clock and control signals, reload signals, and special purpose DAQ/Trigger signals. The ccb_clock40 is distributed to every slot in the crate over individual point-to-point LVDS lines. All of the other signals are sent using GTLP logic, with active "low" level on the bus.

Table 1: Custom Backplane Signals

Clock and Control Signals	Reload Signals	Special purpose DAQ/Trigger Signals
Ccb_clock40	Tmb_hard_reset	Dmb_cfeb_calibrate[2..0]
Ccb_clock40_enable	Tmb_soft_reset	Dmb_l1a_release
Ccb_cmd[5..0]	Alct_hard_reset	Dmb_reserved_out[4..0]
Ccb_ttcrx_ready	Alct_cfg_done[8..0]	Dmb_reserved_in[2..0]
Ccb_evcntres	Tmb_cfg_done[8..0]	Alct_adb_pulse_sync
Ccb_bcntres	Tmb_reserved[0]	Alct_adb_pulse_async
Ccb_cmd_strobe	Mpc_hard_reset	Clct_external_trigger
Ccb_bx0	Mpc_soft_reset	Alct_external_trigger
Ccb_l1accept	Mpc_cfg_done	Clct_status[8..0]
Ccb_data[7..0]	Mpc_reserved[1..0]	Alct_status[8..0]
Ccb_data_strobe	Dmb_hard_reset	Tmb_l1a_release
Ccb_reserved[4..1]	Dmb_soft_reset	Tmb_l1a_request
	Dmb_cfg_done[8..0]	Tmb_reserved_in[4..0]
	Dmb_reserved[1..0]	Tmb_reserved_out[2..0]

The CCB normally distributes the Clock40Des1 deskewed clock provided by the TTCrx. Two other sources are 40.08Mhz clock from on-board oscillator (80.16Mhz frequency divided by 2) and front panel connector. There are fine and coarse delays for clock and command signals incorporated into TTCrx ASIC. They are programmable via I2C interface (using on-board PCF8584 controller) or via the optical path.

Six lines of Ccb_cmd[5..0] and ccb_cmd_strobe allow the CCB to decode up to 63 separate broadcast commands since they actually are buffered Brcst[7..2] and BrcstStr1 output lines of the TTCrx in a "TTC" mode. In a similar fashion, the ccb_data[7..0] and ccb_data_strobe are buffered Dout[7..0] and DoutStr lines of the TTCrx. In a "Test" mode all these signals can be sent via write to dedicated Control and Status Registers (CSR). Some critical signals (Ccb_evcntres, Ccb_bcntres etc) are sent over dedicated lines. A preliminary list of decoded TTC commands with respective codes is given in Table 2.

Table 2: Fast Control Bus Ccb_cmd[5..0] Decoding Scheme

Signal	Code (hex)	Description
BX0	1	Bunch Crossing Zero
L1 Reset	3	Reset L1 readout buffers
Hard_reset	4	Reload all FPGAs from EPROMs
Tmb_hard_reset	10	Reload TMB FPGAs from EPROM
Alct_hard_reset	11	Reload ALCT FPGAs from EPROM
Dmb_hard_reset	12	Reload DMB FPGAs from EPROM
Mpc_hard_reset	13	Reload MPC FPGAs from EPROM
Dmb_cfeb_calibrate0	14	CFEB Calibrate Pre-Amp Gain
Dmb_cfeb_calibrate1	15	CFEB Trigger Pattern Calibration
Dmb_cfeb_calibrate2	16	CFEB Pedestal Calibration
Dmb_cfeb_initiate	17	Initiate CFEB calibration
Alct_adb_pulse_sync	18	Pulse Anode Discriminator, synchronous
Alct_adb_pulse_async	19	Pulse Anode Discriminator, asynchronous
Clct_external_trigger	1A	External Trigger All CLCTs
Alct_external_trigger	1B	External Trigger All ALCTs
Soft_reset	1C	Initializes the FPGA on DMB, TMB and MPC boards
DMB_soft_reset	1D	Initializes the FPGA on a DMB
TMB_soft_reset	1E	Initializes the FPGA on a TMB
MPC_soft_reset	1F	Initializes the FPGA on a MPC
Send_bcnt[7..0]	20	Send Bunch_Counter[7..0] to ccb_data[7..0] bus
Send_evcnt[7..0]	21	Send Event_Counter[7..0] to ccb_data[7..0] bus
Send_evcnt[15..8]	22	Send Event_Counter[15..8] to ccb_data[7..0] bus
Send_evcnt[23..16]	23	Send Event_Counter[23..16] to ccb_data[7..0] bus

There are six possible sources of L1Accept signals: TTCrx, Tmb_l1a_request (backplane), dedicated front panel input, VME command, ALCT_adb_pulse_sync, and ALCT_adb_pulse_async. The selected source can be delayed for a programmable number of 40Mhz clock cycles (up to 255) for testing purposes.

Hard Reset signals allow all or selected boards in the crate to start reconfiguration of their FPGA from EPROMs. Periodic reconfiguration would prevent malfunctioning of the peripheral and on-chamber electronics because of Single Event Upsets (SEU) in the configuration SRAM of FPGA due to neutron fluxes. As soon as the reconfiguration completed, all boards assert Conf_done signals indicating their active status. Soft_reset signals will allow to initialize FPGA after reconfiguration. Similarly to Hard Resets, these signals can also be generated under VME control in "Test" mode.

Special Purpose DAQ and Trigger signals are intended mainly for various testing and calibration modes at FAST sites. All signals (except the ALCT_adb_pulse_async) are synchronized with the selected clock source. In "Test" mode they can be generated upon VME

commands. Anode and Cathode Status[8..0] signals are also transmitted to front panel in ECL levels.

IV. Irradiation Test

On the periphery of the return yoke of CMS the expected Total Ionizing Dose during 10 years of LHC operation is below 1 kRad and the neutron fluence (for E>100KeV) is below 10^{11} cm^{-2}. We chose a proton beam of 63MeV at the UC Davis facility to simulate the effect of the neutron environment at the LHC. Since neither the TTC, nor VME systems were involved in a test, we designed a special logic based on pseudo-random bit stream generators running at 40Mhz. An error signal was transmitted to the control room for counting. Both PLD and EPROM were accessible remotely over JTAG cable. The PLD was irradiated with a dose up to 1 kRad; 20 errors were observed, with an average dose of ~50 Rad needed to get an error. This number corresponds to cross section of SEU of $2.5x10^{-9}$ cm^2. All errors were recoverable upon reconfiguration from EPROM, no latch-ups were observed. The EPROM was continuously read back for error checking; no errors were observed up to 25.6 kRad.

Assuming that the PLD is the only source of SEU on the board and the total LHC run time at full luminosity is $5x10^7$ c, the worst case SEU rate would be $5x10^{-6}$ per second, or 1 SEU per CCB in about 60 hours. The damage of the configuration data seems to be the primary effect during irradiation. One solution to mitigate it would be to reconfigure the PLD periodically the same way as envisaged for other modules in the peripheral crate. An alternative is to replace the Altera PLD with an anti-fuse FPGA (for example, Actel A54SX32). Based on tests reported in [5] the cross section of SEU for this Actel device is about three orders in magnitude less than for an Altera EPF10K100.

V. Conclusion

20 CCB's have been built and tested so far. Most of them are intended for FAST sites in USA, Russia and China. Software development for the integration with the new DMB (designed at OSU), TMB (designed at UCLA) and MPC (designed at Rice University) boards is in progress. One board will be used for tests of the Track Finder crate at the University of Florida (Gainesville).

VI. References

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