A very low offset voltage auto−zero stabilized CMOS operational amplifier

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Abstract:

A high precision operational amplifier has been developed in a standard .8µ CMOS process. A continuous time auto−zero stabilized architecture was used, that leads to a typical input offset voltage less than 2µV −100nV/°C. The amplifier with its output buffer consumes 5mW at a supply voltage of +/− 2.5V. The gain bandwidth product is 2MHz while the slew rate is respectively −6V/µS and +8.8V/µS on 10pF with 10KΩ load. This amplifier is suitable for the control of large dynamic (>10E5) calibration signal, and for very low signal instrumentation.

I) Introduction

Offset is a very important parameter for many applications: high energy physics calibration systems, low signal sensor interfaces, high accuracy instrumentation. A careful layout design could be combined with internal trimming to reduce the offset from a few mV down to around 100µV. The screening steps required for such a strategy could take a long time and consequently would be very expensive. Moreover, in many applications, one has a concern with the offset drift (with the time, temperature, power supply etc..).

Therefore auto−zero stabilization architecture is a more efficient and elegant solution to the offset cancellation. CMOS technology is suitable for such a design, due to its analog switch capabilities, lower power architectures and low cost.

In this paper, is presented the design of an auto−zero amplifier in a CMOS standard process using a folded cascode architecture.

II) Auto−zero amplifier: overview

A continuous auto zero amplifier requires two internal amplifiers. The block diagram is shown in figure 1. The so called 'Main amplifier' is unswitched and continuously available for the incoming signal amplification.

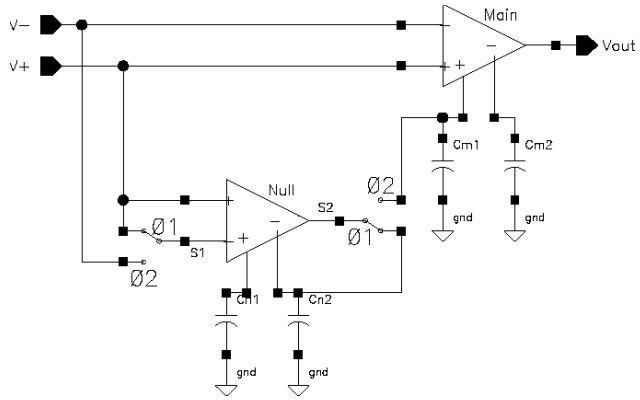

figure 1: Auto zero amp, block diagram

There are two alternating successive phases for the offset cancellation. During the first one, the 'Null' amplifier is disconnected from the signal path for its auto correction. A correction signal Vcn is generated and held on C_n external capacitors connected at the the auxiliary inputs.

During the second phase, the Null amplifier is reconnected to the Main and senses its input offset. Another correction voltage Vcm is generated this way and stored on capacitor Cm for the Main amplifier correction.

Each internal amplifier could be modelized with two differential inputs: a primary and an auxiliary one as in figure 2 .

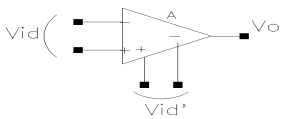

figure 2 Internal amplifier model

The output signal can be expressed as:

$$V_0(s) = A(s).V_{id} + A'(s).V'_{id} + A(s).V_{os}$$

With the assumption that the primary and auxiliary inputs are combined in the first stage of the amplifier, their respective dominant poles will be very closed. Then we could define a constant ratio α between the open loop gains:

$\alpha = A0(s) / A'(s)$

Consider now the full auto−zero amplifier in a feedback loop as in figure 3 ,where V_{osm} and V_{osn} are respectively the

residual offset of the Main and Null internal amplifiers. During phase ϕ_1, S_1 short−circuit the Null amplifier and its output charges the capacitor Cn via S_2 to the the Vc_n value .

$$V_{c_n} = -\frac{A_n}{1+A'_n}V_{os_n} + \Delta V_{c_n} \cong -\alpha_n V_{os_n} + \Delta V_{c_n}$$

ΔV_{c_n} is a perturbation voltage related to the charge injection , noise etc..

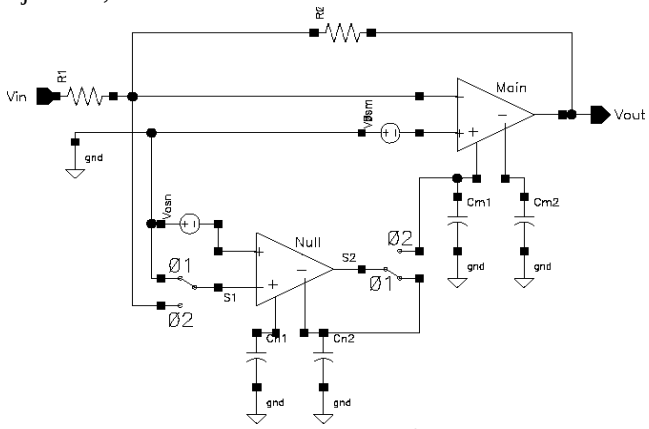

Figure:3 Simulation configuration

During the phase f_2, the Null amplifier senses the offset of the Main and stores the resulting control voltage Vcm on the capacitor C_m.

In a feedback configuration as shown in figure 3 one obtains $V_{out} = A_m(V^+ - V^- - V_{os_m}) + A'_m V_{c_m}$ and

$$V_{c_m} = A_n(V^+ - V^- - V_{os_n}) - A'_n V_{c_n} \cong A_n(V^+ - V^-) - \alpha_n V_{os_n} - A'_n \Delta V_{c_n}$$

In the case V_{out}=0 and $V_+ - V_-$ = Vos(2) (offset during the phase ϕ_2), one can deduce

$$V_{os}(2) \cong \frac{\alpha_m V_{os_m} + \alpha_n V_{os_n}}{A_n} + \frac{\Delta V_{c_n}}{\alpha_n}$$

with $(A_n A'_m >> A_m)$

During the next ϕ_1 phase, the offset will become. $V_{os}(1) = V_{os}(2) - \frac{\Delta V_{c_m}}{\alpha_m}$ leading into:

$$V_{os}(1) = \frac{(\alpha_m/\alpha_n)V_{os_m} + V_{os_n}}{A'_n} + \frac{\Delta V_{c_n}}{\alpha_n} - \frac{\Delta V_{c_m}}{\alpha_m}$$

After many iterations of phases ϕ_1 and ϕ_2 the offset will decrease progressively; its maximum value is:

$$V_{os}^{max} = \frac{a V_{os_m}^{max} + V_{os_n}^{max}}{A'_n} + \frac{\Delta V_{c_n}}{\alpha_n} + \frac{\Delta V_{c_m}}{a\,\alpha_n}$$

where $a = \alpha_m/\alpha_n$. It could be shown that the optimum offset value is reached when α_m and α_n are defined as:

$$\frac{\alpha_m}{\alpha_n} = \sqrt{\frac{\Delta V_{c_m}.V_{os_n}^{max}}{\Delta V_{c_n}.V_{os_m}^{max}}} \quad and \quad \alpha_n = \sqrt{\frac{A_n \Delta V_{c_n}}{V_{os_n}^{max}}}$$

III)INTERNAL AMPLIFIER

The schematic of each of the internal amplifiers is shown in figure 4. The general architecture is the folded cascode which provides a high open loop dc gain.

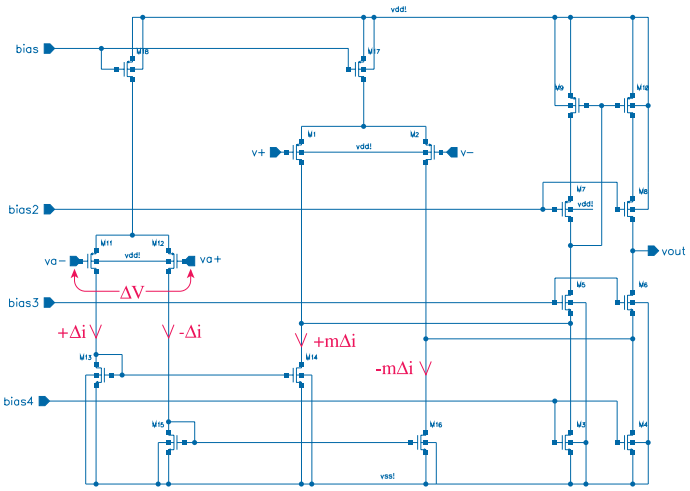

Figure 4: Internal amplifier schematic

The offset depends on how well the quiescent current is balanced through the input differential stage. This balance is controlled via the auxiliary inputs (Va+, Va−). To improve the bandwidth, a high−swing cascode current mirror is used in the amplification stage (M_7−M_{10}).

An additional common source output stage has been added to the Main amplifier to enhance its driving capability: the output impedance of such a buffer was found around 400Ω. The open loop gain (from the primary inputs to the buffer output) is more than 100dB.

The auto zero architecture shown in figure 3 has been simulated in the following configuration:

- feedback gain =100
- initial offset to be compensated = +/−10mV
- Clock frequency = 100Hz

This simulation demonstrates how the compensation is performed step by step until the offset is closed to noise.

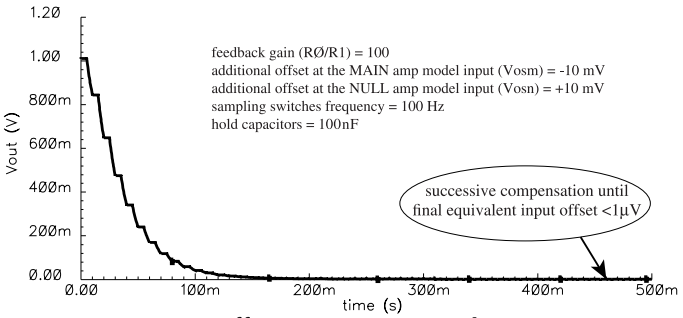

Figure 5: offset compensation step by step

IV)EXPERIMENTAL RESULTS

This amplifier has been designed in a standard .8µm. process, and produced via a multi project center. 5 prototypes have been tested. The mean value found for the offset is less than 2µV.

An evaluation of the drift with the temperature is shown in figure 6. Neither the min nor the max characteric is linear. But one could see a medium value for the drift around 100nV/°C.

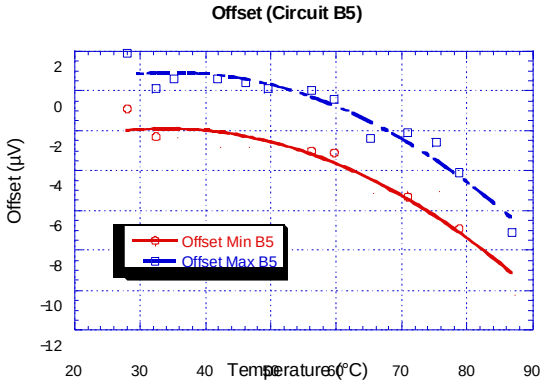

Figure 6: Offset drift with the temperature.

Figure 7 shows the equivalent input noise voltage spectrum measured while the total power dissipation was set at 5mW (including the output buffer), and the supply voltage was +/−2.5V .

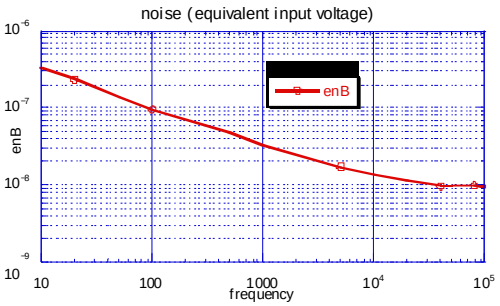

Figure 7: Equivalent input noise voltage.

We show the large signal pulse response in the following figures 8 and 9, where the feedback gain was set to 10, on a 10KΩ//10pF load.

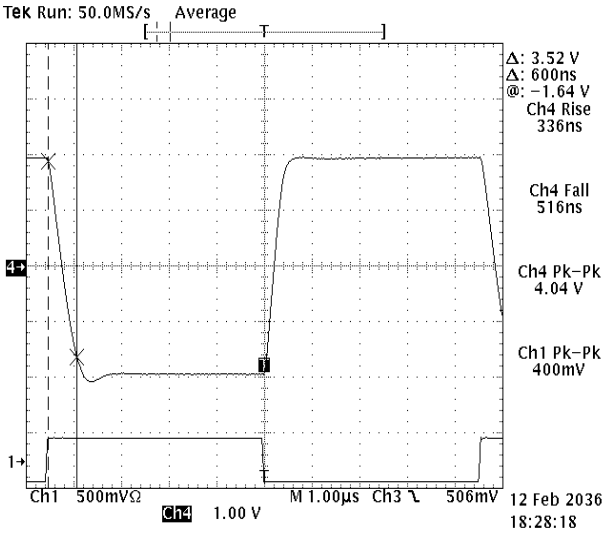

Figure 8: Negative Slew−rate=6V/µs

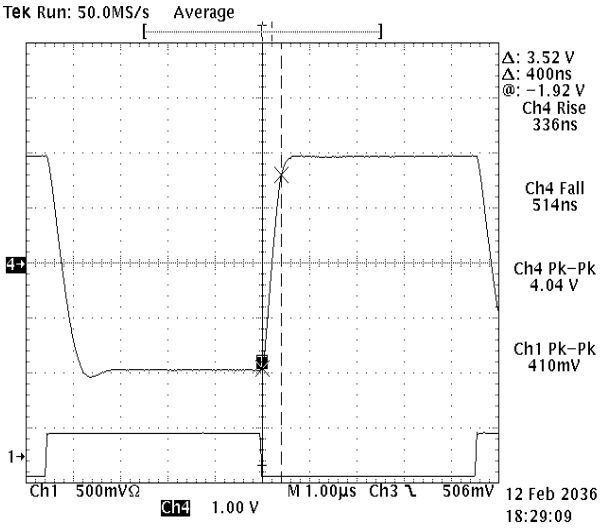

Figure 9: Positive Slew−rate = 8.8 V/µs

IV)CONCLUSION

We have described the architecture of an auto−zero amplifier. Very promising results for the first prototypes are presented. This circuit is an important cell which will be used in the next future to develop a large dynamic integrated calibration circuit.