Micro & Nanoelectronics

LECC-Colmar workshop 9th Sept.2002

This talk addresses some fundamental questions of miniaturization in microelectronics

- Trends in microelectronics and nanoelectronics
- Is there an end to CMOS miniaturization?
- Impact of microelectronics on HEP electronics instrumentation
- What HEP community could gain from the industrial development the next generation of nanoscale CMOS technology
- What is nanoelectronics?
- Is nanoelectronics promising?

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OUTLINE

- Microelectronics trends
- Evolution of front end electronics for HEP instrumentation
- Miniaturization of nanoscale CMOS
- Future of HEP front end electronics in nanoscale CMOS technology
- Nanoelectronics basics and devices

1 .Introduction

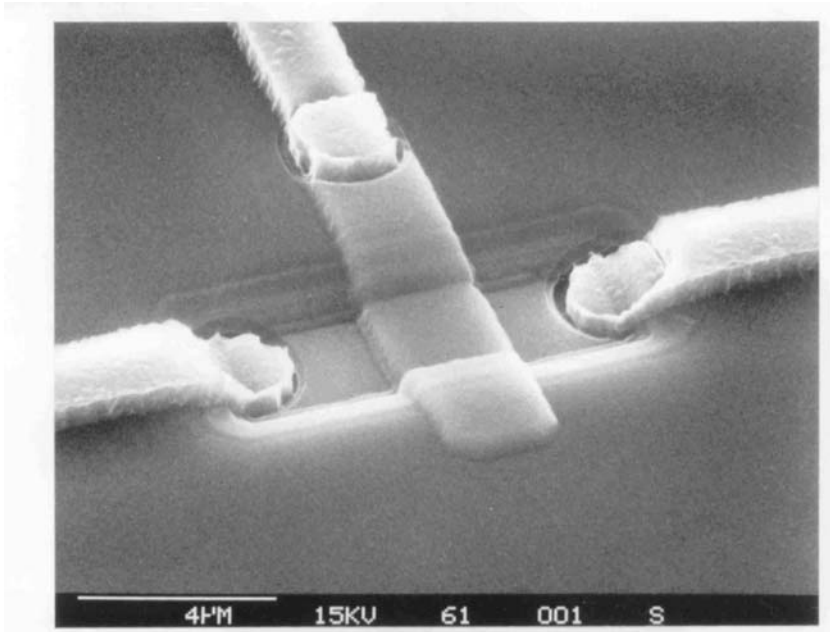
Microelectronics trends

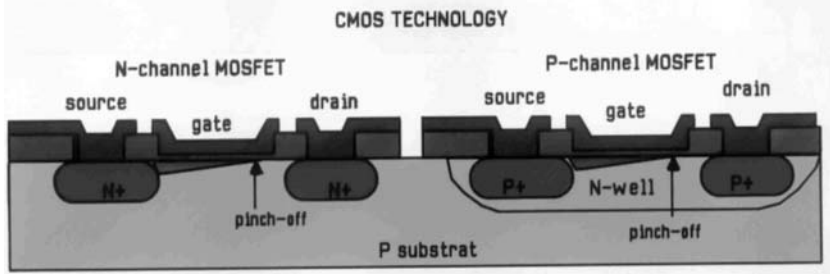
- ✓Moore Law
- ✓CMOS Scaling
- ✓CMOS Gate length trends

MOSFET

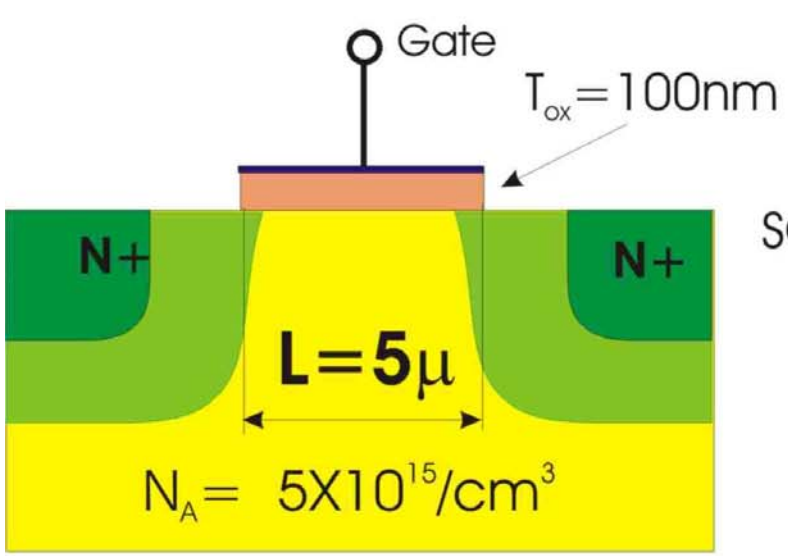
The world's most abundant artificial object!

- ✓As MOSFET was 20 years ago at the 1st MPW:
  - ✓5 micron technology generation with LOCOS isolation.
  - ✓Gate oxide thickness:40nm
- ✓Today:
  - ✓0.25 micron 5nm CERN MPWs
  - ✓0.13micron: industry state of the art, 2nm gate oxide thickness.
- ✓Driving concept behind CMOS
- ✓ miniaturization: SCALING





MOSFET scaling principle

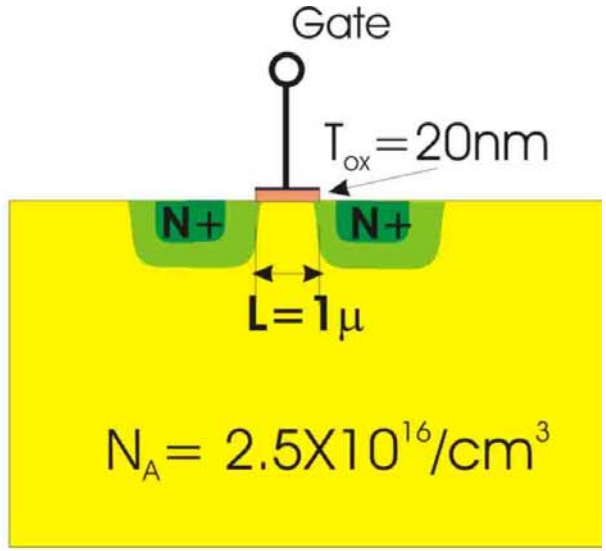


SCALING CHANGES

$X' = X/S$

$V' = V/S$

$N_A' = N_A \times S$



Depletion

$$\mathbf{X_D'} = \sqrt{\frac{2\varepsilon_{SI}(V/S + \psi)}{q(SN_A)}} \cong \frac{\mathbf{X_D}}{\mathbf{S}}$$

Threshold Voltage

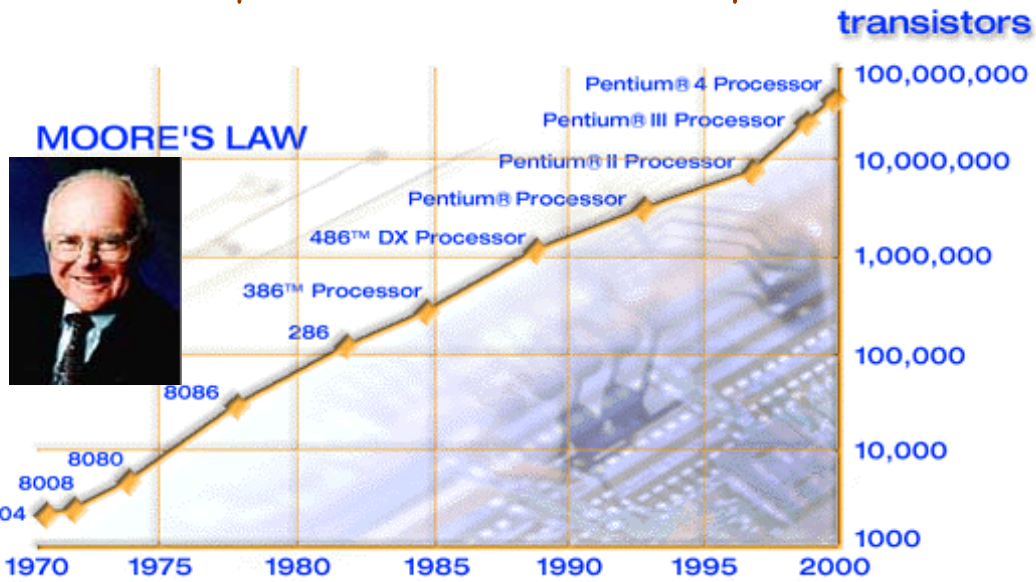
$$\mathbf{V_T'} \cong \frac{\mathbf{V_T}}{\mathbf{S}}$$

Drain current

$$\mathbf{I_D'} \cong \frac{\mu\varepsilon_{ox}}{t_{ox}/S}\left(\frac{W/S}{L/S}\right)\left(\frac{V_g - V_T - V_D/2}{S}\right)\left(\frac{V_D}{S}\right) = \frac{\mathbf{I_D}}{\mathbf{S}}$$

Scaling and Moore's Law

Trends in microprocessor development



4004 in 1971

Pentium4 in 2000

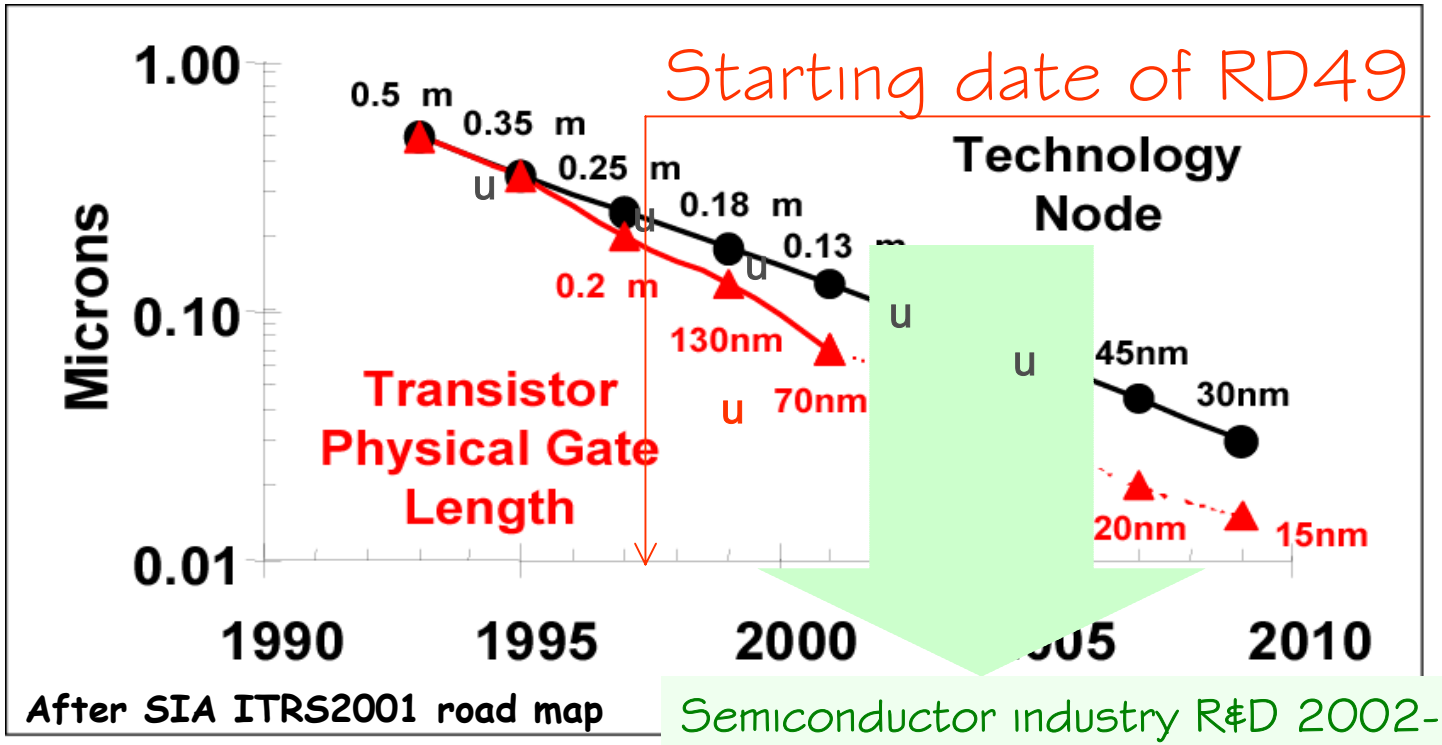
Si starting block

4004	1971	2,250
8008	1972	2,500
8080	1974	5,000
8086	1978	29,000
286	1982	120,000
386™ processor	1985	275,000
486™ DX processor	1989	1,180,000
Pentium® processor	1993	3,100,000
Pentium II processor	1997	7,500,000
Pentium III processor	1999	24,000,000
Pentium 4 processor	2000	42,000,000

Source: Intel

2001 SIA Technology Roadmap

Effective gate length and physical gate length diverge



Semiconductor industry R&D 2002-2007
i.e Crolles2: ST+Philips+Motorola+TSMC)

Node scaling x0.7

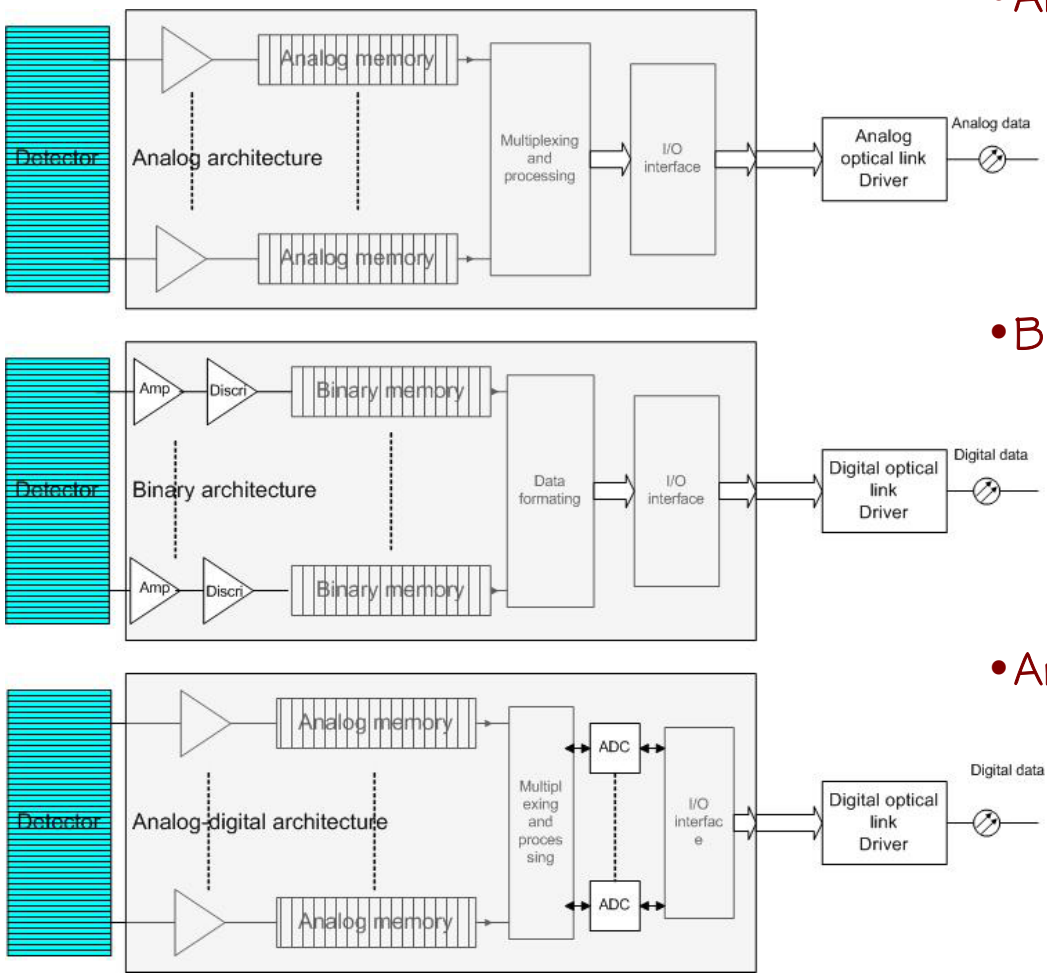
Year	1997	1999	2001	2004	2007	2010	2013	2016
Tech node [nm]	250	180	130	90	65	45	32	22
Node cycle time	2	2	2	3	3	3	3	3
DRAM Gbits	0.52			2	4			64
Transistors/chip			276M		1106M			8848M

2.ASICs for LHC

Evolution of front end electronics for HEP

- ✓Miniaturization: Channel density
- ✓Detector integration: trackers
- ✓System integration: SOC
- ✓Radiation hardening: generic

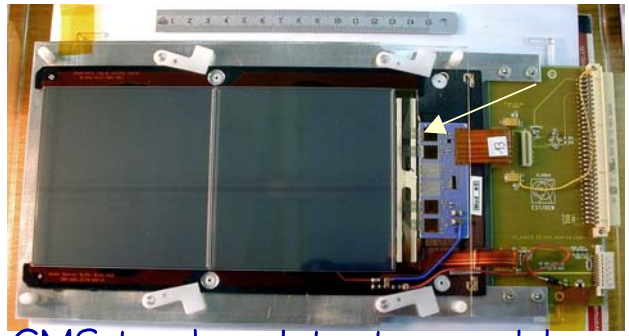
Generic LHC tracker readout



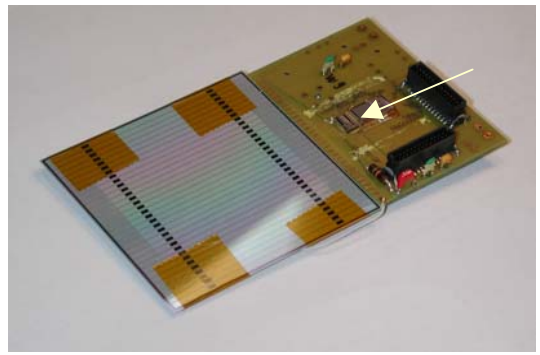
- Analog CMS tracker APV25 radtol
  - Charge amplifier
  - Analog memory 2us deep
  - Signal deconvolution
  - Analog multiplexing 128 channel
  - Serial analog optical transmission
- Binary ATLAS ABCD3T DMILL
  - Local hit decision
  - Preamplifier shaper discriminator
  - Digital memory 2.5us latency
  - Data formatting
  - Token ring, serial digital transmission
- Analog-digital ALICE PASCAL radtol
  - Charge amplifier, shaper
  - Analog memory 4us
  - Readout of the full memory
  - On chip digitization 10bit 5Msamp /s
  - Serial digital transmission

ASICs for LHC tracking systems

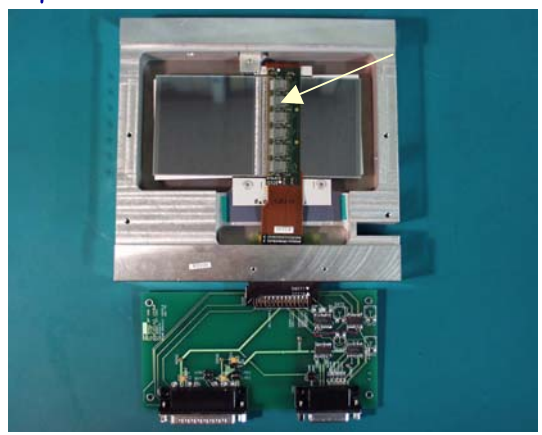
- ✓ Analog scheme – CMS tracker APV25
  - ✓ Preamplifier + shaper
  - ✓ Analog memory buffering trigger latency
  - ✓ Analog multiplexer
  - ✓ Analog data transmission for APV25
- ✓ ECAL preshower PACE
  - ✓ ADC and digital transmission for PACE
  - ✓ Hit decision after level-1 trigger decision
- ✓ Binary scheme ATLAS ABCD3T
  - ✓ Local hit decision
  - ✓ Preamplifier shaper discriminator
  - ✓ Digital memory
  - ✓ Data compression and formatting
  - ✓ Digital data transmission
  - ✓ Hit decision before level-1 trigger decision
- ✓ Pro and cons of the analog and binary scheme
  - ✓ Wait and see systems in operation…



CMS tracker detector module



CMS preshower detector module

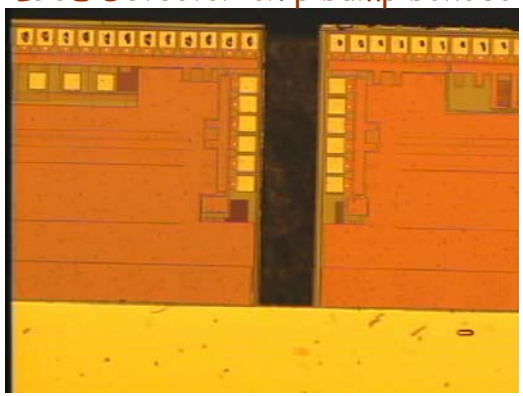


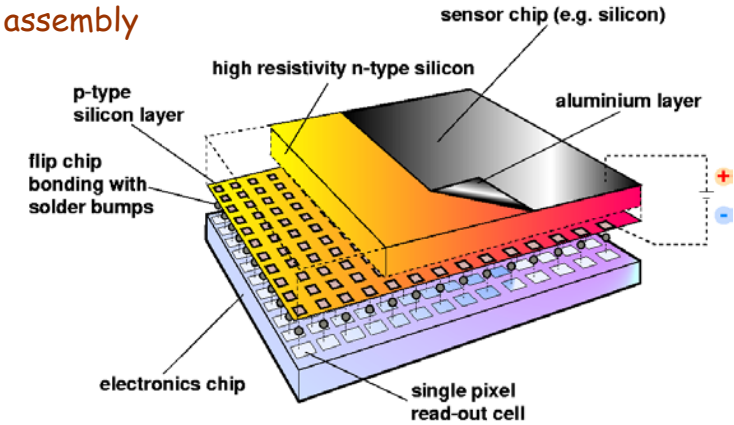
ATLAS SCT silicon tracker module

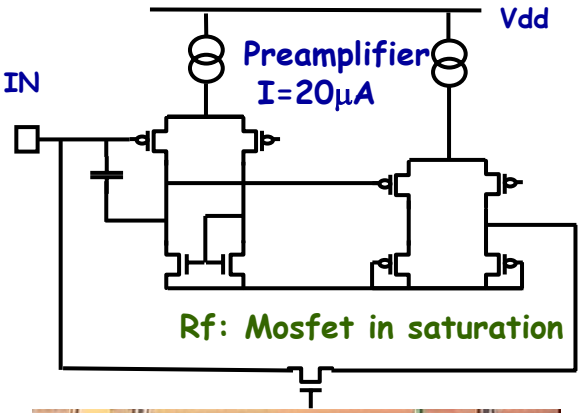
Alice-LHCb pixel detector 8192 ch

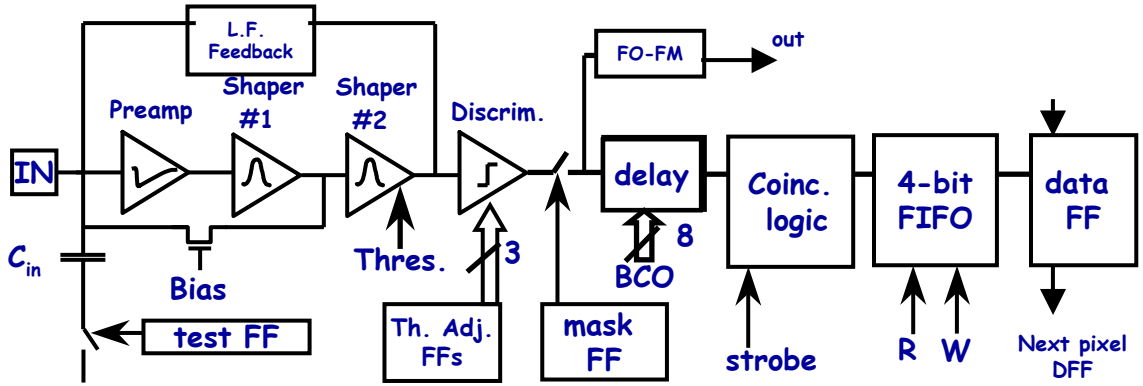
- ✓8192 pixel cells/die
- ✓13 millions transistors/die
- ✓5 dies /detector
- ✓Differential preamp
- ✓Power/die:0.8W
- ✓Pixel size:50 x 450 μm
- ✓All processing functions on pixel
- ✓ENC = 100 e- rms @ C_{det}=0.1pF
- ✓Threshold mismatch:150 e- rms
- ✓Vdd=1.8V

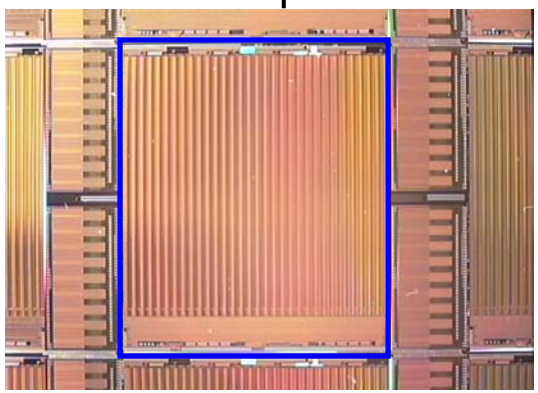
ALICE Detector-chip bump bonded assembly

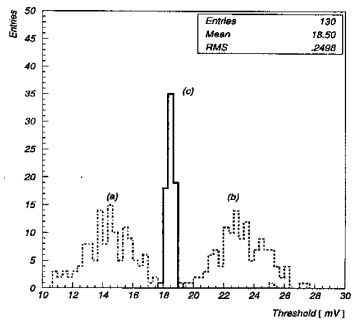




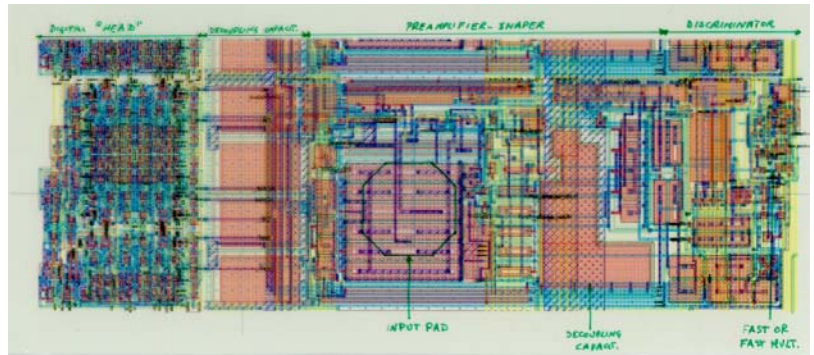








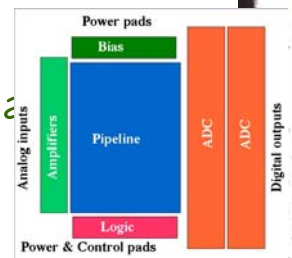
Omega-2 mismatch correction

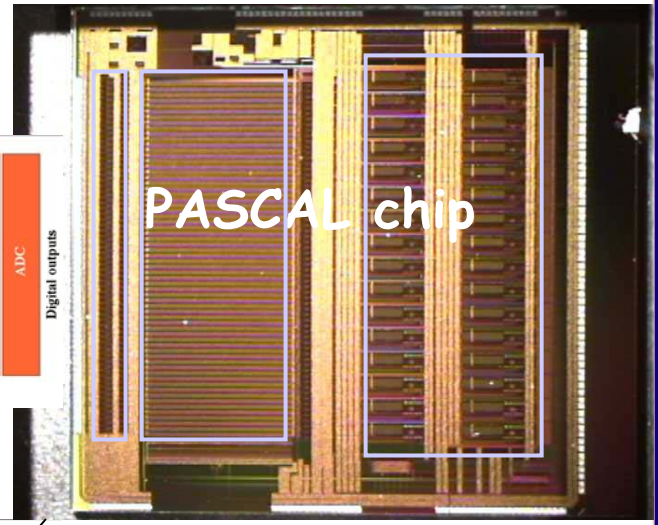


After M. Campbell, W Snoeys, R. Dinapoli, G. Anelli

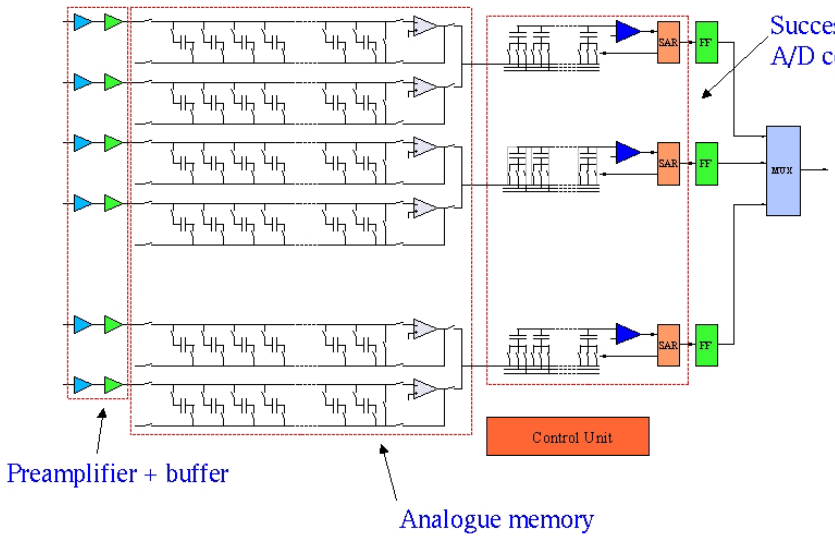
ALICE SDD PASCAL towards SOC

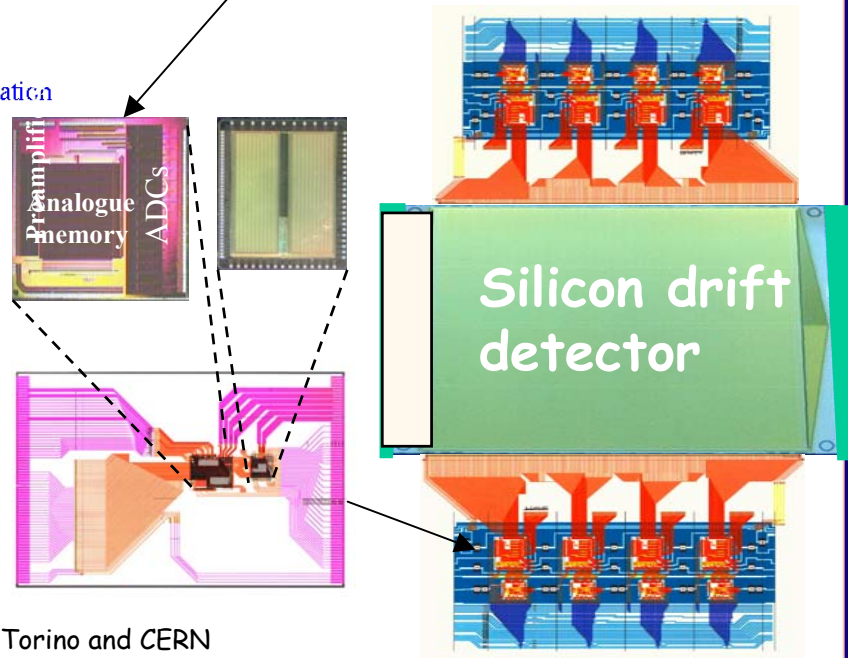
- PASCAL readout chip (time–space projection)
  - Analog-digital readout architecture
  - Preamplifier shaper 40ns peaking time
  - Analog memory 256 cells deep x 64 cha 40-80Mhz writing speed
  - 32 x 10bit-ADC 5Msamples/s ADC
  - Readout system equivalent to 40MHz 10bit ADC with 2mW/channel





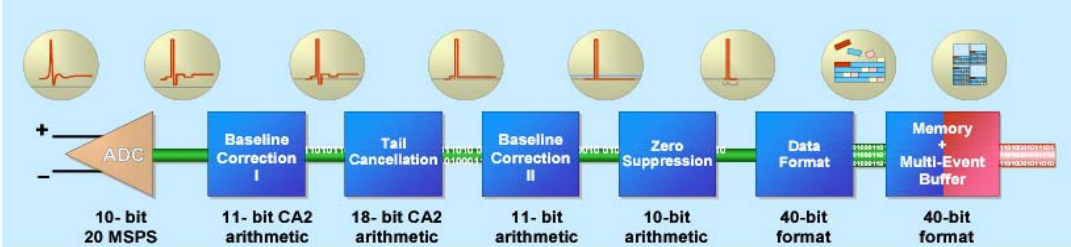
- Block diagram



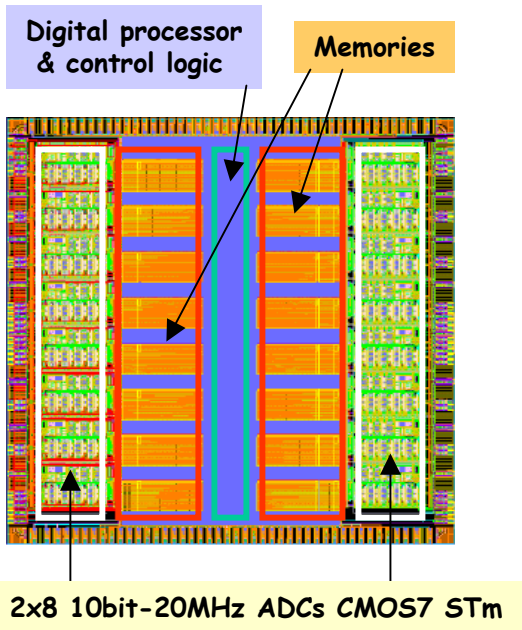


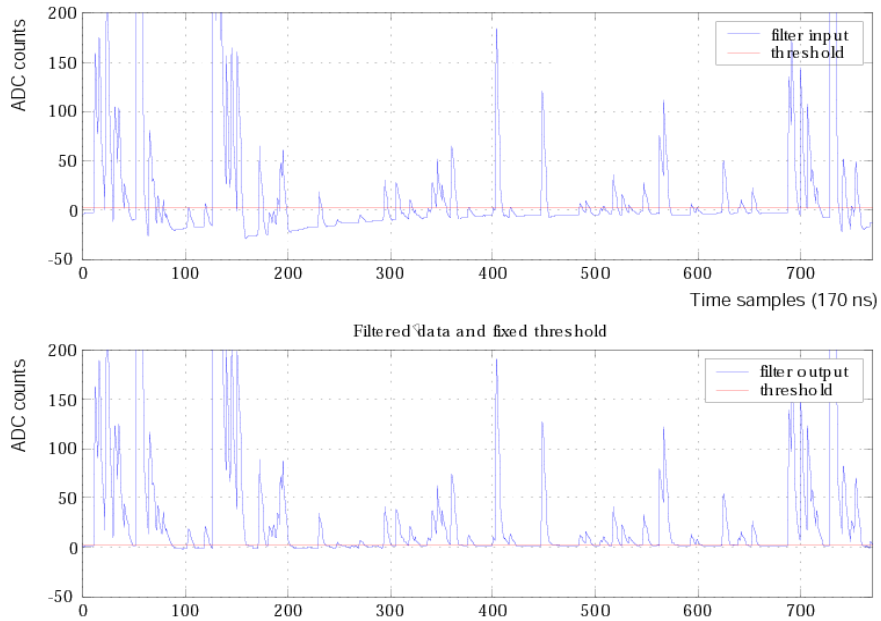
After G. Anelli, P. Giubellino, A. Rivetti,G. Mazza INFN Torino and CERN

ALTRO chip ALICE TPC



- 8-ch ALTRO readout chip performs
  - -64 mm², 29mW/ch
  - -Analog-digital conversion
  - -Digital tail cancellation
  - -Digital baseline correction
  - -Digital data formatting



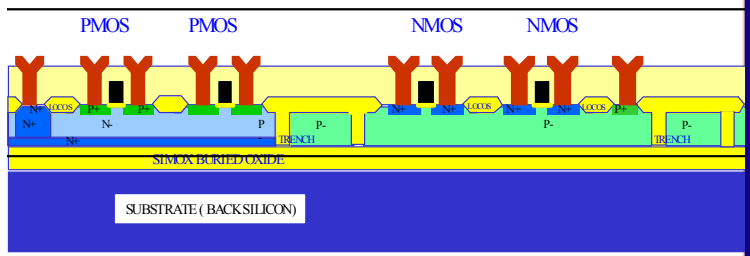


After L. Musa/CERN

Rad-hard, rad-tol technologies

DMILL RH technology

- ✓ BiCMOS 0.8 μm technology on SOI with partly depleted film.
- ✓ Gate oxide hardened by technology, latch-up hardened by SOI.

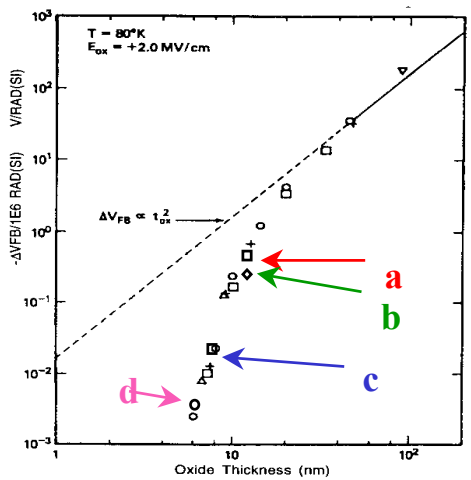


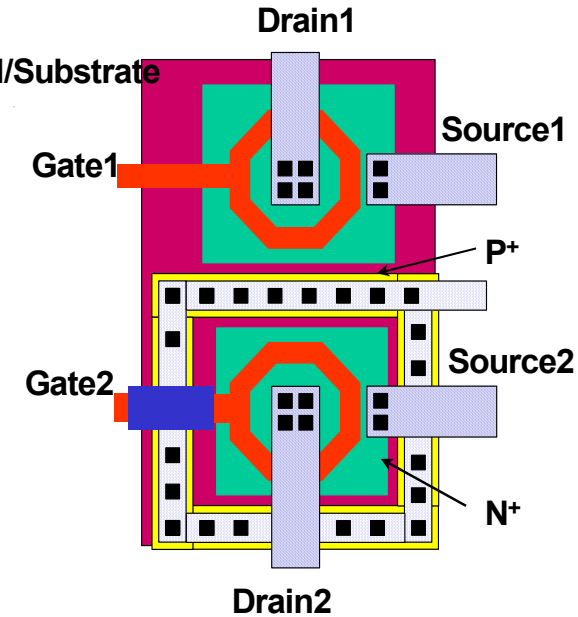
Hardening by technology

0.25μm rad tolerant CMOS RD49

Hardening by design

- ✓ Edgeless NMOS
- ✓ Guard rings
- ✓ Thin oxide tunneling
- ✓ Tolerance up to ten of Mrads





Hardening by design

3. Future Trends of CMOS

Is there an end to miniaturization?

- ✓CMOS feature sizes will enter the range of under 100nm, where a number of serious problems await, technological, financial and physical.
  - ✓*CMOS will hit fundamental barriers caused by quantum effects*
  - ✓Lithography technology will reach a limit with EUV, cost of mask set, millions dollars.
  - ✓*It becomes increasingly difficult to manage heat dissipation from ULSI circuits as transistor count exceeds 100 millions per die.*
  - ✓Design complexity and architecture issues
  - ✓*The cost of semiconductor production facilities is expected to exceed US$5 billion by 2006 .*

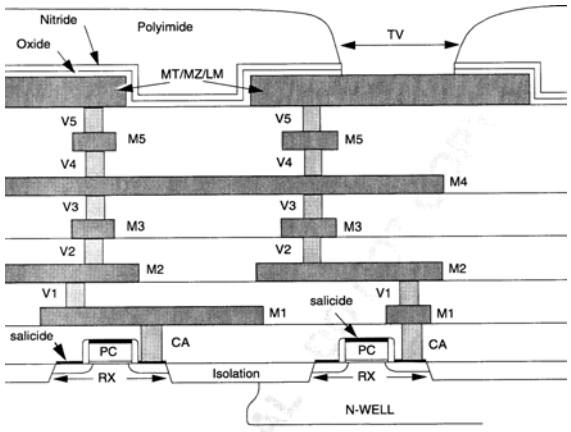
IBM 130nm CMOS

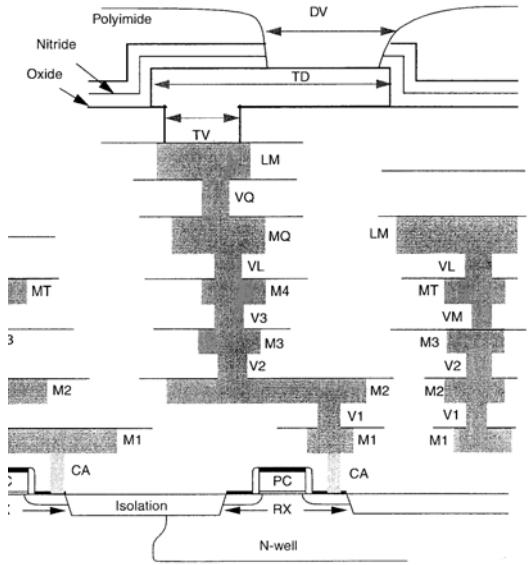
CMOS6SF 0.25µm

- ✓Vdd=2.5V
- ✓Twin Well, P-epi on P+
- ✓tox,phys: 5nm
- ✓Planarized passivation and inter-level dielectrics
- ✓STI
- ✓low resistance Ti salicided N+ and P+ polysilicon and diffusions
- ✓Metal pitch :0.64

CMOS8SF 0.13µm

- ✓Vdd= *1.2V, option 1.5V*
- ✓Twin Well, *non-epi* on P+
- ✓tox: *1.7, 2.2, 5.2*nm
- ✓same planarization *with low k-value dielectrics*
- ✓STI
- ✓low resistance Cu salicided N+ and P+ polysilicon and diffusions
- ✓Metal pitch 0.32



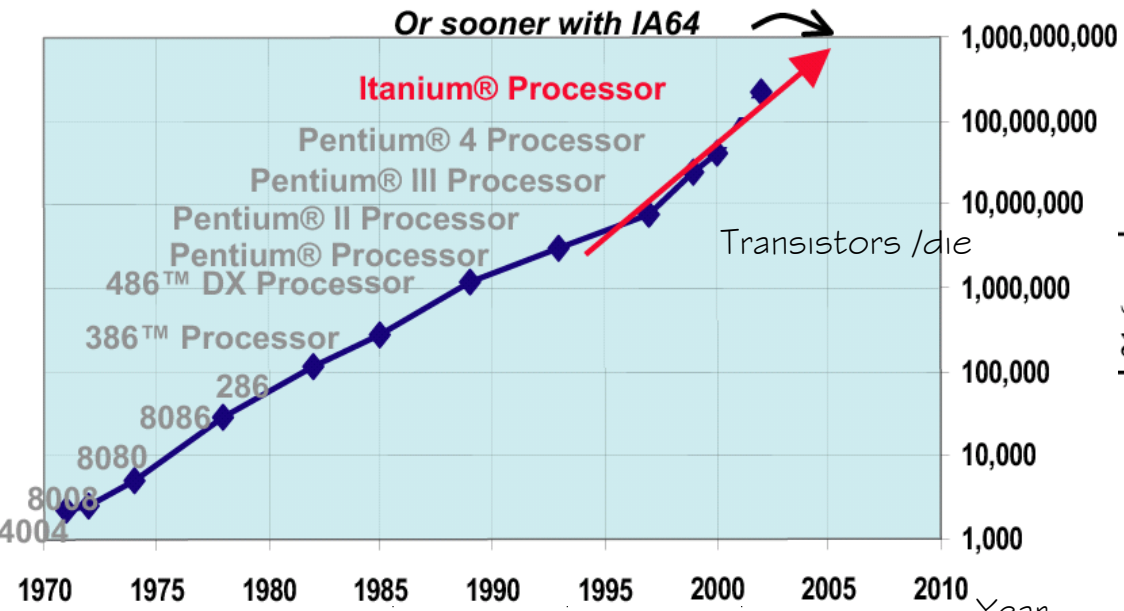


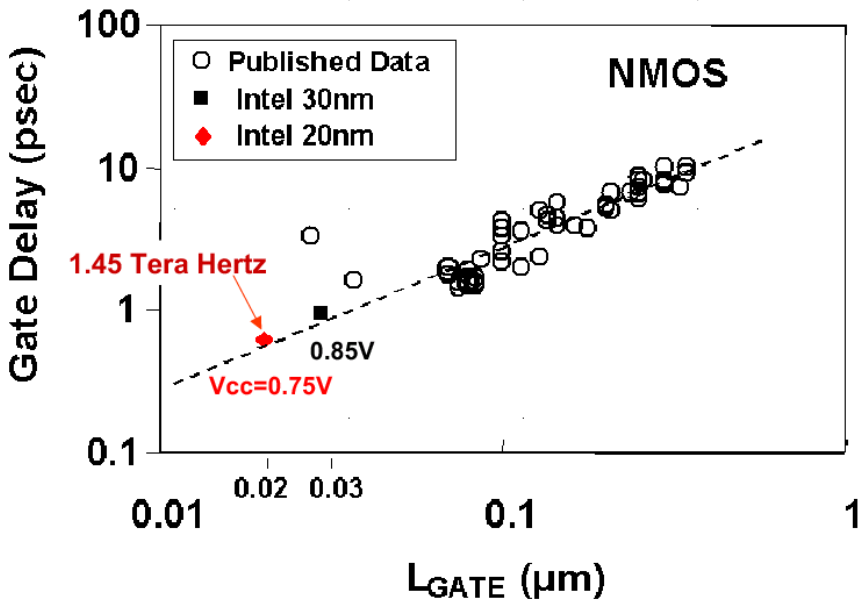
Issues of extreme MOSFET scaling

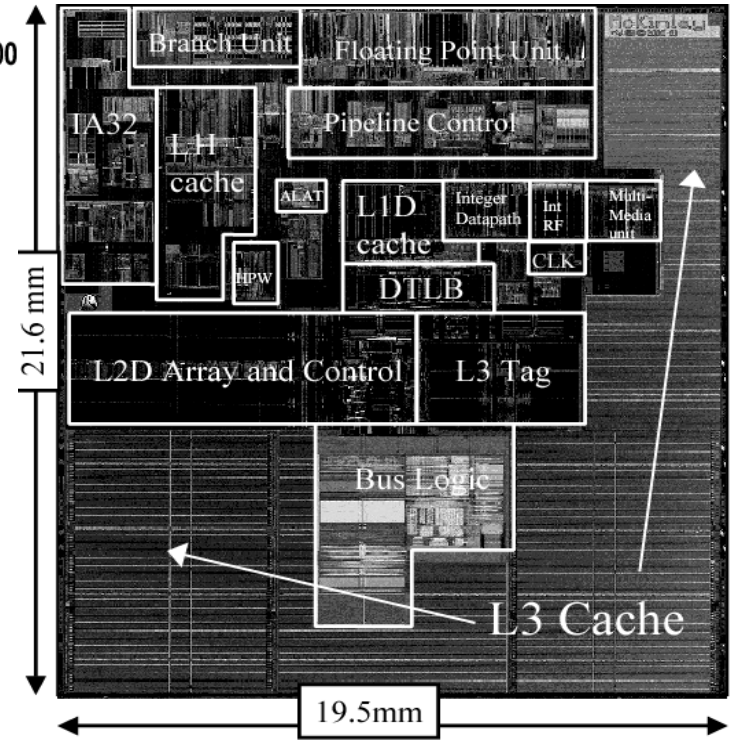
100nm feature size and below

- ✓ Quantum effects
  - ✓ Quantum confinement (ITRS RB wall)
  - ✓ Doping quantum effects (ITRS RB wall)
  - ✓ Tunneling limits (ITRS RB wall)
- ✓ Short channel effects are very pronounced
  - ✓ Linear scaling is increasingly harder
    - ✓ L and V scaling, field limit 1 V/nm
    - ✓ Oxide scaling faces tunneling effect (ITRS RB wall) high K dielectrics
    - ✓ Polysilicon gate depletion
    - ✓ Threshold mismatch
    - ✓ Subthreshold leakage
- ✓ Technology issue
  - ✓ Nanoscale lithography, EUV and then? (ITRS RB wall)
- ✓ Interconnection, complexity and power issues

Intel : Road Map to 2010





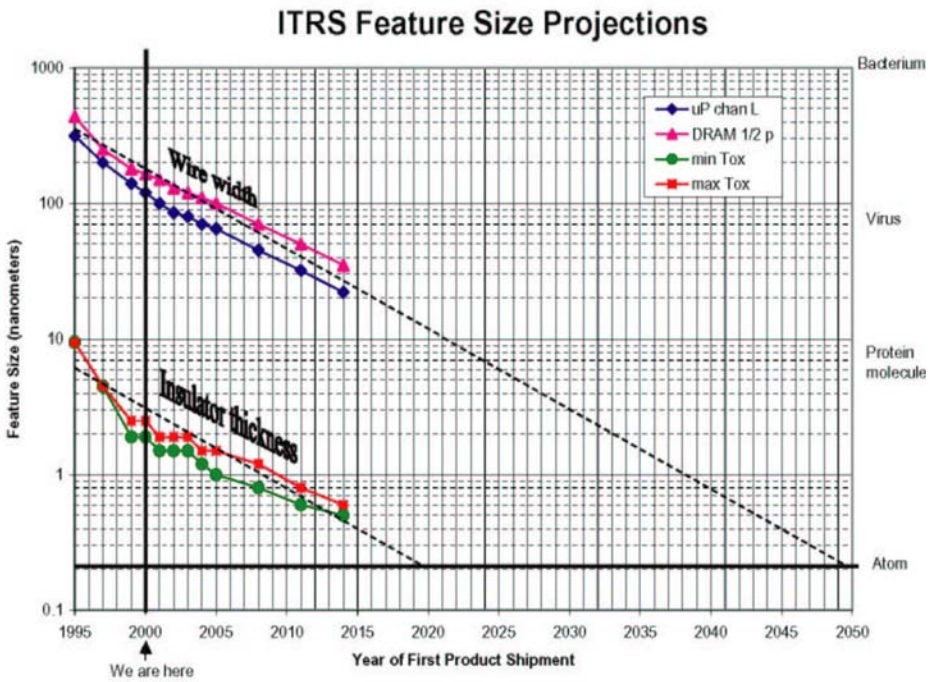


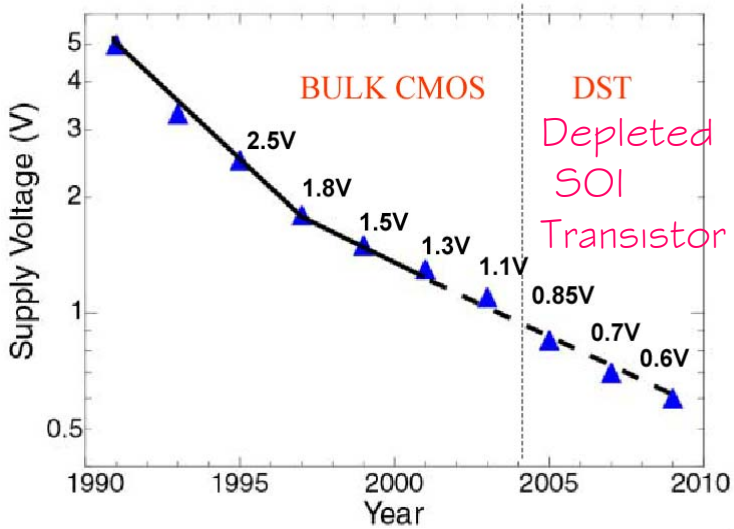
- ✓Itanium, Intel ISCC 2002
- ✓0.18um
- ✓221 millions transistors
- ✓1Ghz clock
- ✓130W, 1.5V

CMOS trends and basic limits

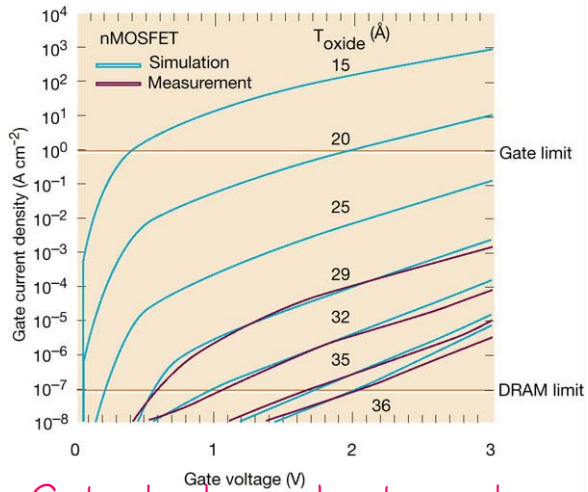
Scaling faces fundamental physical limits

Gate oxide, wire width, voltage supply





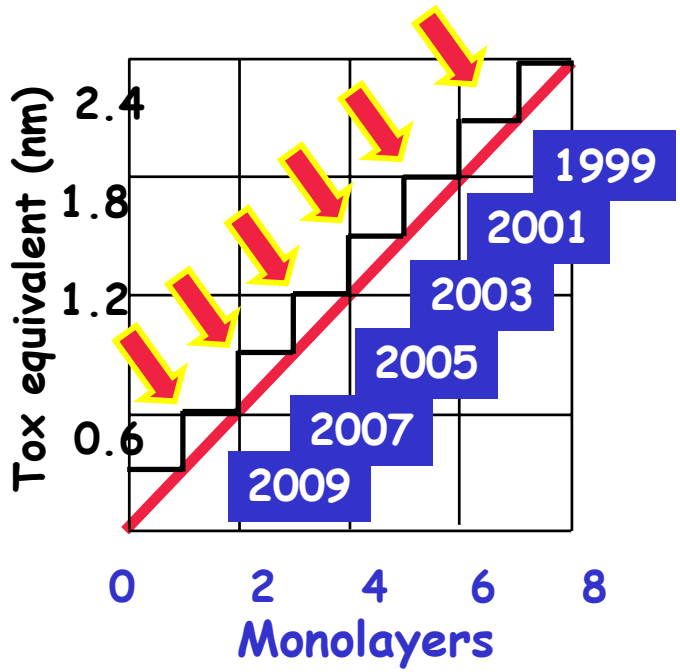
- ✓Oxide thickness
  - ✓Mono molecular layer in 2012
- ✓Wire width
  - ✓Molecule size in 2025



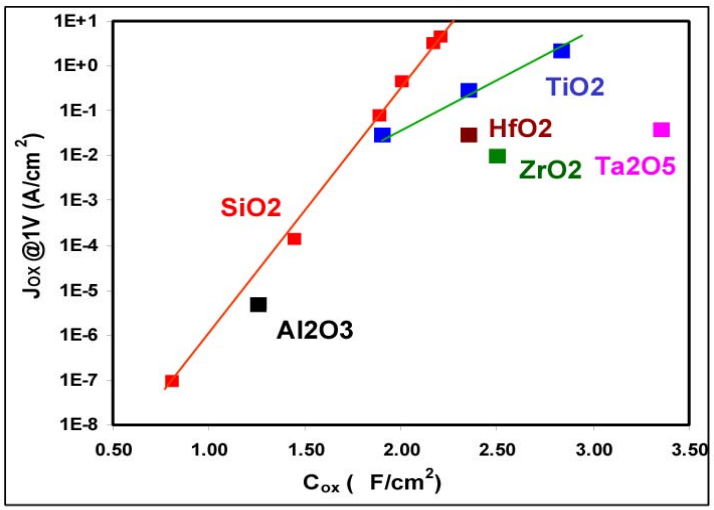
Gate leakage by tunneling

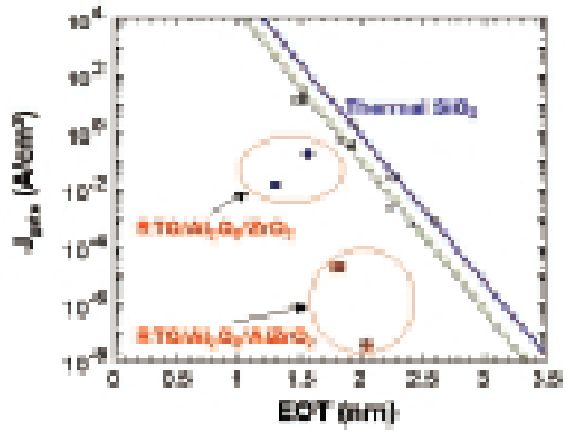
New gate high K dielectrics

- ✓Equivalent Oxide Thicknesses targeted:
  - ✓0.5nm-1.2nm for high-speed
  - ✓1.2nm-1.6nm low power logic
- ✓Aluminum, Hafnium and Zirconium oxides are high K material candidates.
- ✓Recurrent and worrying problem
  - ✓ parasitic regrowth of the SiO2 is a challenging technology issue
- ✓High K oxide reliability and radiation hardness are not well established



Gate Leakage



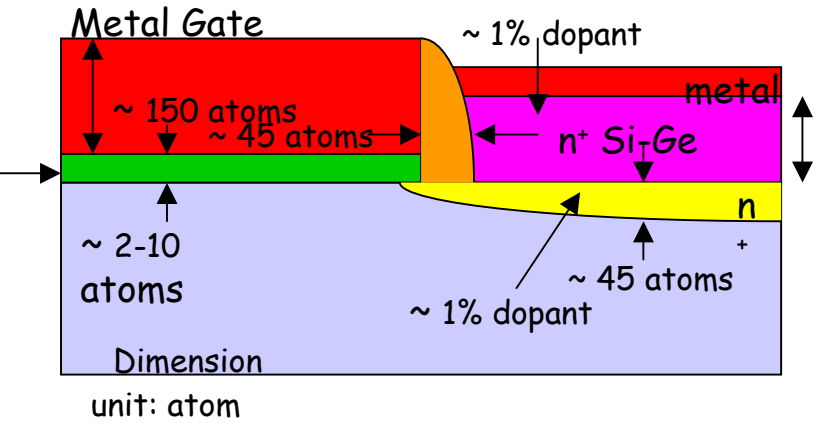


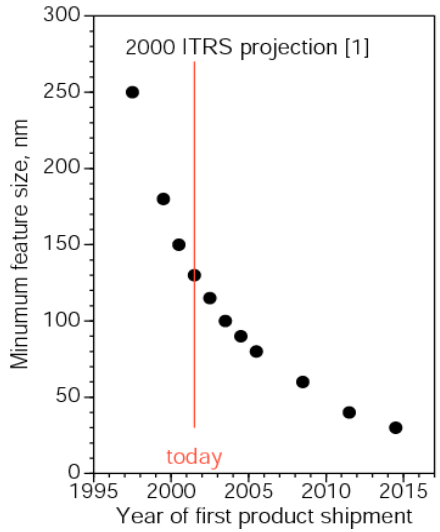
After M. Heyns IMEC

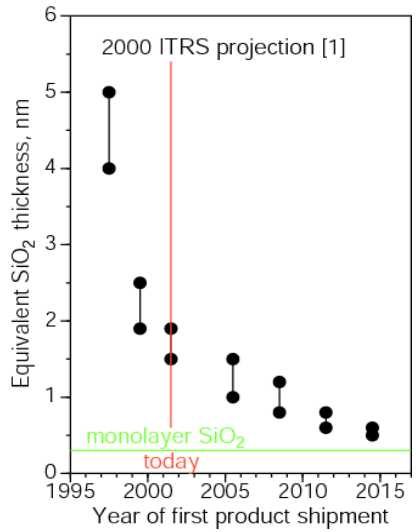
Consequences of extreme CMOS scaling

Beyond 2006

- Traditional MOS geometry will be over
- Scaling should be adapted to quantum effects
- Statistics of dopant distribution
  Large threshold voltage variation
- High K gate mandatory

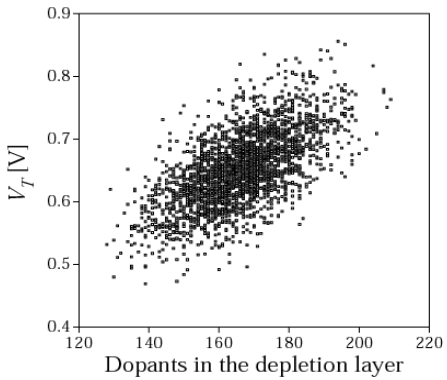


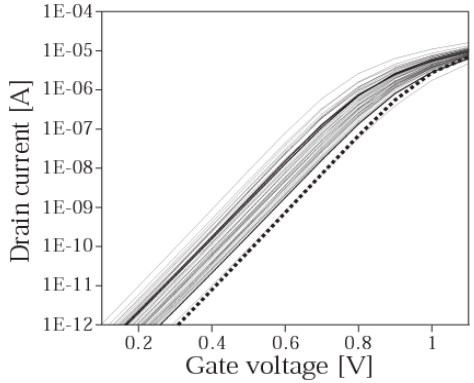




After ITRS 2001 SIA

50nm × 50nm transistors: 'identical ''devices are very different





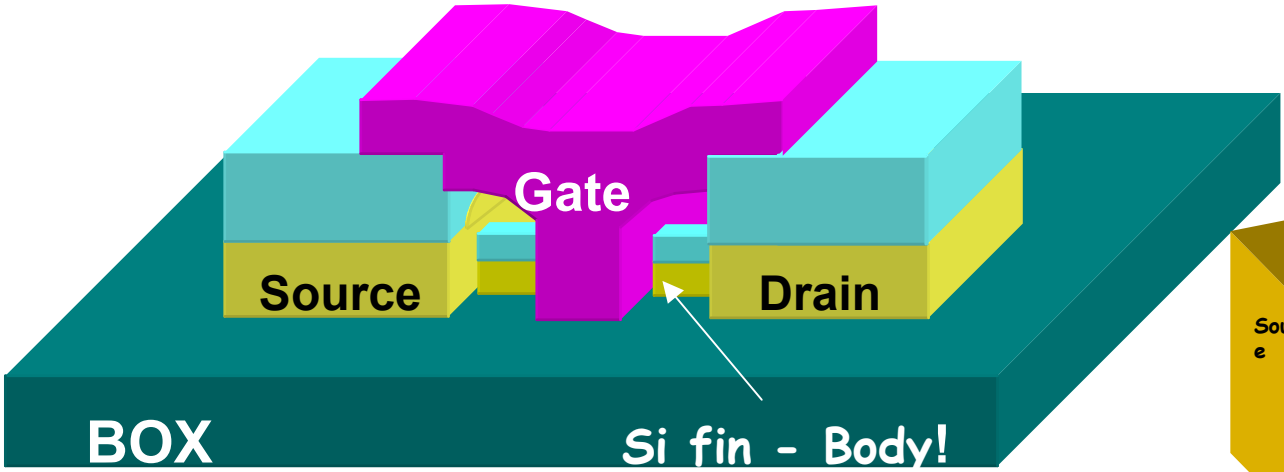
After Dabrowski IHPD-Frankfurt

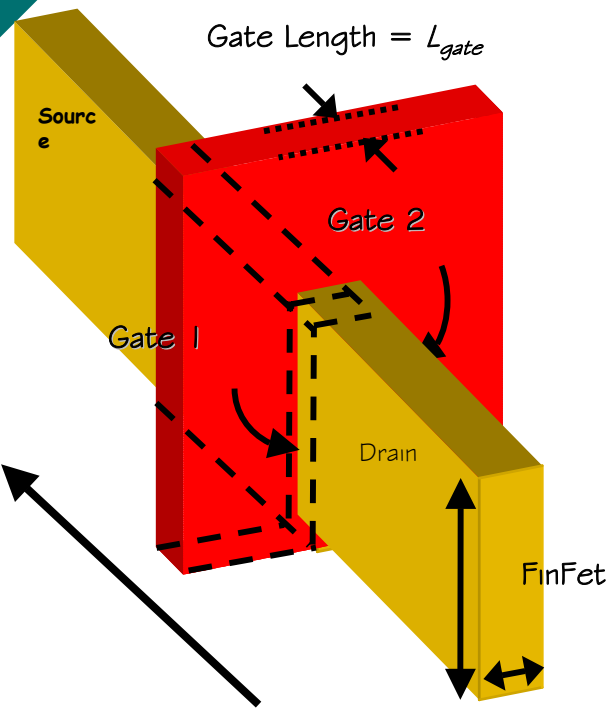
Devices investigated

- Vertical replacement MOSFET
- FINFET elevated source and drain
- Undoped channel, dual metal gate
- Thin film SOI DST

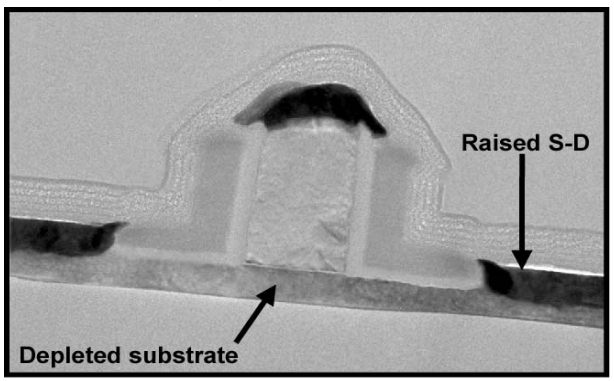
FinFET: FD body thin silicon SOI

- Double-gate structure + thin body on SOI
- Elevated Source/Drain





Intel depleted SOI MOSFET

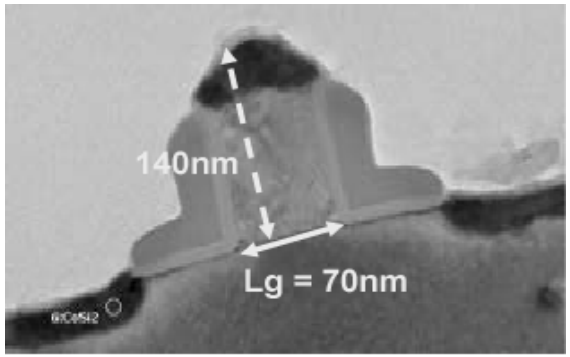


After INTEL

Current flows parallel to wafer surface

After LETI

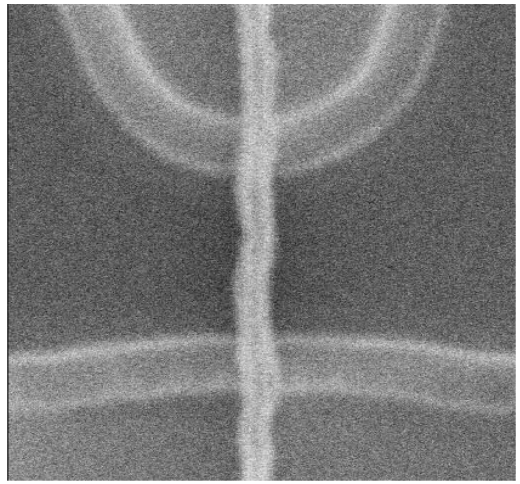
INTEL future technology nodes



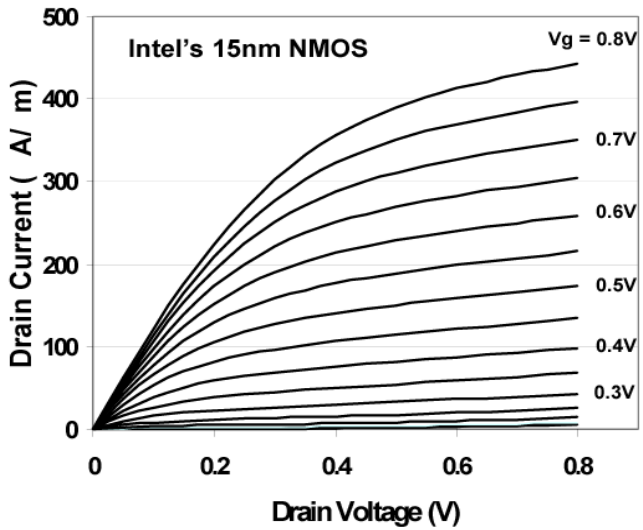
70 nm transistor

70 nm gate length
130nm technology node
In production in INTEL

65nm node

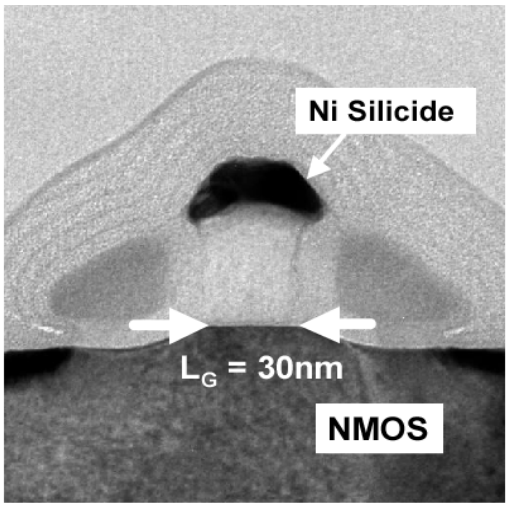


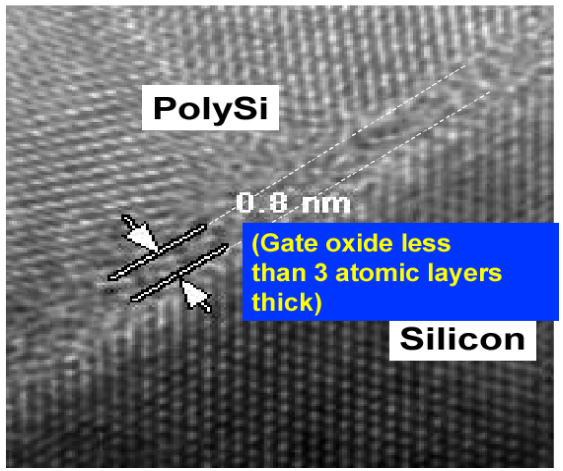
30 nm gate length
65nm technology node



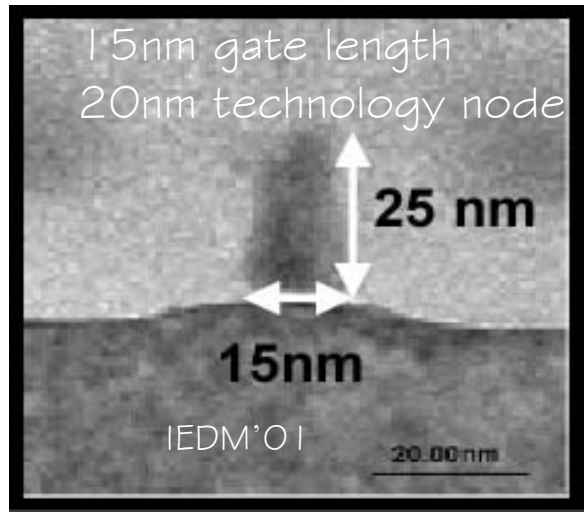
15nm gate length
20nm technology node

Gate Oxides as Thin as Atoms



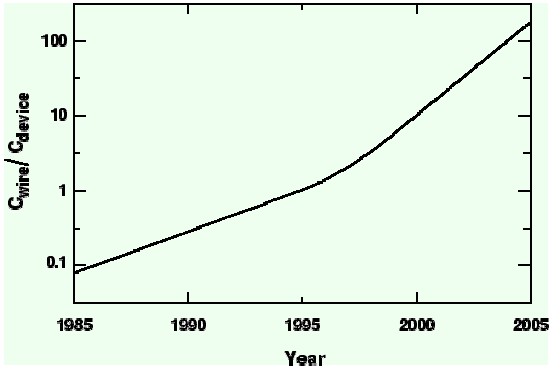


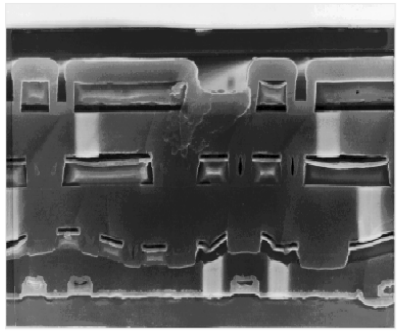
After Intel



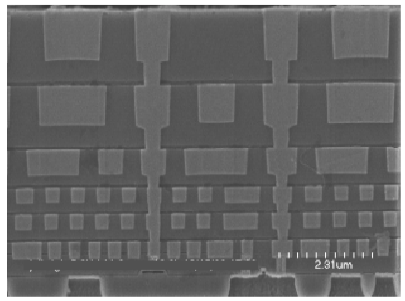
The fault, dear Brutus, lies not in our gates, but in our wires

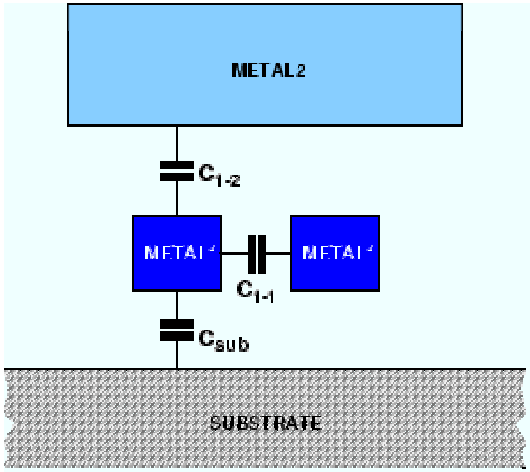
Shakespeare: the fault dear Brutus lies not in our stars, but in ourselves.



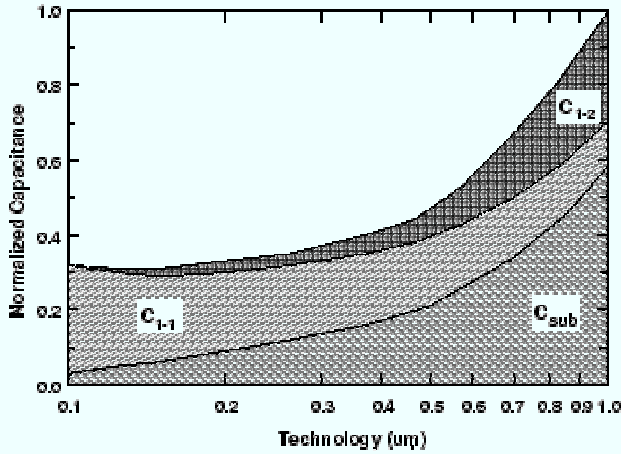


After Intel





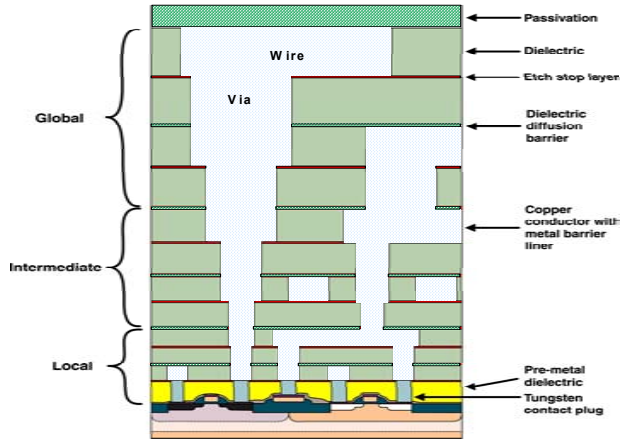
(I)



(II)

After SIA ITRS2001 road map

65nm Node

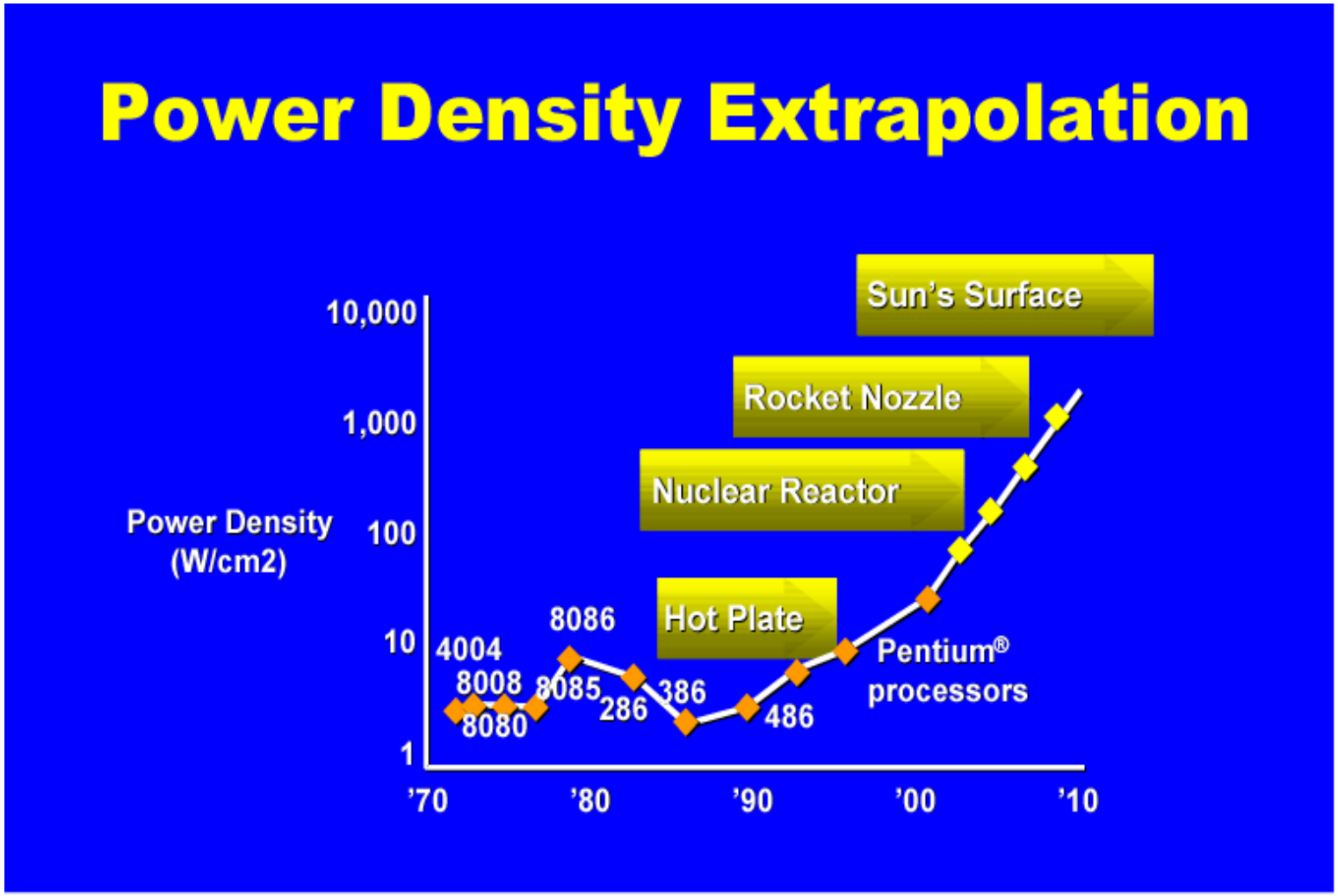


Theoretical limit Energy required to transport a bit irreversibly from device to device in a computational system is $E_t = kT.d.f/c$ (more fundamental than energy now dissipated in a resistive interconnect)
For a maximum information **transport distance of 50 nm**, Feynman's analysis shows that 10^{18} bit transfers per second will require 1 watt of power, 10^9 lower power than CMOS in 2010.

Issues Wire-to-wire coupling
Wire coupling: at 5 Ghz, Z(1 pF)=30Ω!!
Power consumption: 80% in interconnects C_{wire}/C_{device}= 100

Power density trends and limits

Thermodynamic ultimately limits progress of microelectronics

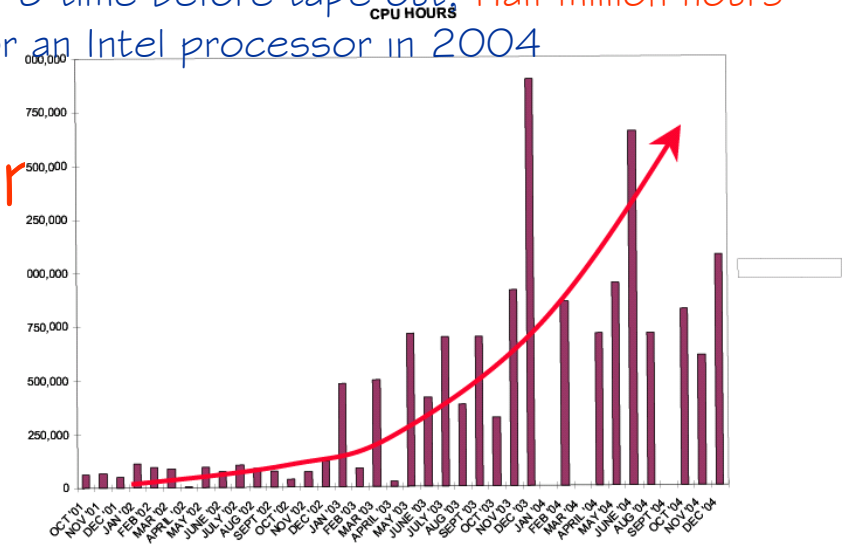


Pat Gelsinger's slide from ISSCC2001 - Intel

Summary of miniaturization issues

- Device limit
  - Quantum effects
  - Short channel effects
- Technological barriers
  - Lithography
  - processing
- Thermodynamic barrier
  - Set by interconnections
- Financial issue
- Complexity issue

CPU time before tape out. Half million hours for an Intel processor in 2004



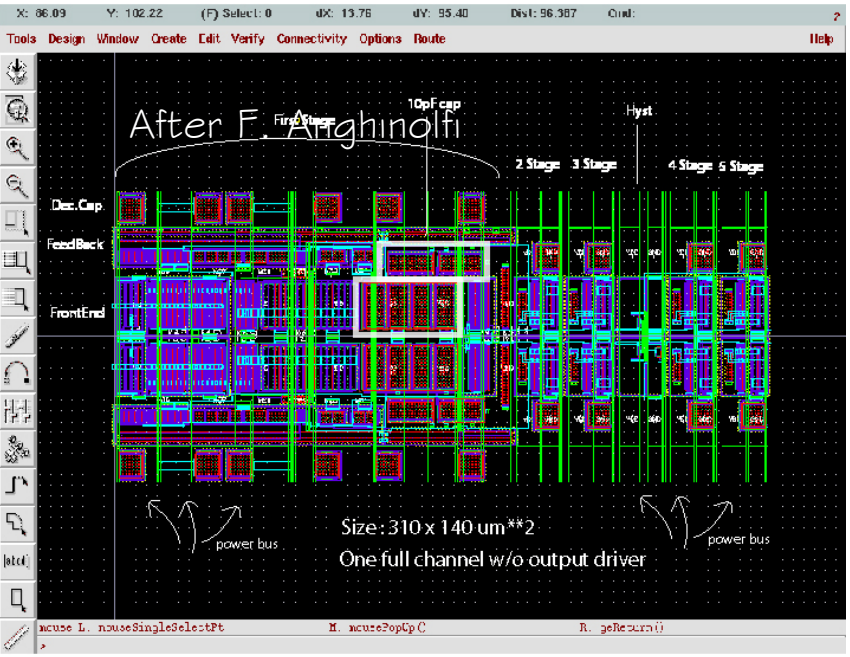
The design of billions transistors chips soon, and trillions transistor chips turns out to be a titan's task

4. Future Trends

Nanoscale CMOS for HEP analog front end

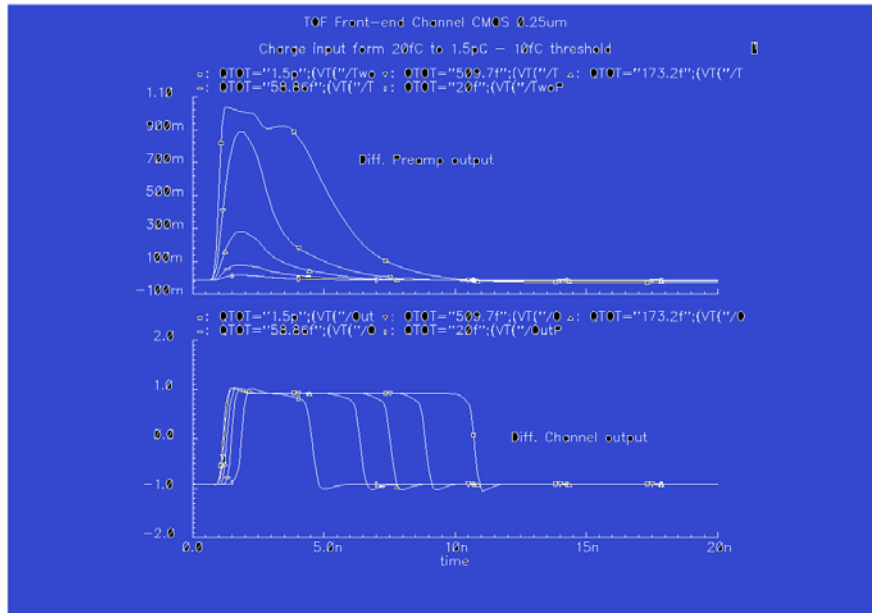
- ✓Ultra-fast electronics
- ✓3D silicon detectors, thin detector
- ✓Monolithic pixel detector
- ✓Few electrons amplification
- ✓Integrated APD's array

Very very fast!



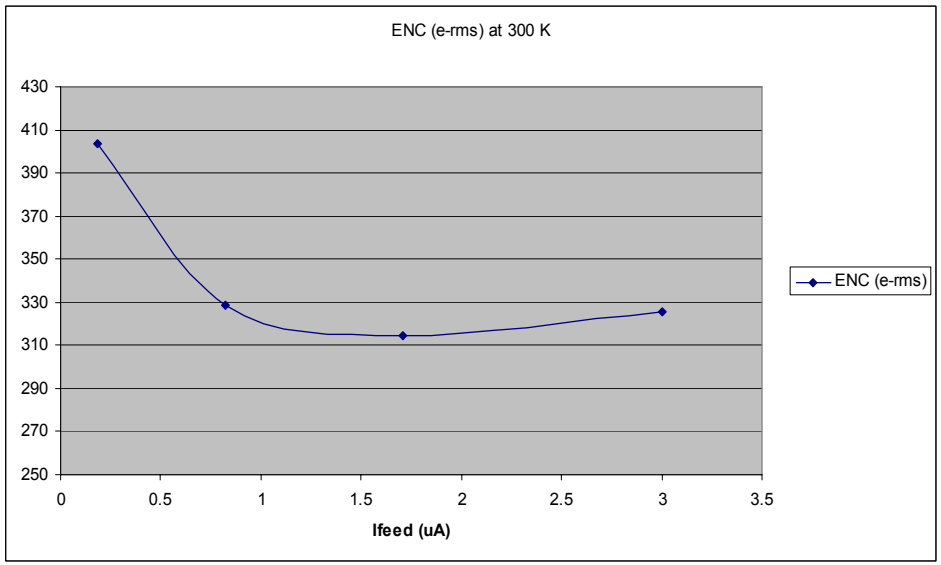
- ✓8-Ch Amplifier-discriminator for ALICE TOF
- ✓Differential IN and OUT
- ✓Tunable input resistance: 50 Ohm
- ✓Power : 20 mW/ch
- ✓Peaking time: 1ns, noise 2500 e- rms @ 10pF
- ✓Walk time without correction: 250ps
- ✓Walk time with correction: 20ps
- ✓Jitter: 10ps rms

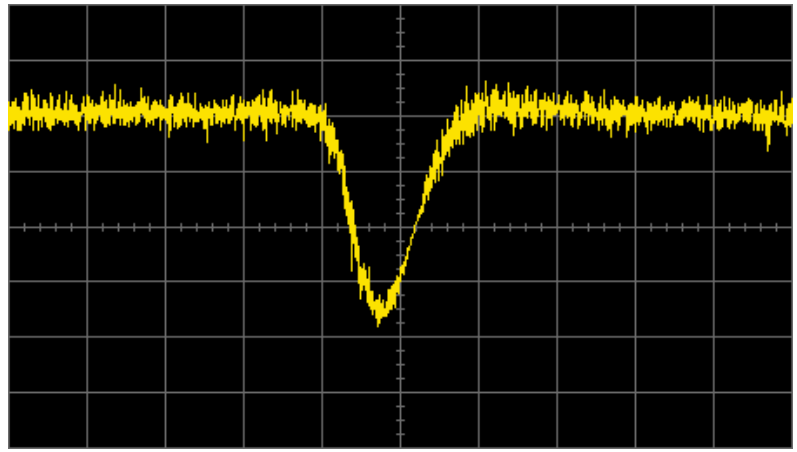
Design based on differential common gate input MOS configuration based on common base circuit of V. Radeka. 0.25 micron CMOS IBM outperforms bipolar design.



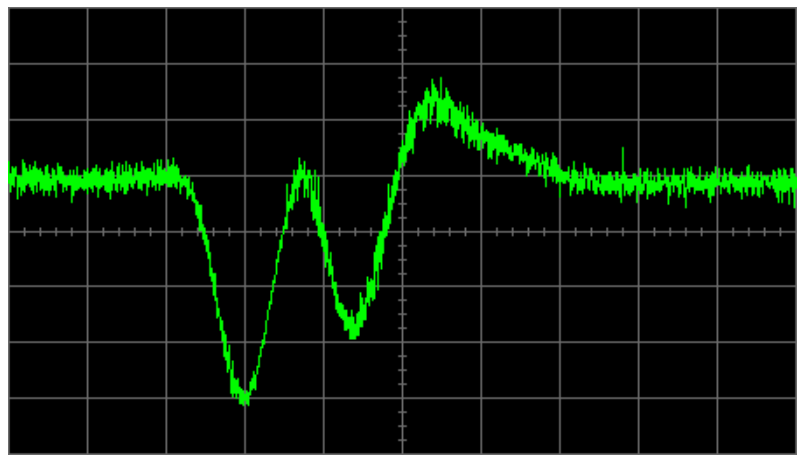
Very fast, low noise and cryogenic

AFP amplifier for the silicon Beamscope of NA60
3.5ns peaking time, 3mW/ch





4fC Time 5ns/cm



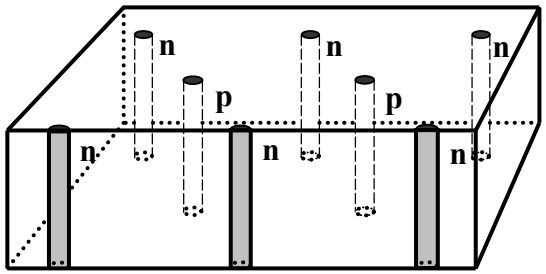
Double pulse resolution 6.5ns

Room temperature and cryogenic
can operate from few K to room temperature
ENC=300 e- rms at Cdet=5pF

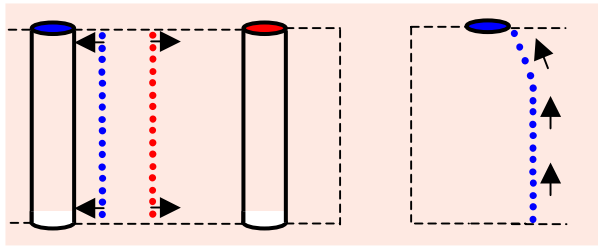
G. Anelli et al. Schloss Elmau conference 2002

3D Si-detector

Simplified Cross Section of Part of Sensor

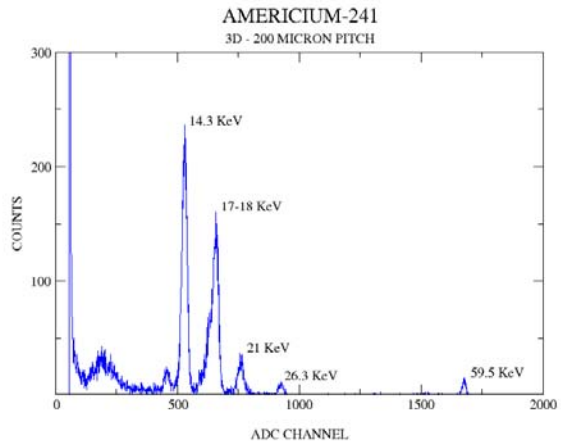


Nucl. Instr. Meth. A 395 (1997) 328, Trans. Nucl. Sci. 46 (1999) 1224; 48 (2001) 189,1629,2405.

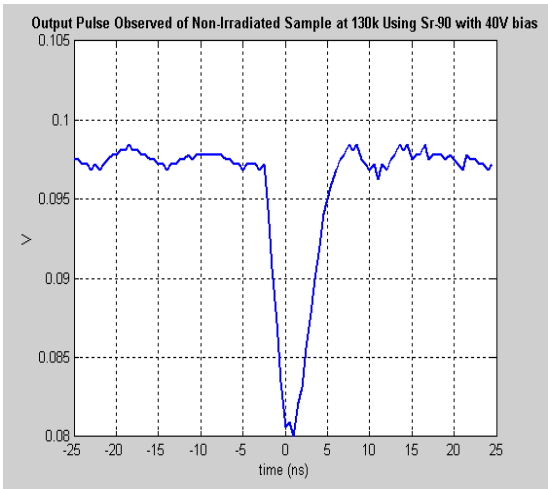


3D Silicon detector Principle
S. Parker

Am 241 Spectrum Recorded With 3D Sensor



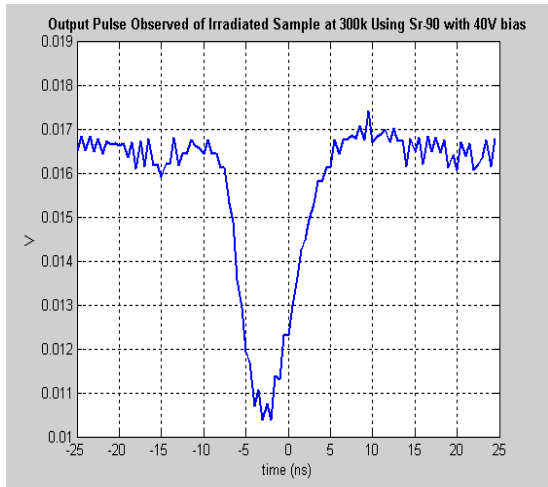
Non Irradiated at 130K



Fall Time= 1.5ns (±0.25ns)

Results of radiation hardness and detector speed are promising for LHC detector upgrade and LHC forward detector

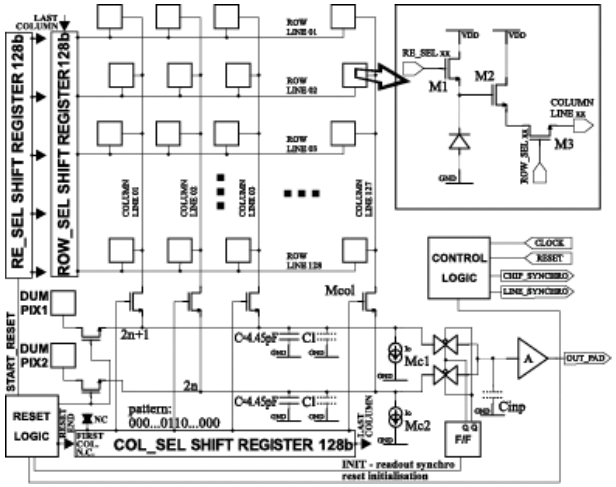
1×10^{15} p/cm^2 at 300K

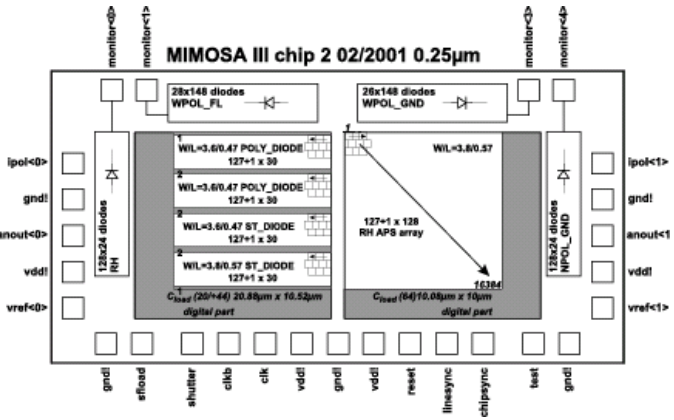


Fall Time = 3.5ns (±0.25ns)

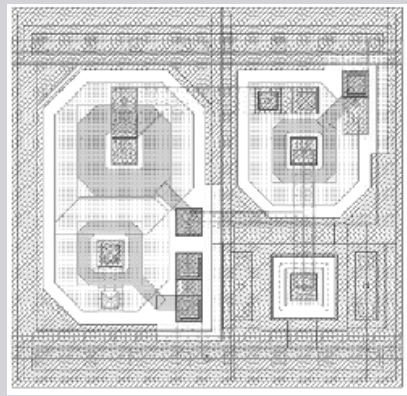
Monolithic Pixel sensor

MAPS-MIMOSA III LEPSI-CERN (2000) in 0.25 CMOS IBM

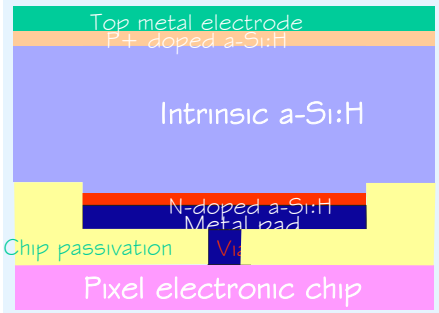


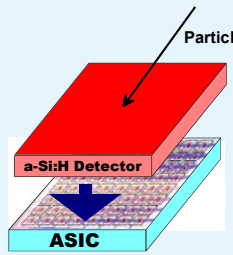


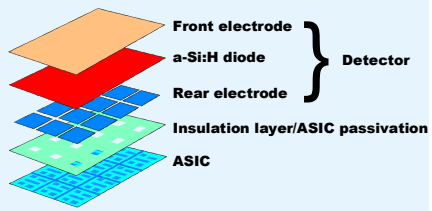
- ✓Pixel size 8µm x 8µm
- ✓Passive integrating readout
- ✓Processing time(CDS) ≈ 1 ms
- ✓Charge sensing node ≈10fF
- ✓Leakage current≈ 2 fA
- ✓ENC= 6 e- rms



Above IC technology



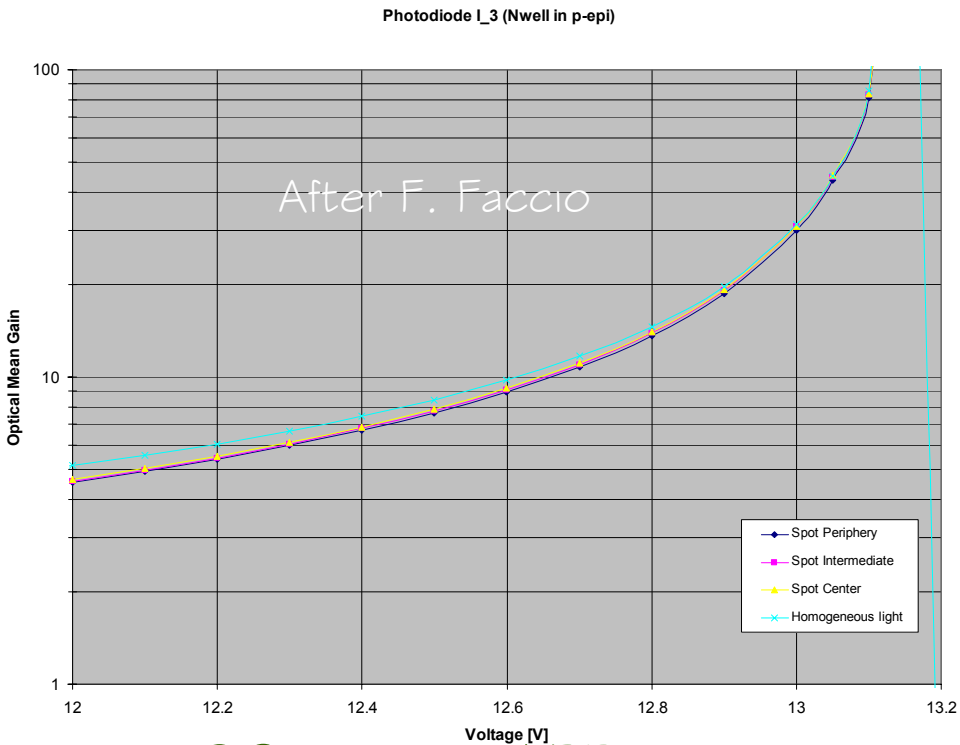




0.25 CMOS compatible APD

Integration of APD in CMOS IS THE TECHNOLOGY
Potential high resolution solid state PM
Single or fewer photons counting integrated device

Preliminary results of test structures in IBM 0.25micron



90 micron APD diameter

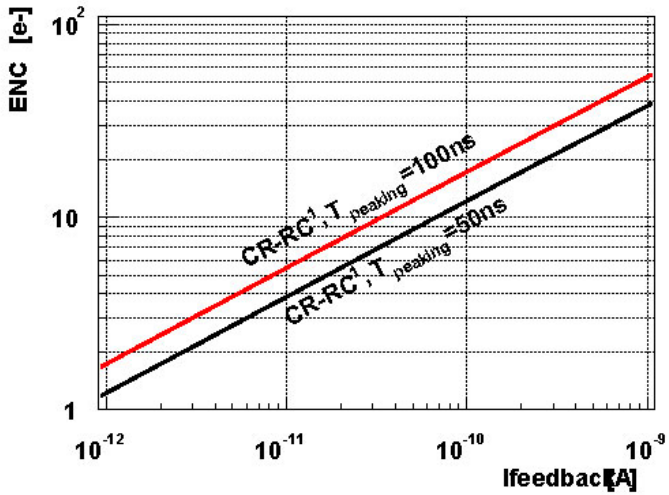
Gain Characteristics
Up to X100
Avalanche voltage: 13V
Good gain uniformity

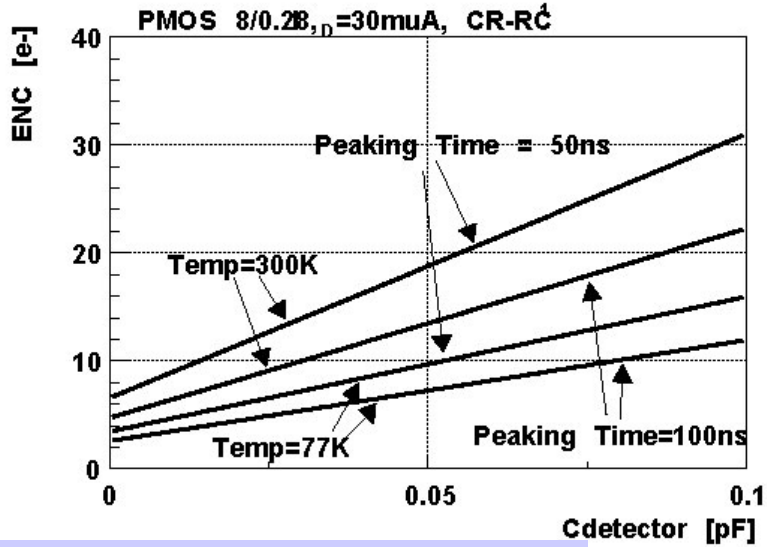
Unpublished work 2002 CERN, EPFL

Noise limit in pixel readout

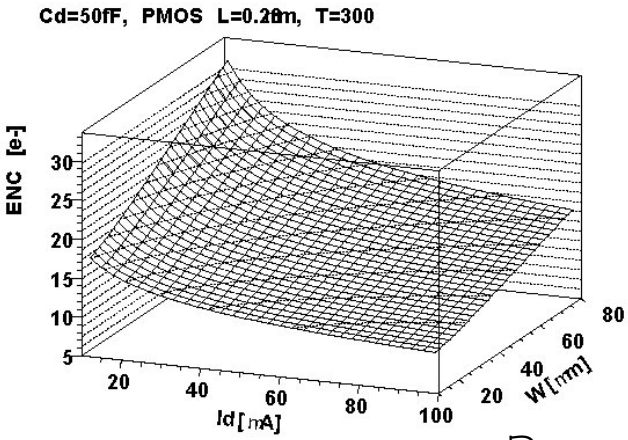
Towards single electron circuits: L=0.28 μm Id/W≈ 1 μA/ μm

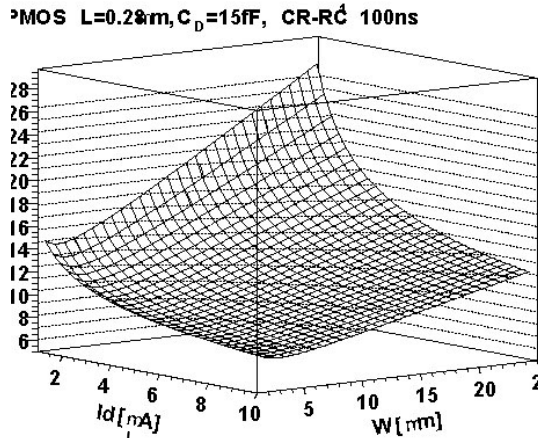
Parallel and series noise calculation done by J. Kaplon for 0.25 CMOS IBM

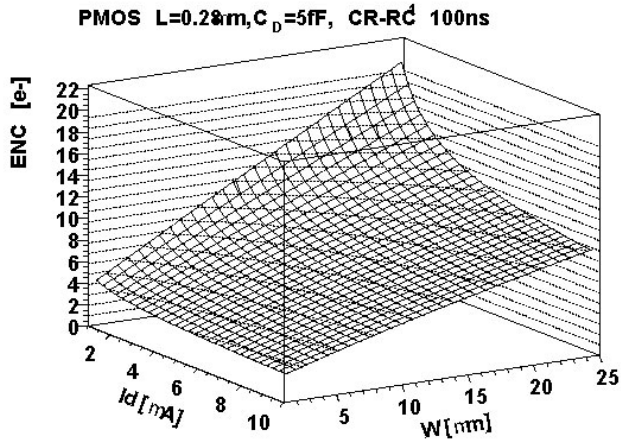




Pixel miniaturization trends 50fF(≈ 50μm) to 5fF(≈ 5μm)







Drain current in microamps

5.Beyond nanoscale CMOS

✓Nanoelectronics

✓Nanotechnology has often been defined as the science of fabricating, characterizing and using structures from the atomic scale up to around 100 nanometers

✓This definition embraces many fields

- ✓from electronics and physics, through nanobiotechnology, chemistry and on to mechanical engineering.

✓Below the 100 nanometers limit?

- ✓Quantum effects
  - ✓Electron tunneling
  - ✓Quantum confinement
  - ✓Single electron effects (Colomb Blockade)

Nanoelectronics: devices

- ✓ Single Electron Devices
  - SET
  - Hybrid CMOS-SET
  - Single electron Memory
- ✓ Quantum devices
  - Quantum dot
  - Quantum wire
  - CNT devices
  - Quantum computing
- ✓ Spintronics
- ✓ Molecular devices
- ✓ DNA devices
- ✓ Nano-mechanical devices
- ✓ .....ad infinitum

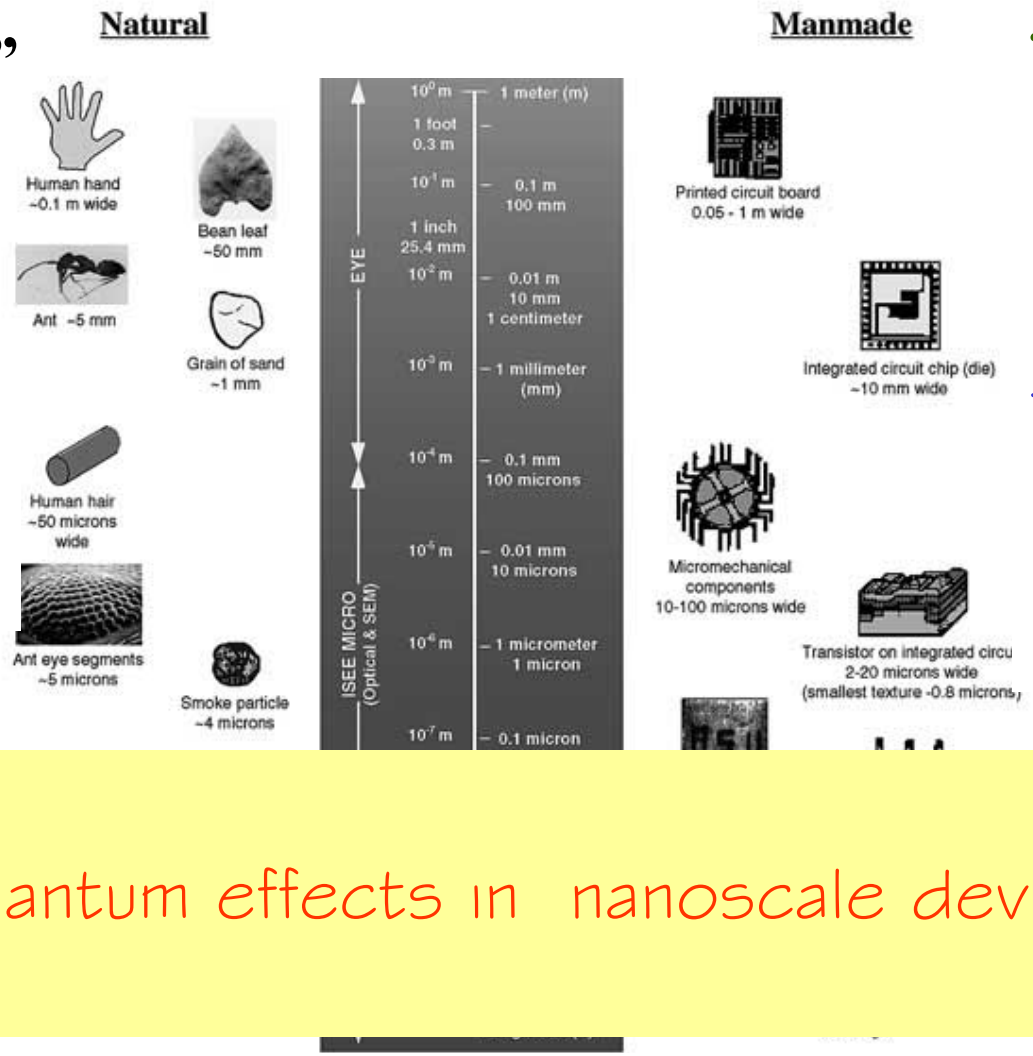
"The paradigm of the microelectronics industry is not the way forward; we can only miniaturize two more orders of magnitude before we reach the atomic level, and it will cost an absolute fortune. Do we really need pentabit devices? Or would we be better off pursuing higher complexity, instead of smaller transistors?"
IBM Zurich Nobel laureate Heinrich Rohrer (AFM)

Dimensional scaling top-down, bottom-up

Down scaling breaking and quantum effects

Nature
"technology"

After MIT condensed matter group



Manmade
Technology

Bottom-up
Self
organization

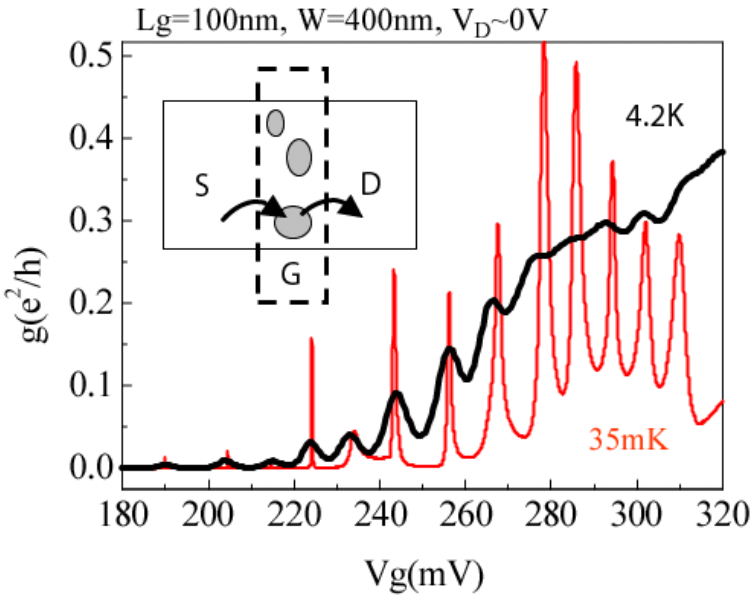
Top – Down
design
based
on Specs

Quantum effects in nanoscale devices

There is plenty of room at the bottom" Richard Feynman

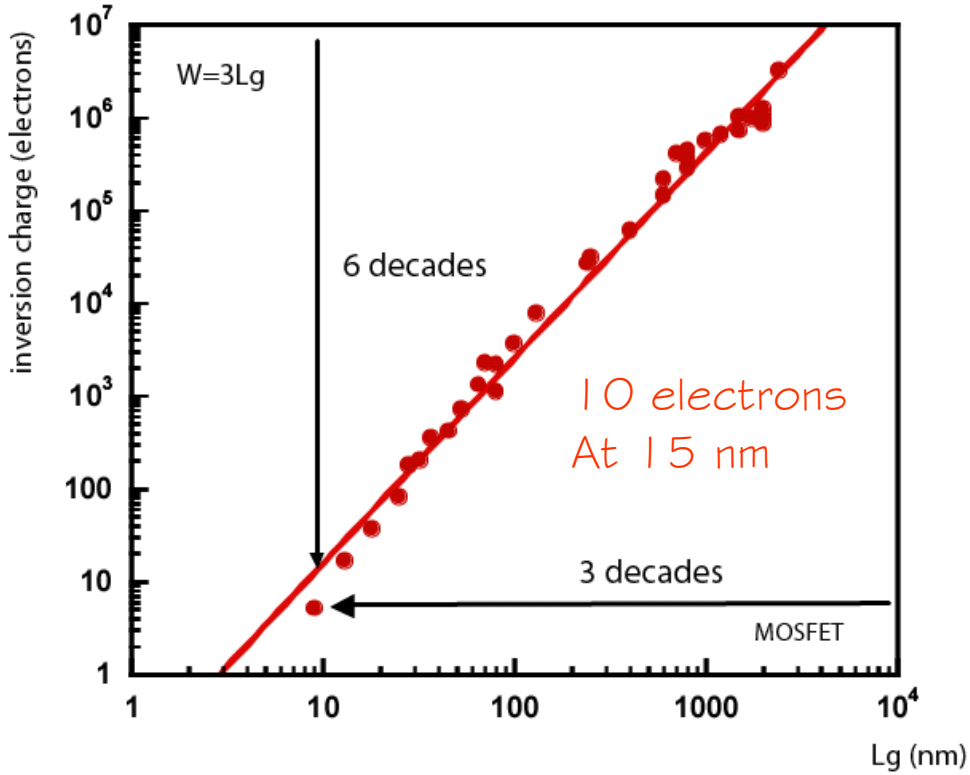
MOSFET device fundamental limits

- ✓ **Colomb Blockade**
  - ✓ Quantum confinement in the channel caused drain current oscillations
  - ✓ Discrete doping center caused Colomb blockade in channel



M. Specht, CEA/DRFMC
IEDM 1999

Channel charge f(Lg)



After J. Gauthier LETI

Nanoscale devices

Mesoscopic device

✓ Crossover regime between classic physics and quantum physics

✓ Fills the gap between the atomic and micrometer scales, where quantum mechanical effects come into play

Molecular device

✓Quantum devices

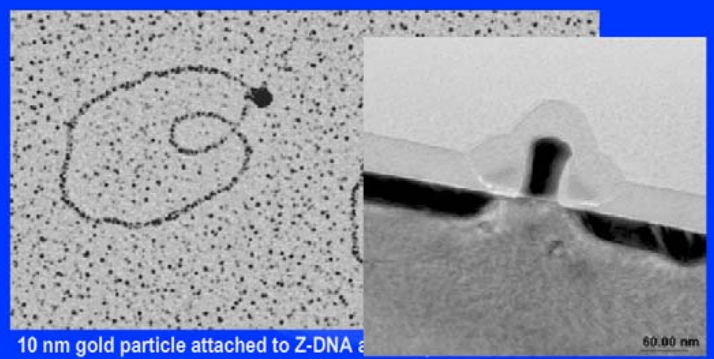
✓Individual electrons observed

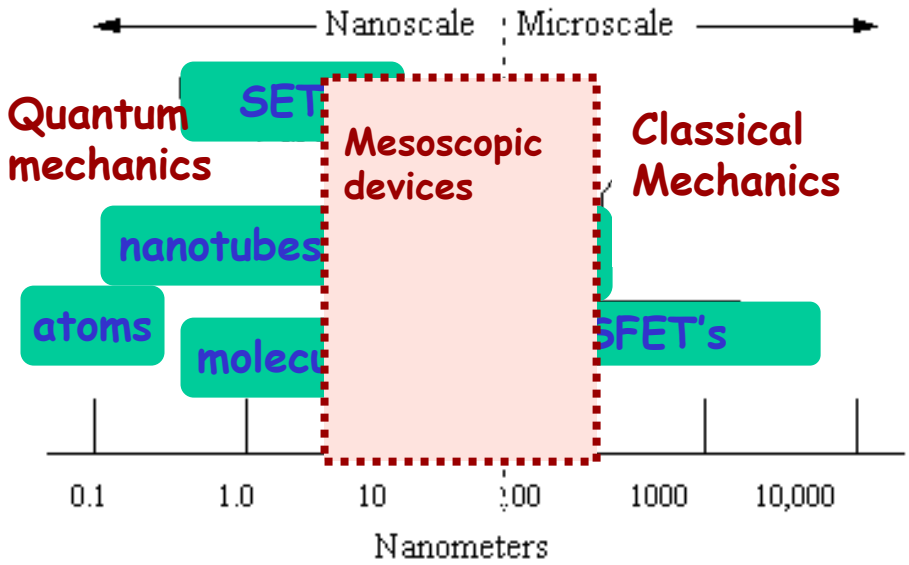
✓size of mesoscopic device comparable to the spread of electron.

✓ Nature of electrons is strongly resolved, wavelength nature of electron becomes important.

✓Complete space and energy quantization

DNA and 30nm MOSFET





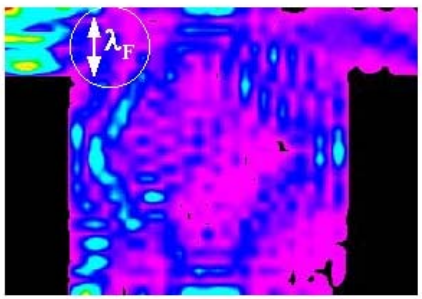
Quantum confinement in quantum dots

Classical point charge, valid for macroscopic size

$\lambda_F \approx 1nm \text{ to } 50nm$

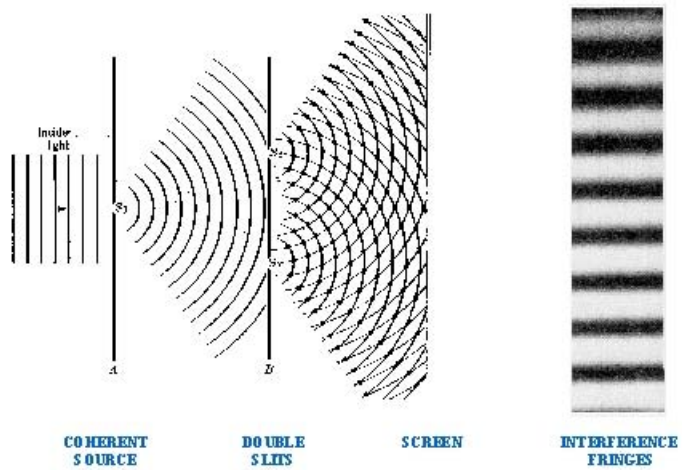
$$\lambda_F = \frac{2\pi}{k_F} = \frac{2\pi}{\sqrt{\frac{2mE_F}{h^2}}} \propto T$$

Quantum Dots
Electron wavelength



Interference in Classical Wave Systems

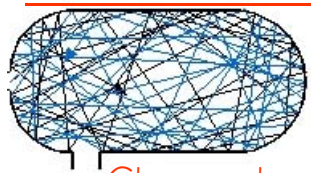
Model from optics



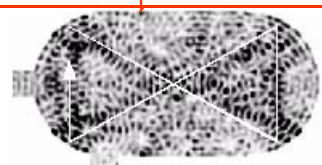
Why wave interference plays a role in mesoscopic devices? Because phase coherence of electron wavefunction is stable at nanoscopic scale.

✓Example of electron wave function in a 100nm quantum dot, Fermi length in the range of the quantum dot size.

Electron transport in quantum dots

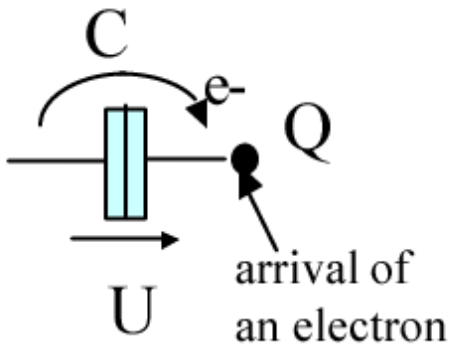


Classical model

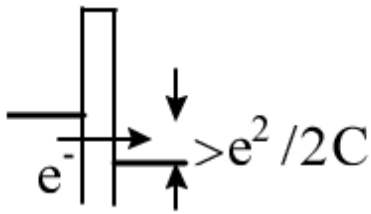


Quantum wave model

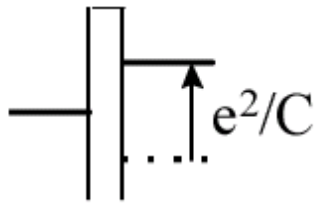
Tunneling & Colomb Blockade



tunneling junction



before tunneling



after tunneling

The free energy of the system cannot increase spontaneously

$$\Delta F = \frac{1}{2}\frac{(Q-e)^2}{C} - \frac{1}{2}\frac{Q^2}{C}$$

$$= \frac{e^2}{2C} - \frac{Qe}{C} \leq 0$$

Drop of electrostatic energy:

$$\Delta W = e\left(-\frac{e}{2C} + U\right) \geq 0$$

$\Rightarrow$ threshold for the arrival of an electron: U > e/2C

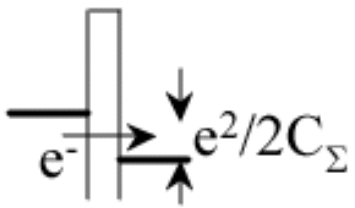
After J. Gauthier LETI

Colomb Blockade

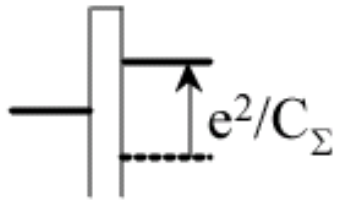
- thermal energy: $kT << E_C = \frac{e^2}{2C_\Sigma}$

$Ec = 10kT @ 300K \rightarrow C_\Sigma = 0.3aF \rightarrow$ nanometer size

Arrival of one electron on a tunneling junction



Before tunneling



After tunneling

- quantum localization:

(of the electron wavefunction in the island)

quantum fluctuations $\Delta E << \frac{e^2}{2C_\Sigma}$

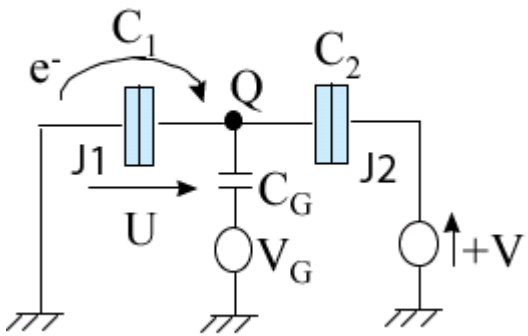
$\Delta E \geq \frac{\hbar}{\Delta t} = \frac{\hbar}{R_T C_\Sigma}$

$\Rightarrow R_T >> \frac{1}{p}\frac{h}{e^2} \approx 8k\Omega \approx R_Q$

After J. Gauthier LETI

Single electron transistor - SET

Condition for the arrival of an e⁻ through J1:

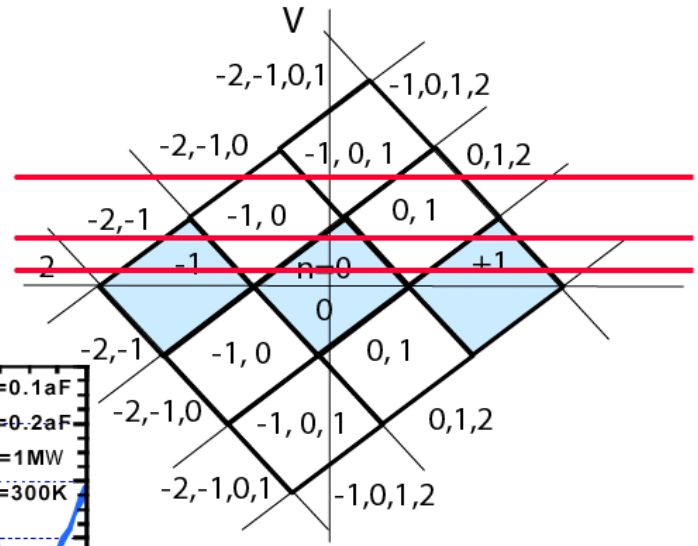


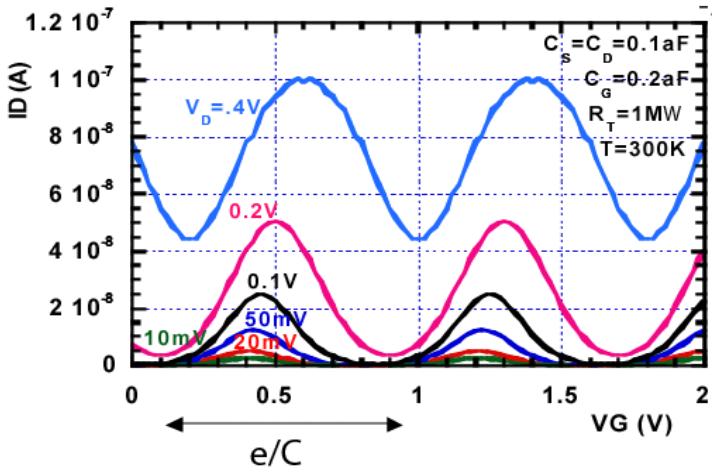
$$U > \frac{e}{2C_\Sigma}$$

$$U = \frac{1}{C_\Sigma}\left(Q + C_G V_G + C_2 V\right)$$

$$C_\Sigma = C_G + C_1 + C_2$$

- low V_D
  - ✓ periodic ON state
- higher V_D
  - ✓ broadening of ON state

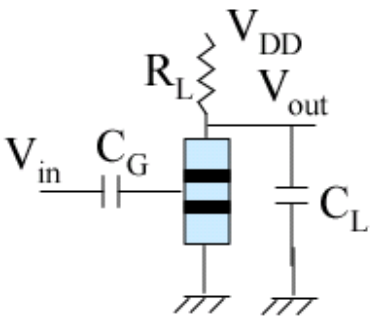




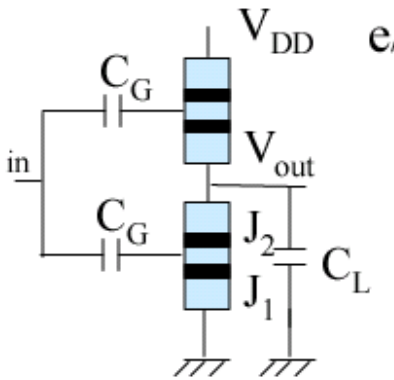
Coulomb Blockade Oscillations (CBO)

After J. Gauthier LETI

SET-based logic SET

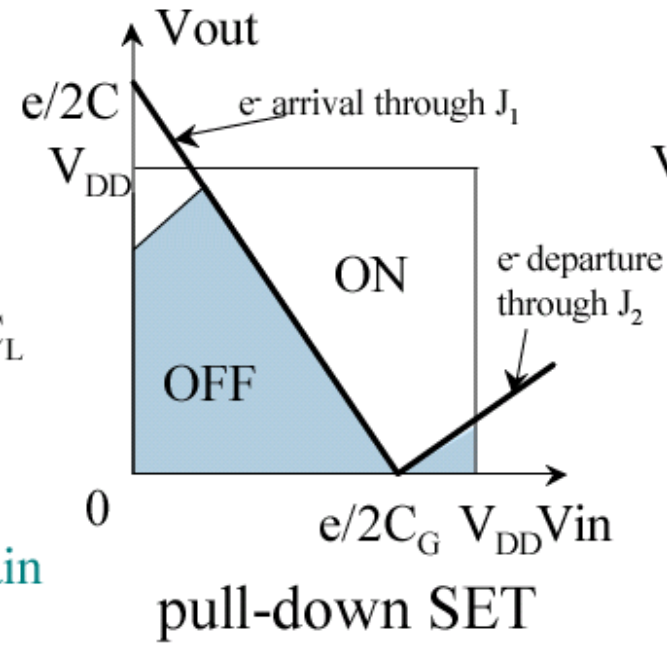


- Resistance-load Capacitively coupled
- Complementary Capacitively coupled

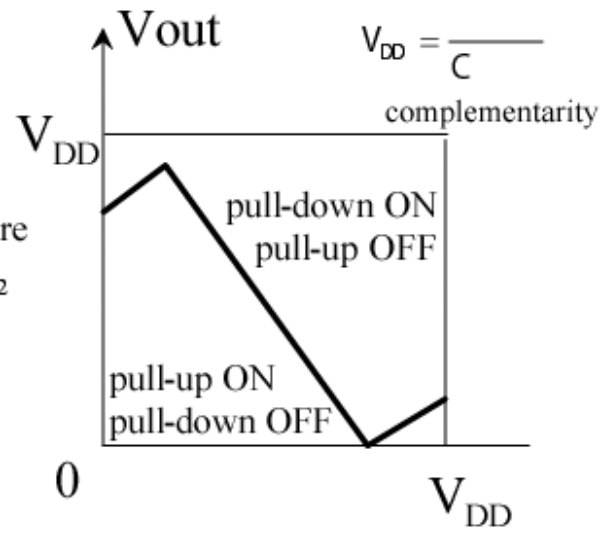


$=C_2=C$

$_G$~2 to 3 C for gain



pull-down SET



inverter

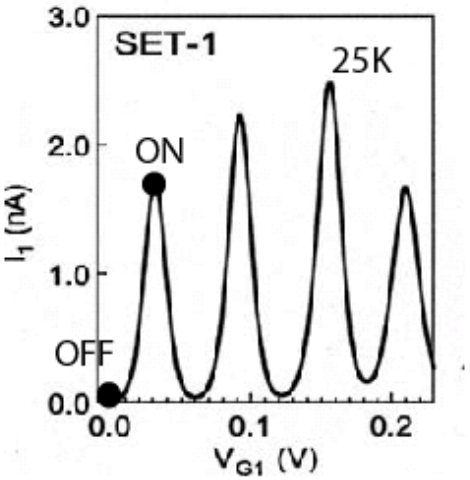
-one type of SET (complementarity of action adjusted by V

-constraint on V_{DD} → lower flexibility than CMOS

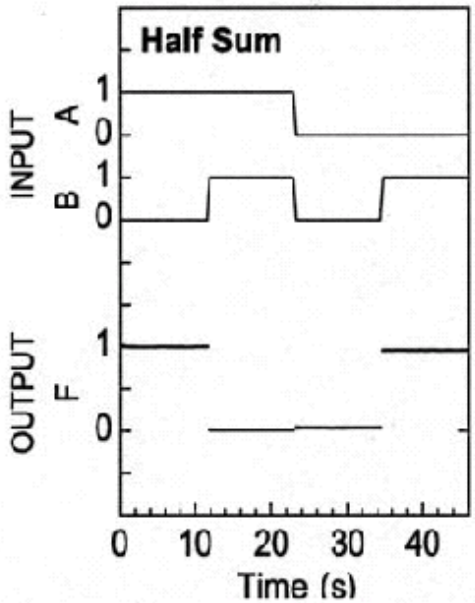
After J. Gauthier LETI

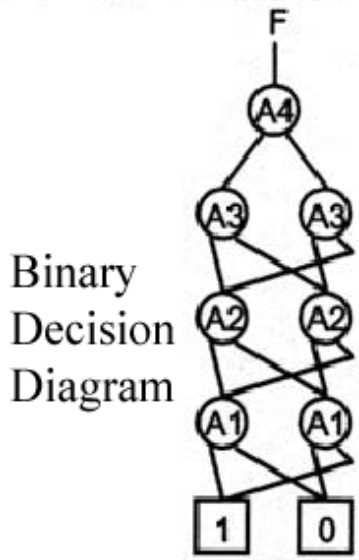
Single Pass Electron Transistor(NTT)

- Pass transistor logic
  - ✓ Twin SET
- ultralow-power
  - ✓ Logic swing DV_G=24mV
  - ✓ Messenger V=4mV
- Need of CMOS amplifier
  - ✓ Hybrid logic
- demonstration half sum and carry out adder

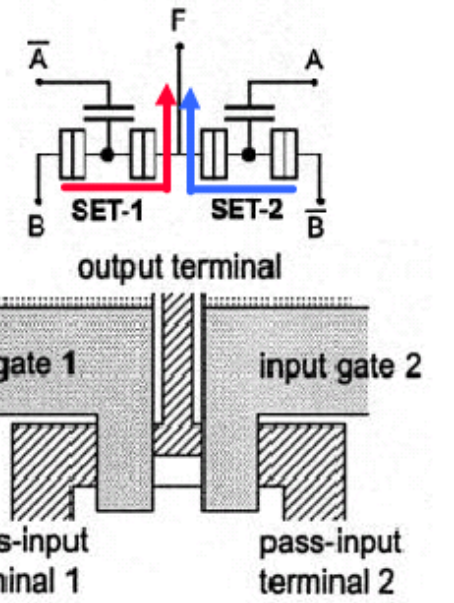


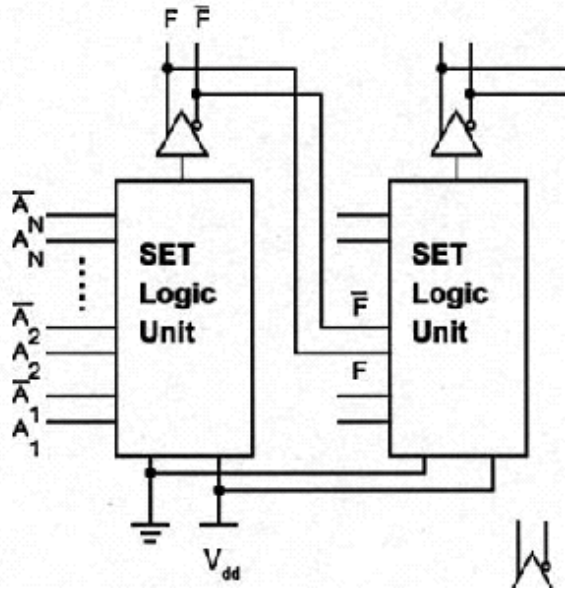
Y. Ono, NTT, IEDM 2000, pp. 297





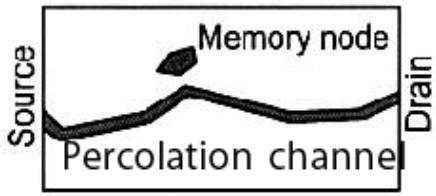
Binary Decision Diagram

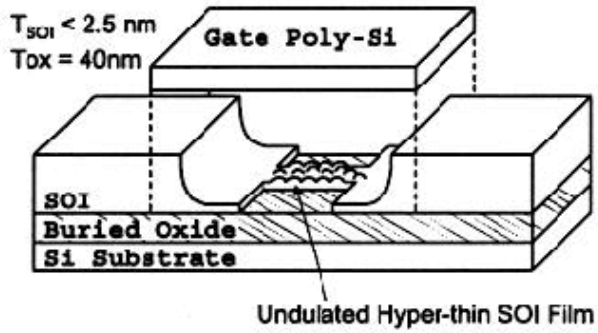


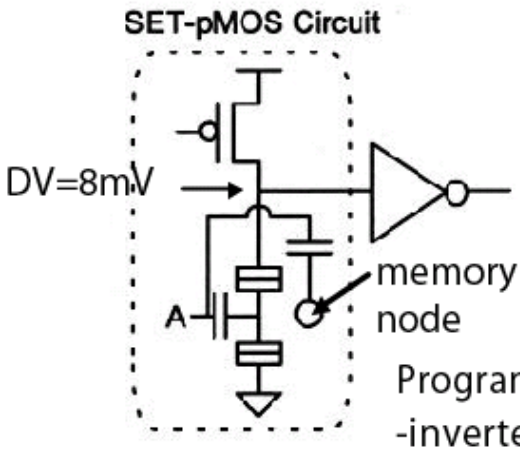


Multifunctional SET logic (Toshiba)

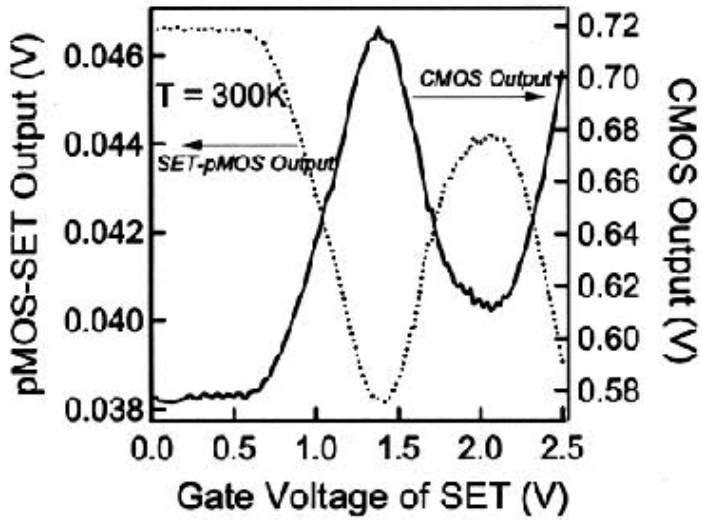
- Memory effect in undulated hyper-thin SOI (t_{Si} <2.5nm)
- Tuning the phase of CBO
  - ✓ Program the operation of SET
- Demonstration of inverter / non inverter gate at 300K
- Need of CMOS buffer
  - ✓ Hybrid logic







Programmable gate:
-inverter
-non inverter

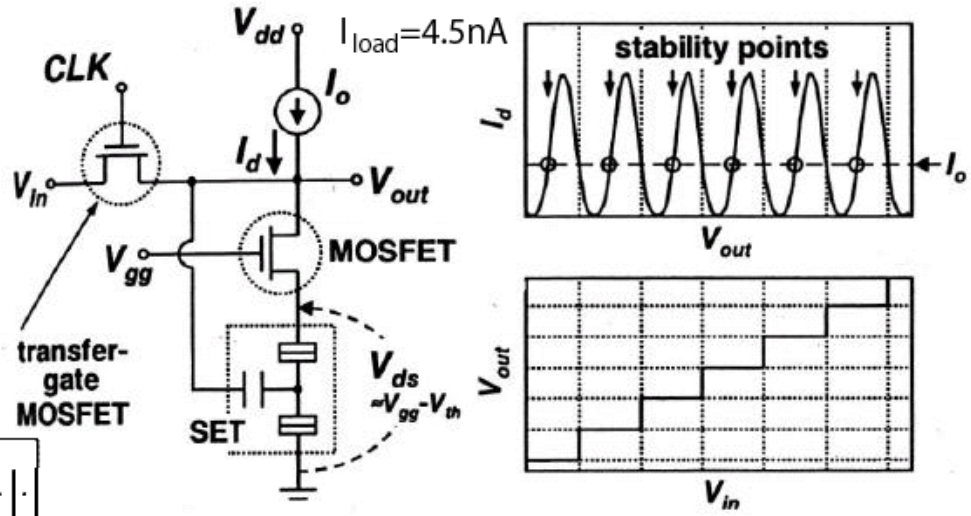


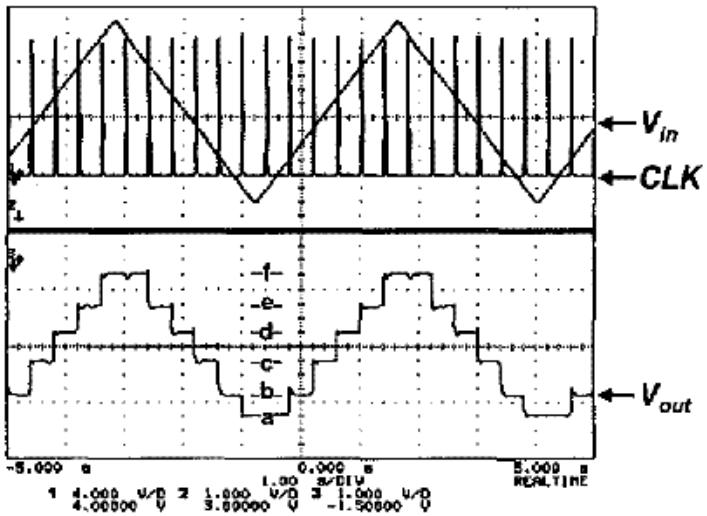
K. Uchida, IEDM 2000, pp.863

ADC converter (NTT)

Taking advantage of the periodicity of current oscillations

- Demonstration of basic functions for an ADC
- Hybrid SET-CMOS
- Fabrication by PADOX process
- quantizer operation at 25K
- Application to multiple-valued logic

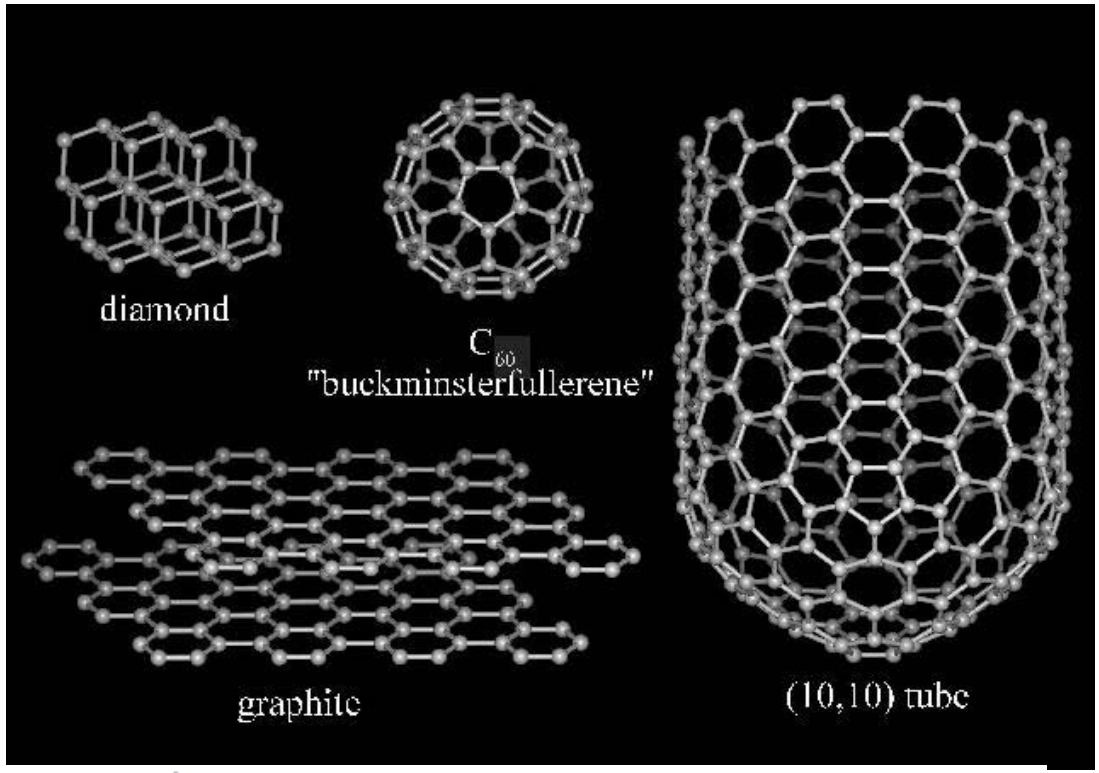




H. Inokawa, IEDM 2001, pp.147

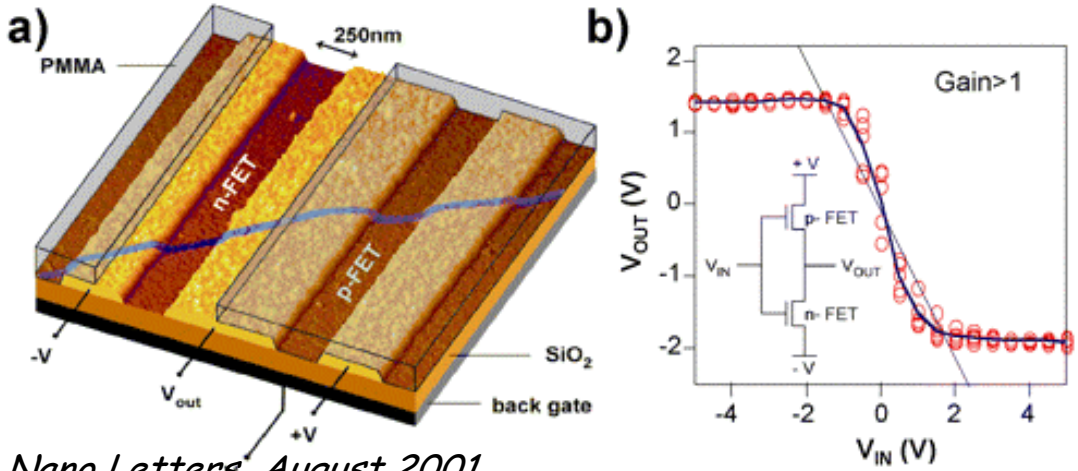
Carbon nanotube (CNT)

- **What it is?**
  - It is stronger than steel
  - it is far sharper than a pin
  - it shoots electrons
  - it draws away heat
  - it is the thinnest wire
  - it can be the tiniest electronic device



a) A single nanotube bundle is positioned over the gold electrodes to produce two p-type CNTFETs in series.

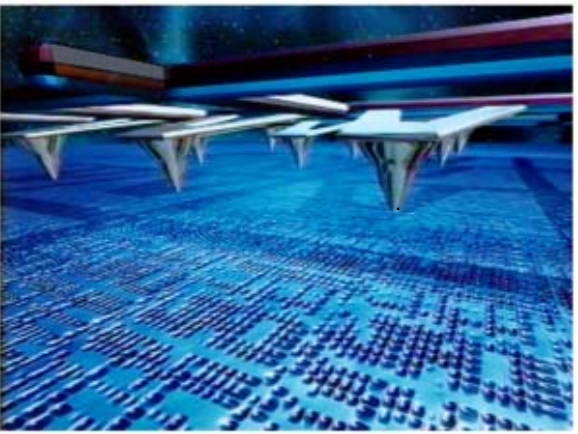
b) Characteristics of the resulting CNT voltage inverter.

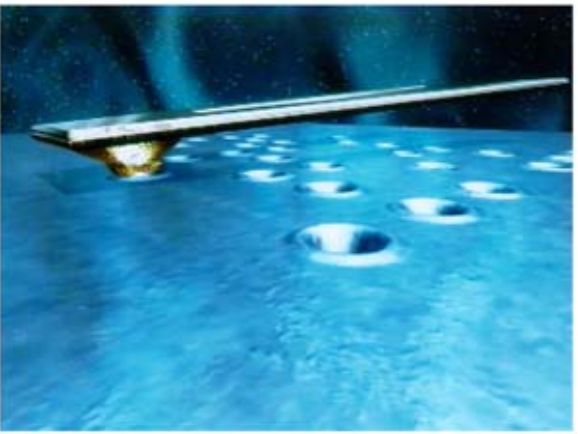


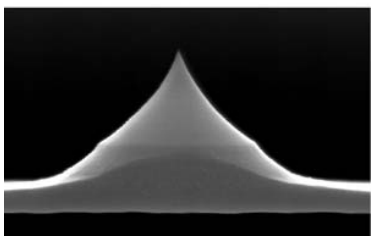
AFM image After IBM. Published in Nano Letters, August 2001

Nanotechnology could surprise us!

A good old memory concept revisited: nano-mechanical memory

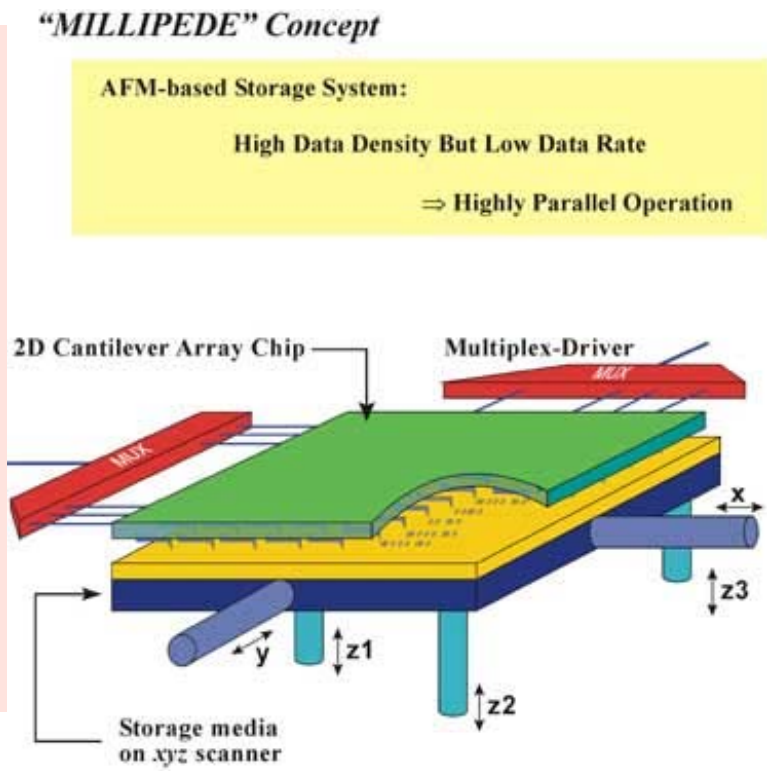






This technique is capable of achieving data densities in the hundreds of Gb/in² range, well beyond the expected limits for magnetic recording (60–70 Gb/in²).

June 11, 2002 Zurich Using an innovative nanotechnology, IBM Zurich has demonstrated a data storage density of one trillion bits per square inch — 20 times higher than the densest magnetic storage available today.



http://www.research.ibm.com/resources/news/20020611_millipede.shtml

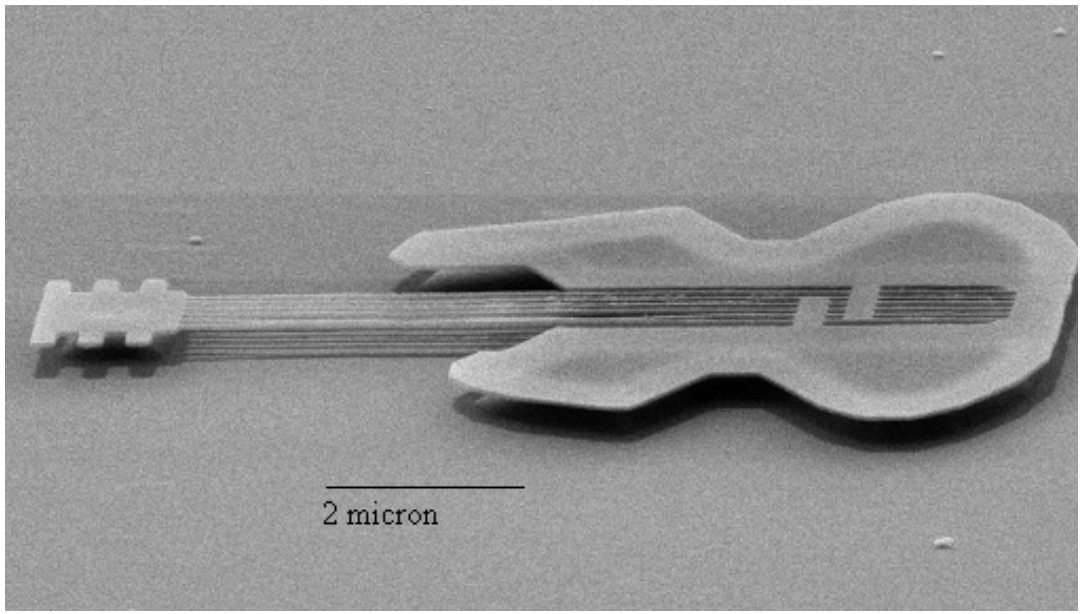
SUMMARY

CMOS will continue its scaling until 2015-2020

- **HEP community must continue to monitor new technology opportunities for sensor and ULSI circuit developments**
  - Get ready for the next technology generations: 130nm, 90nm and then 50nm
  - Understand trends in circuit architecture and radiation hardness of nanoscale CMOS technologies
  - Adapt analog circuit design techniques to very low voltage supplies
  - Investigate new design opportunity, i.e few electron circuits,
- **Sensor integration**
  - Room temperature monolithic single visible photon sensor array
  - Low cost macropixel detector for future tracking systems
  - Ultra-thin micron scale monolithic silicon pixel
- **Have a look on nanoelectronics**
  - Challenging and risky to use nano devices, would require enormous effort for uncertain result.

CONCLUSION on Nanoelectronics

Nice instruments
But not yet ready to play music!



From nothing to somethingness

the tinier your "something" gets, the more "nothing" will turn out to be "something".