Trends in microelectronics and nanoelectronics and their impact on HEP instrumentation

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Abstract

Microelectronics is the key technology that has made possible the construction of the electronics instrumentation for the LHC experiments. For example, deep sub micron CMOS technology has enabled the challenging design requirements for the tracker systems, such as radiation tolerance, low noise figure, low power readout circuits, and very high channel density to be successfully achieved. The semiconductor industry forecasts that CMOS technology will continue its current pace of miniaturization towards the nanoscale CMOS regime until 2015 and probably 2020. Beyond this timescale it is thought that nanoelectronics will play an important role. The paper discusses trends in microelectronics and nanoelectronics and their future impact on particle physics instrumentation.

I. Introduction

Since the transistor was invented some 50 years ago[1], the trend in electronics has been to create ever-smaller products using fewer chips of greater complexity implemented in microelectronics technologies that allow smaller and smaller feature sizes. The development of integrated circuits and storage devices has continued to progress at an exponential rate; as shown in Fig.1 at present it takes two or three years for each successive halving of minimum feature size. The miniaturization of CMOS integrated circuits follows the well-known Moore's Law [1], which is a result of the semiconductor industry's ability to implement linear down scaling of CMOS technology [2]. This is achieved by linear scaling of geometry, voltage and doping levels as shown in Fig.2.

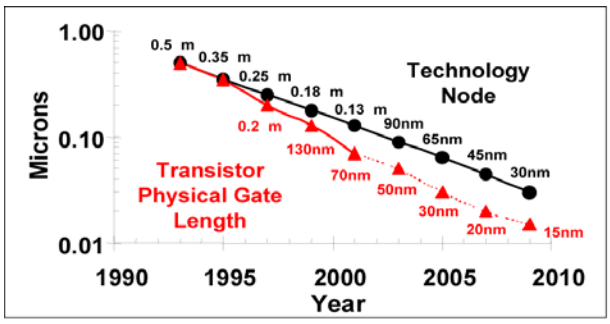

Figure 1 Forecast of the evolution of the CMOS technology nodes (gate length) as described in the ITRS roadmap. Cycle time has been recently updated by SIA to 3 years and not 2 years as used in this graph. Source: SIA,2001 ref [11].

Following the introduction of the organisation of Multi-Wafer-Projects at the beginning of the eighties, the development of ASICs in the high-energy physics community deeply impacted the way HEP electronics instrumentation is conceived, and opened new avenues for the development of silicon strip and silicon pixel detectors in the LEP experiments. ASICs now play a vital role in all LHC experiments. In particular in the front-end electronics for tracking systems, for which channel density, chip compactness together with a carefully optimised design for minimum noise and minimum power are essential.

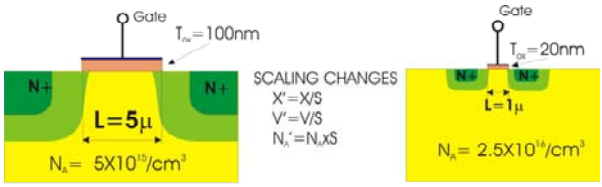

Figure 2 Scaling rules of the MOS transistor have been the foundation of more than 30 years of successful miniaturization of CMOS technology.

The need for radiation hardness in LHC experiments has also been fulfilled by the development of specialized ASICs in radiation hardened technology [3,4] and the development of a radiation tolerant approach developed by RD49 [5,6,7,8]. The radiation tolerant technique is a good example of the impact of the development of microelectronic technology on the field of HEP instrumentation. Thanks to miniaturization of the MOSFET transistor currently available industrial deep submicron CMOS technologies employ thin gate oxides in which, electron tunnelling [9] prevents significant threshold voltage shift of the MOS transistor when exposed to ionising radiation.

II. Microelectronics Trends

Miniaturization of CMOS technology seems to have no end if we observe the trend over the last 30 years. The forecast of the Semiconductor Industry Association (SIA) for the next 15 years is published in the 2001 edition of the

[1] In the June 1952 issue, Scientific American announced the introduction of the junction transistor in the market at a price of $30 per piece.

International Technology Roadmap for Semiconductors 2001 [11] (ITRS 2001). It predicts that CMOS miniaturisation will continue until 2010-2015. After 2015 new technologies based on nanoelectronic devices should be envisaged.

Today 0.25 micron and 0.18 micron CMOS processes form the mainstream industrial production technologies, and 0.13 micron processes are coming on-line as the next industrial generation. As summarized in Table 1, the SIA forecasts that the MOSFET channel length will continue to scale at the same pace and will reach the 22nm technology node in 2016.

Year	1997	1999	2001	2004	2007	2010	2013	2016
Tech node [nm]	250	180	130	90	65	45	32	22
Node cycle time	2	2	2	3	3	3	3	3
DRAM Gbits	0.52			2	4			64
Transistors/chip			276M		1106M			8848M

Table 1. CMOS technology forecast after ITRS 2001. Source, SIA, ref [11].

At nanoscale geometries, below 100nm feature sizes, the short channel effects already observed in previous generations of technology become more difficult to overcome. In addition, fundamental quantum barriers start to play an important role and will deeply affect MOSFET performance.

A. CMOS feature size limit

Extrapolation of current trends of MOSFET miniaturization based on the ITRS projections, as depicted in Fig.3, shows clearly geometrical limits to miniaturization. In 2020 wire width would be comparable to molecular dimensions, and the gate oxide would consist of a single atomic layer.

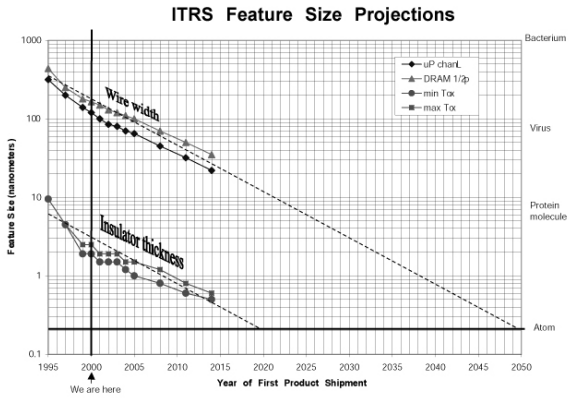

Figure 3 . Long-term projections of the CMOS feature size based on the SIA's roadmap. The forecast shows that inevitably someday CMOS miniaturization must end. Source, SIA, ref [10].

Achieving dimensions of 100nm and below requires adapted lithography techniques. The semiconductor industry currently employs deep ultraviolet light sources (DUV) at 248 nm wavelength for 0.25µm technology. For the 130nm and 90nm technology nodes 193 nm ArF excimer, 157 nm excimer laser and extreme ultraviolet light (EUV) sources are employed. Beyond these technologies, patterning smaller features will not be possible with optical lithography techniques. Several non-optical lithography techniques are being explored by industry such as e-beam lithography and proximity x-ray lithography.

B. Interconnection issues

The wiring required to interconnect transistors must scale at the same rate as transistor scaling to take advantage of improvement in size and speed. The industry is now moving from aluminium to lower resistance copper metallurgy which can decrease both capacitance and resistance. With nanoscale CMOS technologies the wiring density is becoming a severe issue [12].

As shown in Fig.4, for 0.18 µm technology and below, parasitic capacitance between interconnects dominates. One solution already implemented in 0.13 µm technology is the

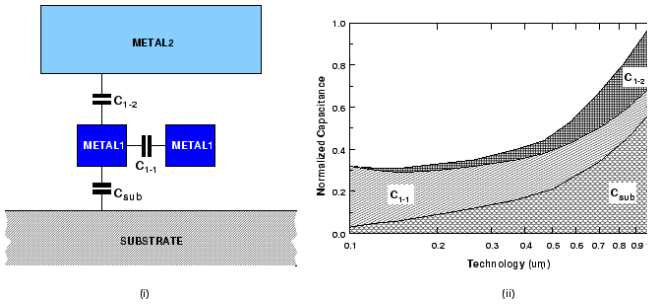

Figure 4. Load capacitance in deep submicron CMOS technology is dominated by electrostatic coupling between interconnections where most of the power is dissipated

use of low-k dielectric isolation between metal layers. However, despite this change in material there is great concern that extremely fine wires with large resistance and capacitance will severely limit performance enhancement for the future generation of CMOS technologies.

C. Scaling limits

Several quantum effects will affect performance of integrated circuits fabricated in sub-100nm CMOS technologies that will emerge in the coming years. Scaling of the gate insulator is a key requirement for continued MOS device scaling. However, aggressive reduction of the gate oxide thickness into the direct tunnelling regime results in an exponential increase of the DC power due to gate leakage current. A high dielectric constant (high-k) gate insulator with a thick physical thickness and a thin equivalent electrical thickness has been the focus of intense research for several years. Several high-K dielectrics are promising such as ZrO_2 and HfO_2. Thermally stable Al_2O_3 MOSFETs have been already demonstrated [13]. However a key concern is the mobility degradation in high-K gate MOSFETs that tend to have a high density of traps.

Several other limitations to scaling such as source-to-drain tunnelling, statistical doping fluctuations in the channel, depletion of the polysilicon gate electrode, sub threshold OFF-channel current, have motivated research into novel MOS device structures for ultra scaled technologies (65 nm and below). These novel MOS devices will introduce major

changes compared to the traditional MOS device [14]. The channel will be formed on an undoped silicon-on-insulator (SOI) substrate; metal gates will replace polysilicon gates [15,16].

D. Power issue and VDD scaling

One of the most important barriers to further CMOS scaling is the power issue. The ITRS forecast for 2013, given in table 1, estimates about 1 billion transistors per cm^2 in logic circuits. For a maximum power dissipation density of the silicon die of $140W/cm^2$, it can be found that the supply voltage should be scaled down to 0.3V, a value lower than the ITRS roadmap forecast. As a result, with no breakthrough in low power design the future performance of integrated circuits, and more specifically microprocessor and complex logic circuits, will be ultimately limited by affordable cooling technology.

Design of analogue circuits in CMOS technology with deeply scaled threshold voltages becomes a tough challenge. This is particularly acute for large dynamic range circuits such as analog-to-digital converters. To avoid this problem, emerging 0.13μm technologies offer MOS device options with higher supply voltages more adapted to analog circuit design.

III. IMPACT OF MICROELECTRONICS ON HEP

The development of ASICs for HEP electronics instrumentation started in the eighties, and has been a key technology for the construction of the silicon microvertex detectors and silicon strip trackers during the LEP era. For the LHC electronics, the development of ASICs is now a pervasive design approach that has been utilized not only for tracker systems [17,18,19] that require highly optimised and dense readout electronic channels, but also for all electronic systems ranging from front end electronics for calorimeter and muon systems to timing and trigger processors.

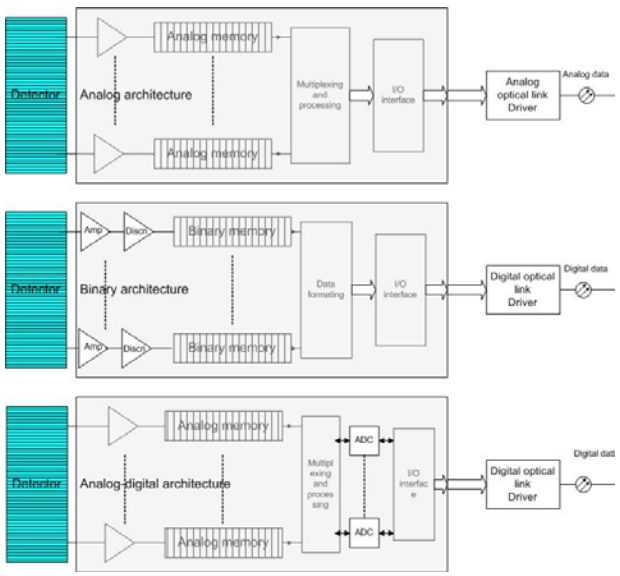

Figure 5. The 3 types of readout architectures of LHC silicon tracker systems as implemented in radiation hardened or radiation tolerant ASICs. Top: analog architecture. Middle: Binary architecture. Bottom: digital architecture.

The development of radiation hardened ASICs for the front end electronics of tracker systems based on silicon strip and pixel sensors has been the focus of intense research and development during the past ten years in preparation for the LHC experiments [20-27]. Two important aspects of the design of LHC tracker systems have been addressed. The first is detector-electronics integration, which is vital to achieve feasible tracker construction with the massive parallelism of readout channels, a maximum of integrated functions on chip for minimum system noise and minimum mass.

The second aspect is the high level of radiation hardness required of the ASIC. This was a new issue in HEP instrumentation and was one of the most challenging aspects of the tracker electronics. Two approaches to design radiation hardened ASICs have been successively developed and used. The first approach is based on the radiation hardened DMILL technology that has been developed by DAPNIA-CEA Saclay and is now in production in ATMEL Nantes-FR [28]. The DMILL technology, although successfully used for several radiation hardened ASICs for the LHC experiments, has shown some limitations for ASICs requiring extreme device density and hardness levels, such as pixel detectors. In addition, the obsolescence of radiation-hardened technology with its niche market and modest feature size was a great concern.

For these reasons, a second approach has been explored by RD49 [29] since 1997 based on the availability of quarter-micron commercial-grade technology. It has been verified that the thin oxides of deep sub micron technologies, below 7nm thickness, exhibit excellent intrinsic radiation hardness with tiny threshold voltage drift and mobility change after radiation exposure up 100 MRads levels. This hardness results from electron tunnelling in thin gate oxides, the same effect that becomes a major obstacle for ultra-thin gate in nanoscale technology as discussed in section II.

Fig. 5 depicts three readout architectures for the LHC trackers that have been implemented as ASICs fabricated both in DMILL technology and with the radiation tolerant quarter-micron approach. All three architectures have the analog signal processing synchronised with the 40Mhz LHC clock.

- The analog readout for which analog data from preamplifiers are sampled and stored in an analog memory that has a depth (typically 2μs to 4 μs) compatible with the trigger latency. This architecture is used for the tracker (APV25) [30] and preshower readout of CMS (PACE) [31], and for the LHCb inner tracker (VELO) [32].
- The binary readout for which a discriminator circuit placed after the preamplifier shaper performs binary digitizing. Then, the one-bit digital data flow is buffered in an on-chip digital memory during the trigger latency. This readout scheme is used in the readout electronics of the ATLAS tracker (ABCD) [33], and a similar scheme is used for the pixel readout chips of ALICE and ATLAS [34].

- The digital architecture in which the analog data flow from the analog front-end circuit is digitised in an array of on-chip analog-to-digital converters (ADC). This new approach, employed for the silicon drift detector of ALICE (PASCAL), has been possible thanks to the low power analog design and the 10-bit 4 Msamples/s ADC that has a power dissipation below 2mW [23].

Several other ASICs have been successfully developed, for example, for calorimeter electronics [35], muon electronics [27], TRT electronics [36] and data transmission electronics [37].

IV. NANOELECTRONICS

Today the impetus for nanoelectronics [38,39] comes from the recognition that someday silicon scaling will be faced with unaffordable fabrication costs caused by the extreme difficulty of manufacturing integrated circuits in the future nanoscale CMOS. In the "top-down approach" used since the beginning of integrated circuits, nanometer scaled lithography, together with the increase of process complexity of highly scaled transistors and interconnects, is the crux of probably the most challenging manufacturing process in history. Today's wafer foundries cost around $3B each and are expected to reach over $ 10B within a decade.

Another obstacle comes from physics as previously discussed. Device and process engineers have been extraordinarily clever in creating novel transistor structures on silicon to demonstrate MOS device operation at less than a few tens of nanometers [40]. However, in spite of this progress, the barriers to further scaling of CMOS are becoming clear, and the more fundamental are quantum effects, which cannot be circumvented by technological tricks.

Therefore, around 2015-2020 microelectronics will probably reach in a point beyond which totally new approaches will be necessary. Several completely new approaches are emerging in order to replace CMOS and address the timeframe that follows on from the current SIA Technology Roadmap. Nanoelectronics is widely considered the most attractive approach because quantum effects such as quantum confinement and the Coulomb blockade, which both appear at nanoscale dimensions, are exploited to form the basis for fundamentally new device types, whereas in MOS devices they limit attainable performance.

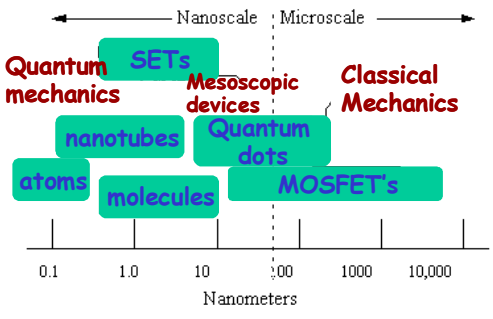

Figure 6. The different types of nanoelectronics devices organized in sizes. In the mesoscopic range 10nm-100nm, device behaviour is governed by both classical and quantum mechanics.

A wide range of new device concepts, as shown in Fig 6, has been proposed, such as single electron circuits, molecular electronics, quantum computation etc. These novel concepts rely on being able to control of the properties of artificial atoms (nanometer-scale silicon islands and quantum dots) or even individual atoms or molecules.
For the first time, the 2001 edition of the ITRS roadmap contained a chapter on "Emerging Research Devices"[14]. However, as characteristic of any new area, it is difficult to discern which of these concepts has the potential to provide a technological basis of the future. It is believed that alternative nanoelectronic technologies are possible within a horizon of 15 years.

A major barrier to the introduction of nanoelectronics is that there are no established mass production techniques for creating devices on a commercial basis. Whereas the transistor is a basic building block for microelectronic devices, it is not clear what the basic (three-terminal) element of a nanoelectronic device will be.

The two possible routes to the future fabrication of nanoelectronic devices are 'top down' or 'bottom up' approaches. The 'top down' approach is basically an extension of the established method of engineering in microelectronics processing, using controlled lithography steps by photons, thermal oxidation, substrate doping by ion implantation, and metallisation. This "planar" process approach is characterised by the deposition, patterning and etching of layers of material, with typically a planarisation step using chemical-mechanical polishing to create layers of wiring.

The bottom-up approach is inspired by self-organisation and self-replication concepts from the biotechnology world [41], but is far from practical reality at this time. Manipulation of atoms and molecules with the Atomic Force Microscope (AFM) is currently a research laboratory activity and the practicality of eventual industrial scale processing of self-organized molecular electronics is far from clear off at this time. Nevertheless, several semiconductor companies are pursuing this approach by developing toolboxes [42] containing organic molecules, carbon nanotube devices (CNT's), DNA molecules and nanoparticles (quantum dots) that can be self-arranged into an information processing system. However, today the most mature emerging device is the Single Electron Tunnelling transistor (SET).

The SET transistor

In contrast to the beginnings of the integrated circuit 50 years ago, when only one device candidate was known (the bipolar transistor, and later the MOS transistor), today's development of nanoelectronics devices is much more complex [43]. There is a plethora of nano-scale devices under development in research laboratories. The oldest one is the SET transistor [44], whereas carbon nanotube devices [45], molecular devices [46], nanowires [47], and DNA are among the more recent and exotic ones.

The SET transistor is the best example to illustrate the potential of nanoelectronics, because there is already an accumulated experience of 15 years, and several

semiconductor companies have developed SET processes compatible with CMOS planar technology and have manufactured functioning memory or logic circuits.

The SET device depicted in Fig. 7 consists of just one nanoscaled conducting island (single-electron box) separated from external electrodes by two tunnelling junctions RT1 and RT2. An electrical field may be applied to the central island using a capacitively coupled electrode Cg. The SET device is clearly reminiscent of the MOSFET, but with a small conducting island limited by two barriers, instead of the usual channel connecting source and drain.

Electrostatics shows that the energy of the system depends on one single electron charging phenomena that heightens the tunnelling potential barrier between the source and the central island. This is the Colomb Blockade effect, which is only possible under certain conditions. One of the most important conditions is that the charging electrostatic energy $E_C = e^2 / C_\Sigma$ involved in one tunnelling event should be higher than the thermal energy kT. The control of the transmission of a single electron through the SET is achieved by modulating the gate electrode voltage. At a certain threshold voltage Vt, the Coulomb blockade is overcome, more electrons are attracted to the central island, and current starts to grow with voltage. The most important property of the SET transistor is that the threshold voltage Vt that controls the conductance of the device is a periodic function of the gate voltage, vanishing for periodic values, called Coulomb blockade oscillations as shown in Fig 8.

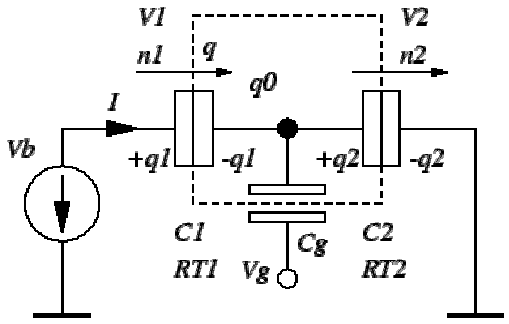

Figure 7. Equivalent circuit of the Single Electron Transistor (SET). Device conductance is controlled by Vg gate voltage. Total gate capacitance C_Σ that includes Cg and RT1-RT2 junction capacitances is in the range of one atofarad and below.

One of the main challenges in the development of the SET device was to prove its operation at room temperature, which has been demonstrated in 1999 [48] with few-nanometer scale silicon islands. At nanometer-size with gate node capacitance C_Σ of a few atofarad, the silicon island begins to operate as a quantum dots in which quantum confinement energy adds to the electrostatic energy.

The periodic conductance oscillations characteristic of double junction electron transistor have also been observed in several other nanoelectronic devices, such as quantum wires and arrays of nanoparticles. Several attempts have also been made to hybridise SET transistor with MOS devices to build realistic digital circuits [50].

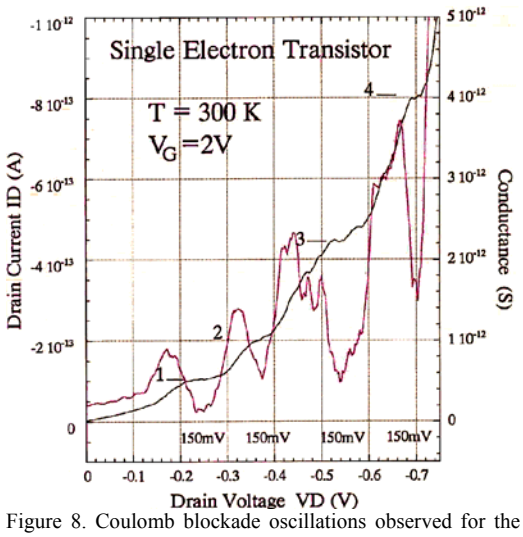

Figure 8. Coulomb blockade oscillations observed for the first time with a room temperature single electron transistor. Source J. Shirakashi et al, , 1998, ref: [49]

So far, all attempts made with single electron devices are not yet good enough for digital and analog circuits. Nanoelectronic fabrication techniques based on CMOS technology methods turn out to have very poor yield and uniformity in threshold voltage due to random charging effects.

V. FUTURE IMPACT OF MICROELECTRONICS ON HEP

The next emerging industrial CMOS technology node, the 0.13μm CMOS process, will still use thermal oxide to form the gate insulator. Subsequent technology nodes, 90 nm and below, will employ novel high-k gate dielectrics with unproven radiation hardness. Therefore, 0.13 μm CMOS is a good choice for the technology for the future generation of ASICs for LHC.

One can expect that the radiation hardness of 0.13 μm technology will be at least as good as the 0.25μm technology, since the SiO2 gate dielectric will be the same. The thinner oxide (2nm) will even increase radiation tolerance because electron tunnelling will be more efficient in neutralizing radiation-induced trap charges. However, low-voltage operation (1.2V) and gate leakage will become an issue for the design of analog front-end circuits, and the development of adapted analog design techniques is certainly necessary.

For the future sub-100nm CMOS process, 90 nm and below, radiation hardness of high-k dielectrics cannot be predicted, and sub-1V supply voltage will make the design of any analog circuit extremely difficult. Pixel detectors could be the only remaining route to design front-end electronics in these future technologies, because binary readout could be still feasible and gain in noise and pixel density would be quite substantial. Monolithic integration of the pixel detector will be certainly an interesting approach for high-density pixel detectors.

Future applications of nanoelectronics in HEP still remain unclear. So far applications of single electron circuits have been limited to quantum electrometers [51,52] and single-photon detection [53]. The adaptation of the single electron transistor to analog front-end amplifier turns out to be extremely difficult. The single electron transistor cannot be used as a "detector impedance adapter" as is done with bipolar and MOS transistors, because its geometry is not scalable with the detector capacitance [54]. Therefore, to be compatible, the detector should be segmented into nanoscale dimensions, which is not an obvious approach.

VI. SUMMARY

Thanks to MOS scaling and the availability of deep sub micron CMOS manufacturing to HEP design teams, most of the challenging tasks of building complex radiation hardened ASICs with performance pushed to the limits for the LHC experiments has been very successful. The forecast by the semiconductor industry shows that miniaturization of CMOS technology will continue for another decade. Certainly, there are opportunities for novel circuits and sensors integrated in the emerging technologies, such as sensors integrated in CMOS electronics for particle and light detection.

Beyond the 10-year horizon, deep nanoscale CMOS technology will face a whole range of potential obstacles; as the technologies are pushed to smaller sizes, the cost of the silicon foundries and fabrication cost of lithography mask sets shoots up, and the tolerances at nanoscale range are more difficult to maintain.

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