The Front-End Driver Card for the CMS Silicon Strip Tracker Readout

8th Workshop on Electronics for LHC Experiments Colmar

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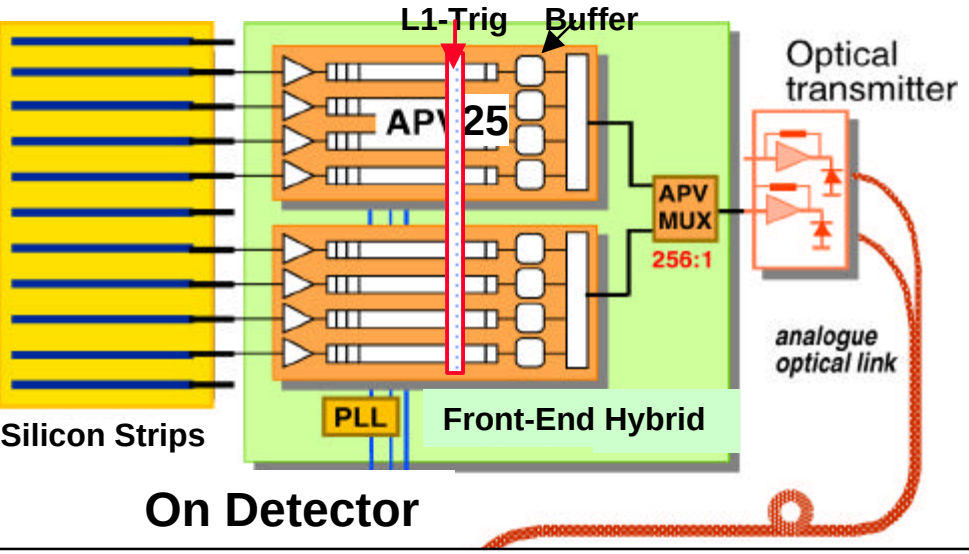
CMS Silicon Strip Tracker FED

Silicon Strip Tracker Readout Overview



~ 9 million Silicon Strip channels

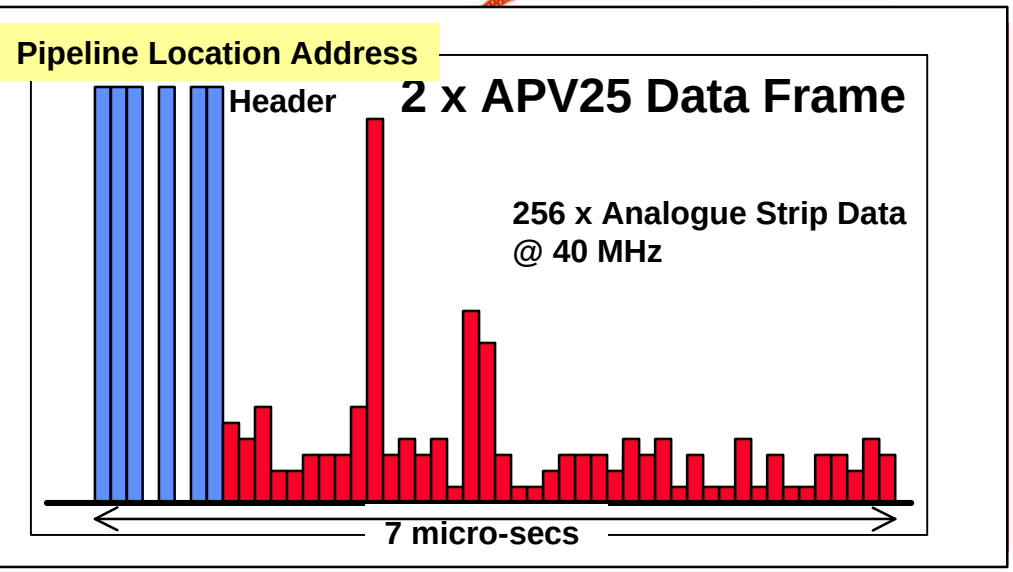
ON Detector: 73K APV25 pipeline chips

@ L1 Trigger: MUX APV Frame output clocked at 40 MHz

Analogue Data readout via Optical links

(APV Frame: Header + Strip Data)

Max L1-Trigger rate = 100 kHz*



*** "Back to Back" Frames**

in absence of Triggers
APV25 outputs "Tick" marks

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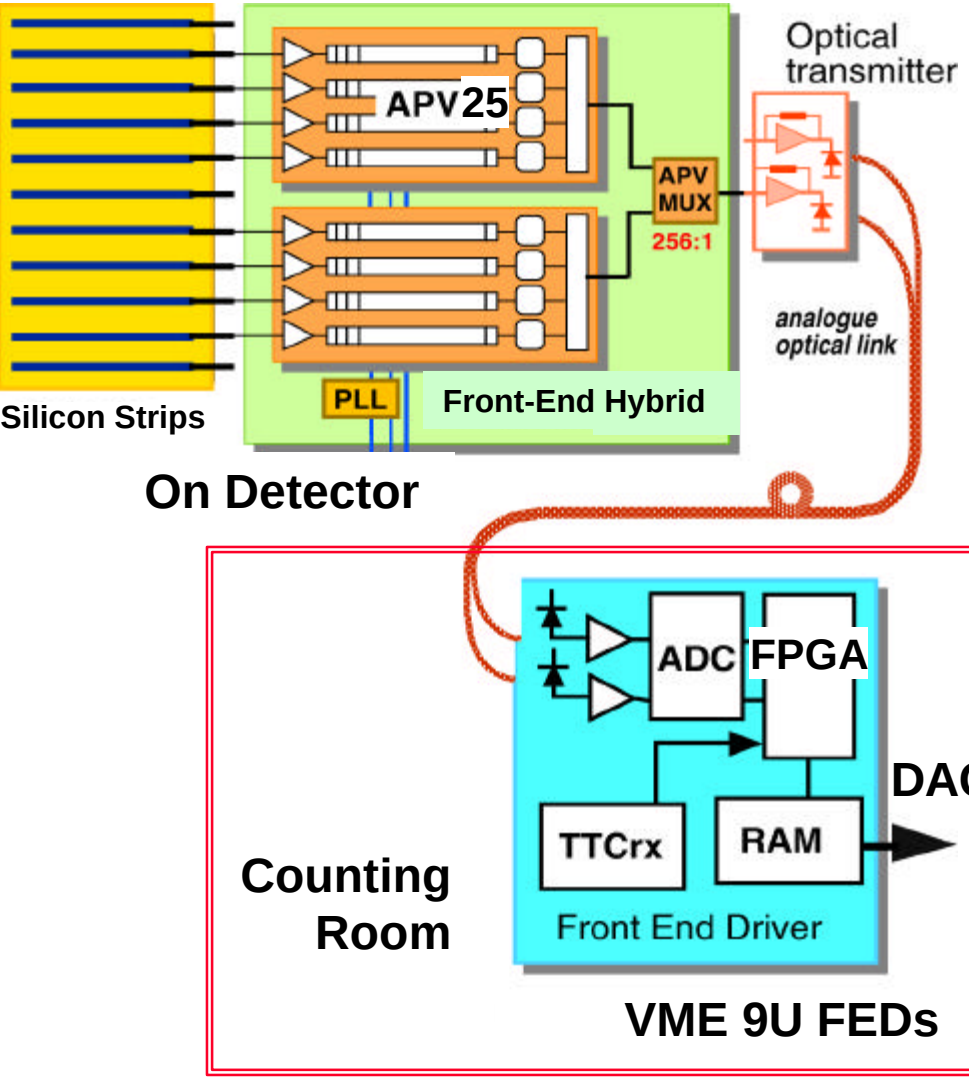

~ 9 million Silicon Strip channels

ON Detector: 73K APV25 pipeline chips

@ L1 Trigger: MUX APV Frame output

Analogue Data readout via Optical links

(APV Frame: Header + Strip Data)

OFF Detector: Front-End Drivers (FED)

Digitise / Zero Suppress / DAQ readout

440 x 9U VME64x boards

96 ADC channel boards

"Front-End Hybrid" : Ulrich Goerlach

"Tracker System Test" : Nancy Marinelli

FED Project Status:

50 x PMC 8 ADC Prototypes used for module tests

First Full Scale 96 ADC Prototypes FF1 about to be manufactured

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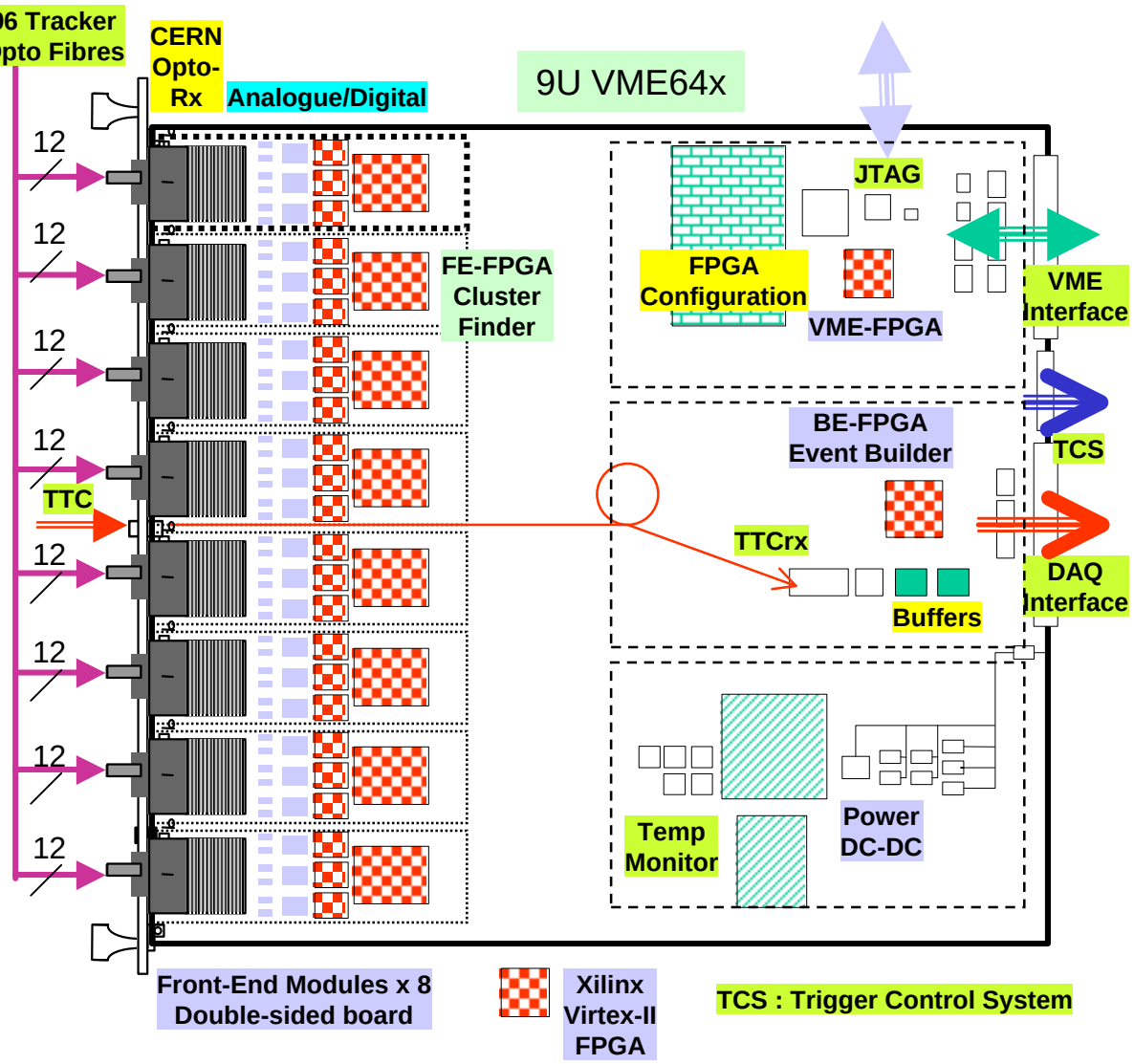
FED Layout



Modularity

9U VME64x Form Factor

Modularity matches Opto Links

8 x Front-End “modules”

OptoRx/Digitisation/Cluster Finding

Back-End module / Event Builder

VME module / Configuration

Power module

Other Interfaces:

TTC : Clk / L1 / BX

DAQ : Fast Readout Link

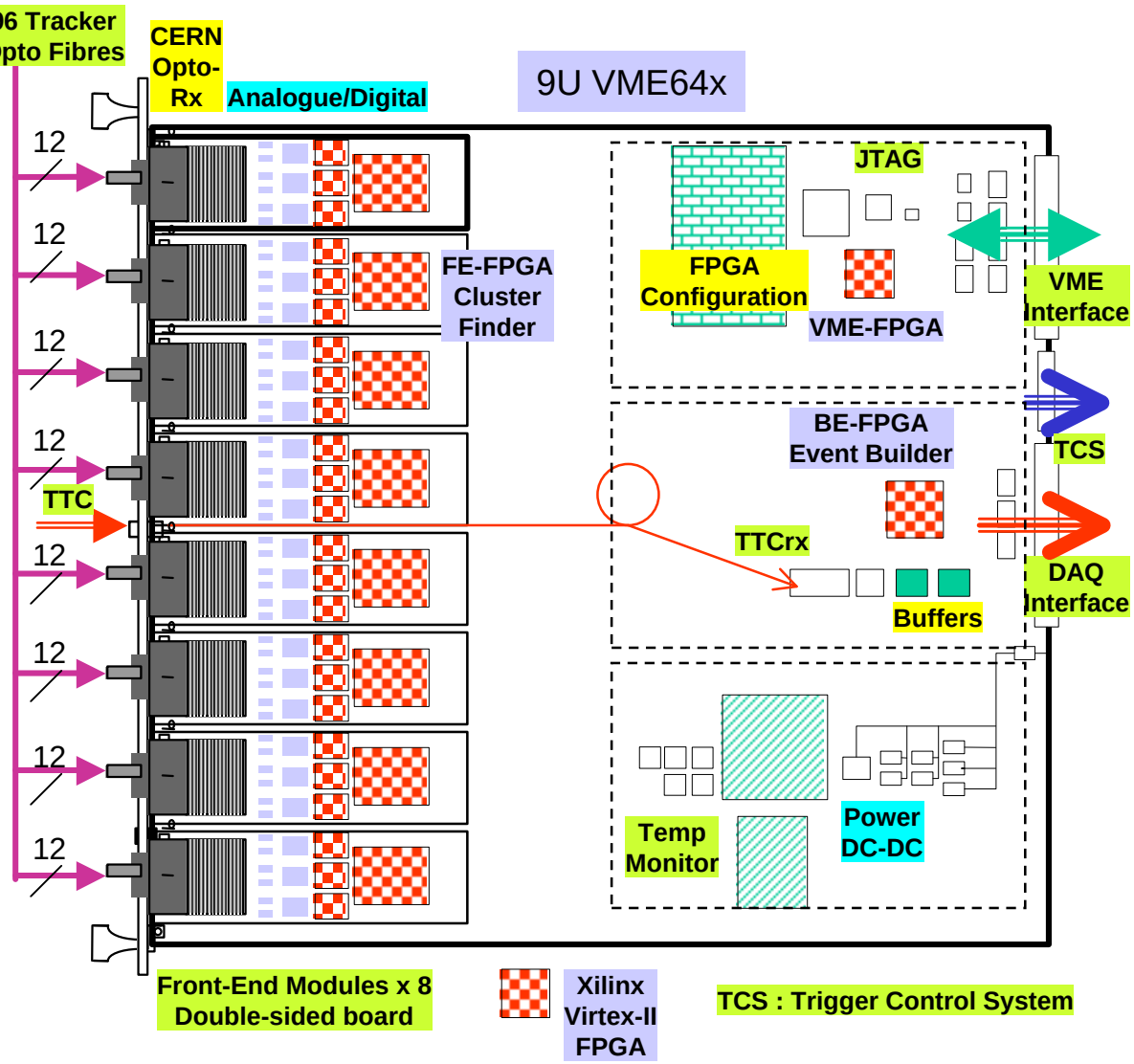
TCS : Busy & Throttle

VME : Control & Monitoring

JTAG : Test & Configuration

CMS Silicon Strip Tracker FED

FED Layout



Data Rates

9U VME64x Form Factor

Modularity matched Opto Links

Analogue: 96 ADC channels (10-bit @ 40 MHz)

@ L1 Trigger : processes 25K MUXed silicon strips / FED

Raw Input: 3 Gbytes/sec*

after Zero Suppression...

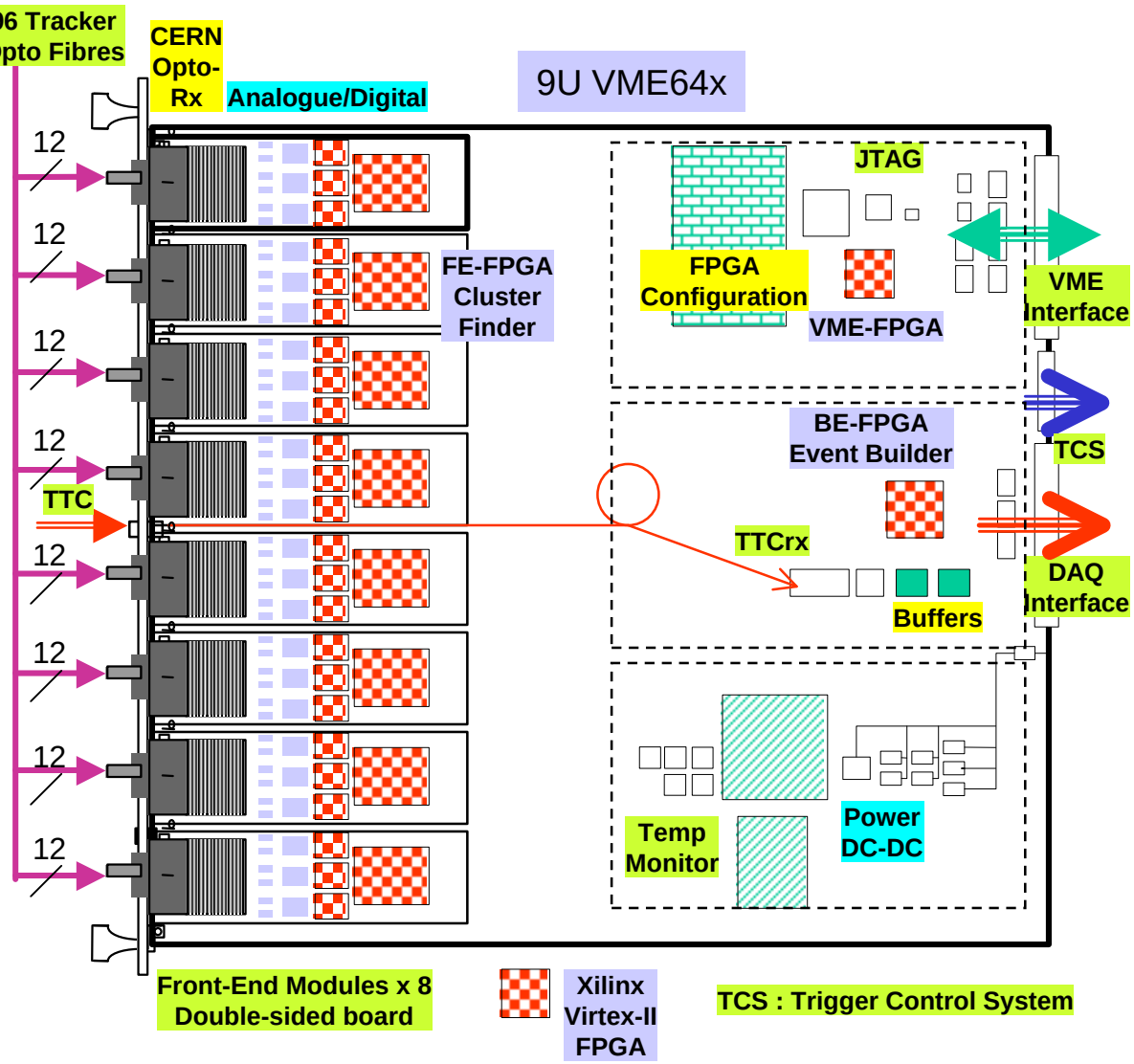
DAQ Output: ~ 200 MBytes/sec

~440 FEDs required for entire SST Readout System

*(@ L1 max rate = 100 kHz)

CMS Silicon Strip Tracker FED

FED Layout



Digital Processing

Flexible Digital Logic:

Xilinx Virtex-II FPGAs 40K->3M gates*

*some in pin compatible packages

Features:

Dual Ported Block Rams

Digital Clock Managers DCM

Double Data Rate I/O DDR

Digitally Controlled Impedance I/O

Various I/O signal standards

Debugging: Logic Analyser cores

FPGAs programmed in

VHDL & VERILOG

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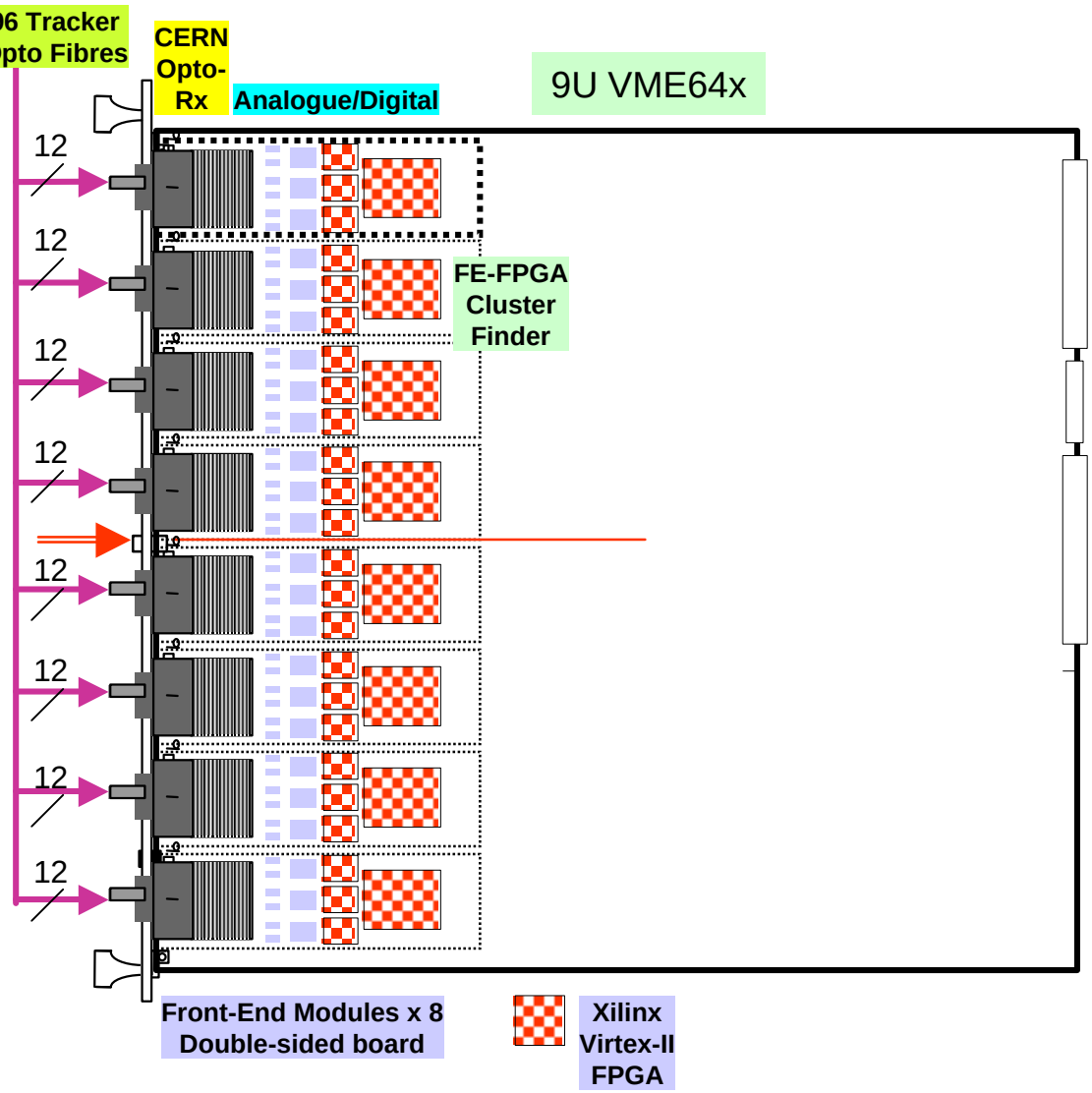
FED Layout

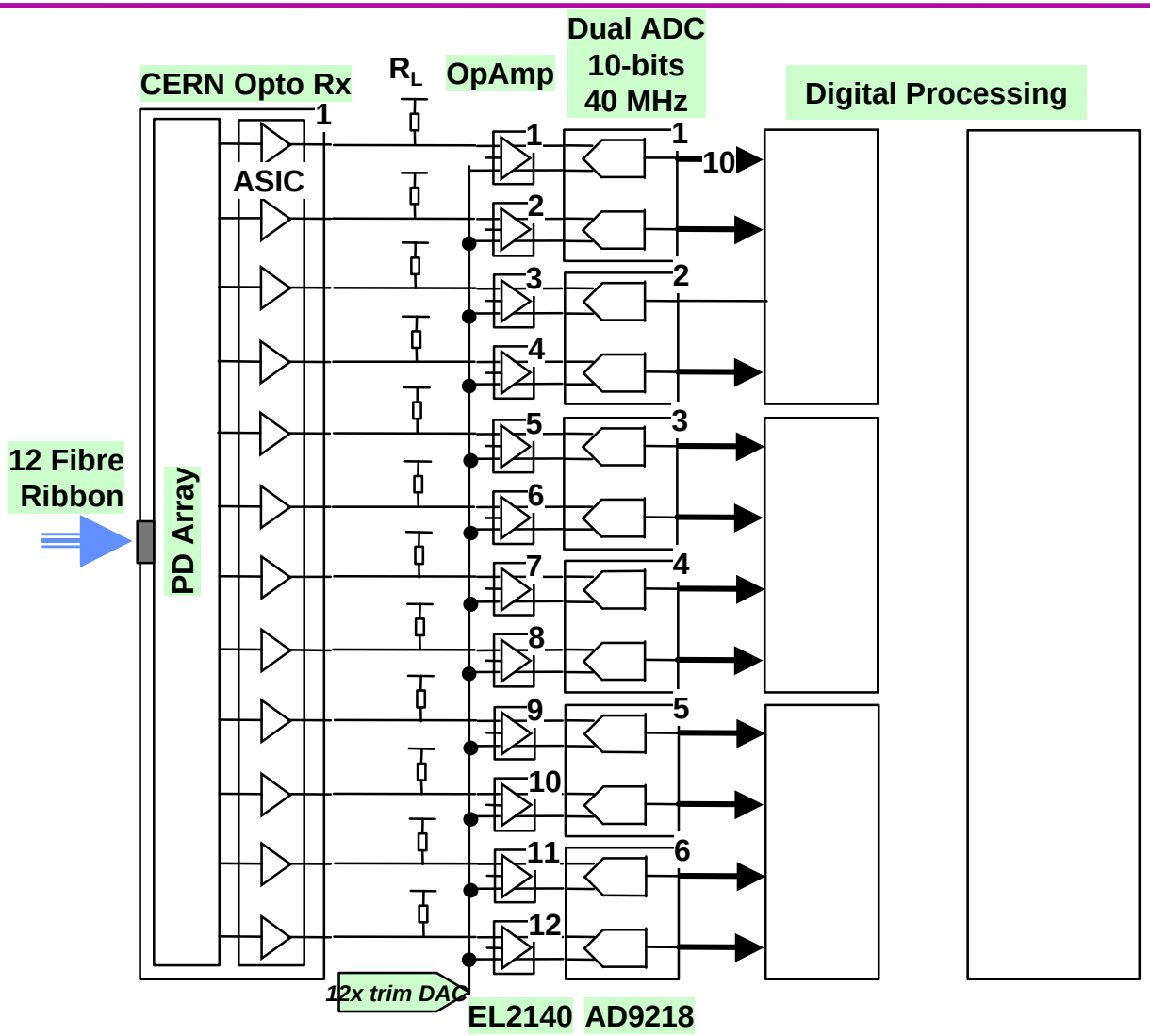


Modularity

8 x Front-End “modules”

CMS Silicon Strip Tracker FED

Front-End module



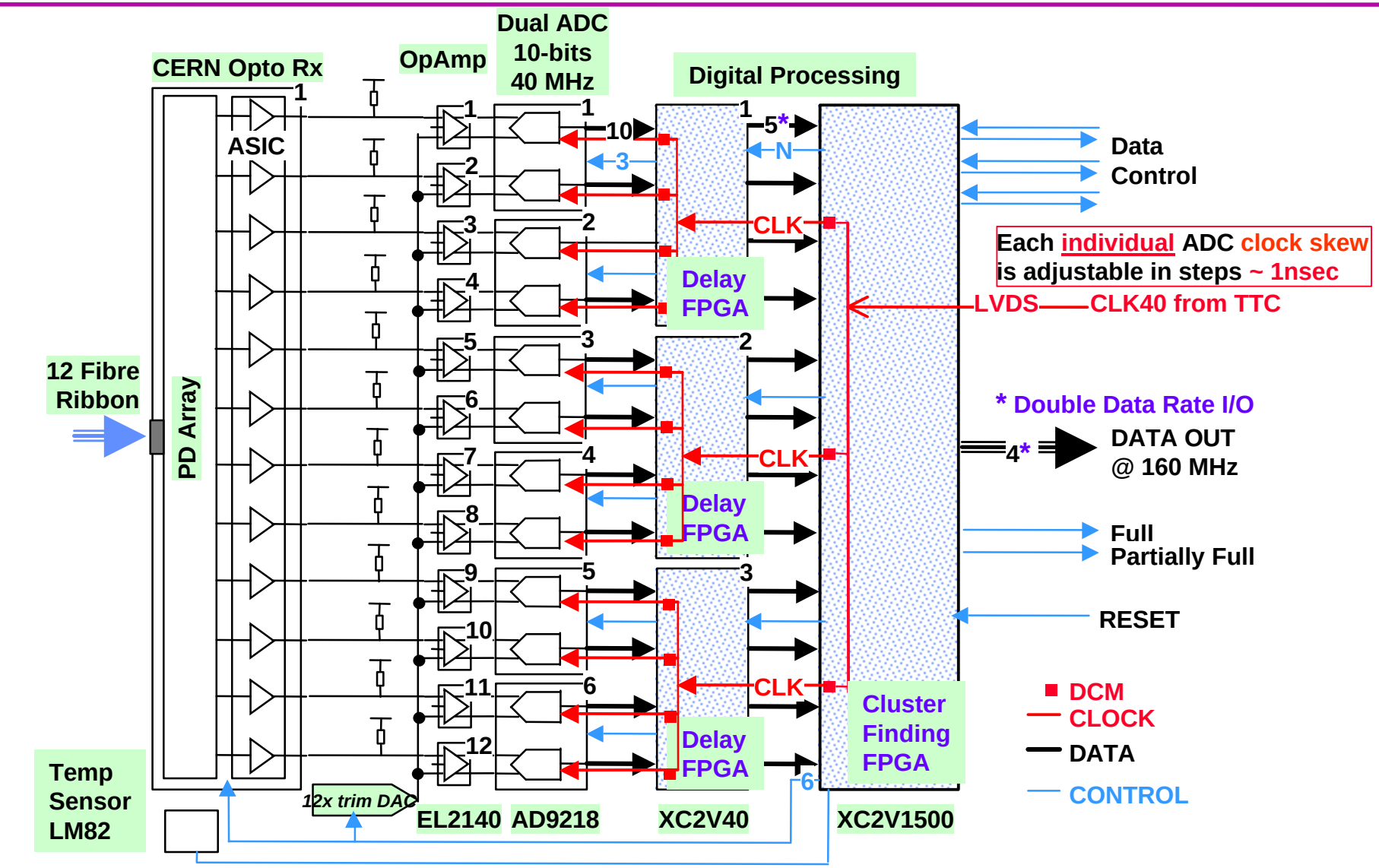
1 MIP ~ 80 ADC counts

Double-Sided Board

DCM
CLOCK
DATA
CONTROL

CMS Silicon Strip Tracker FED

Front-End module



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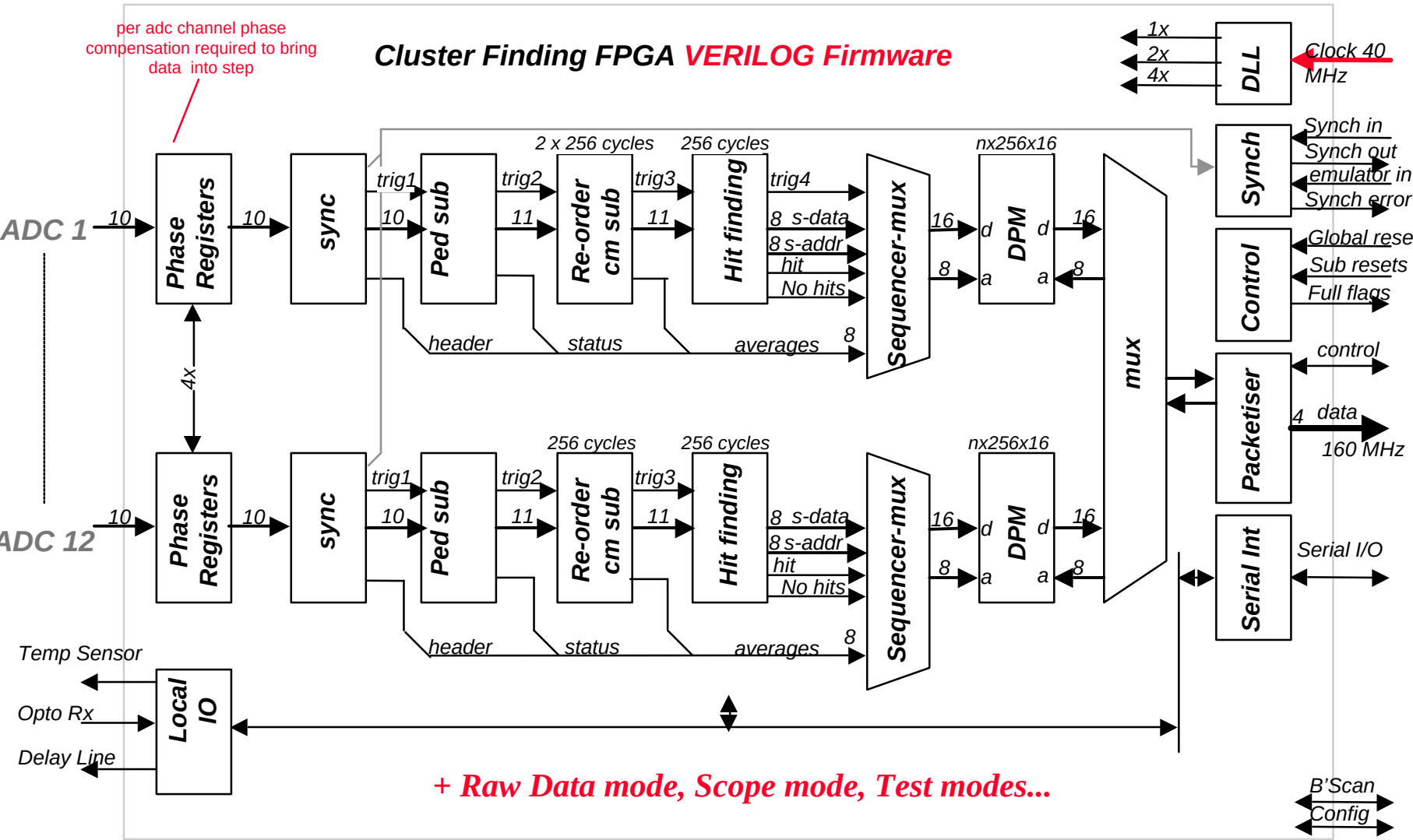
Front-End FPGA Logic



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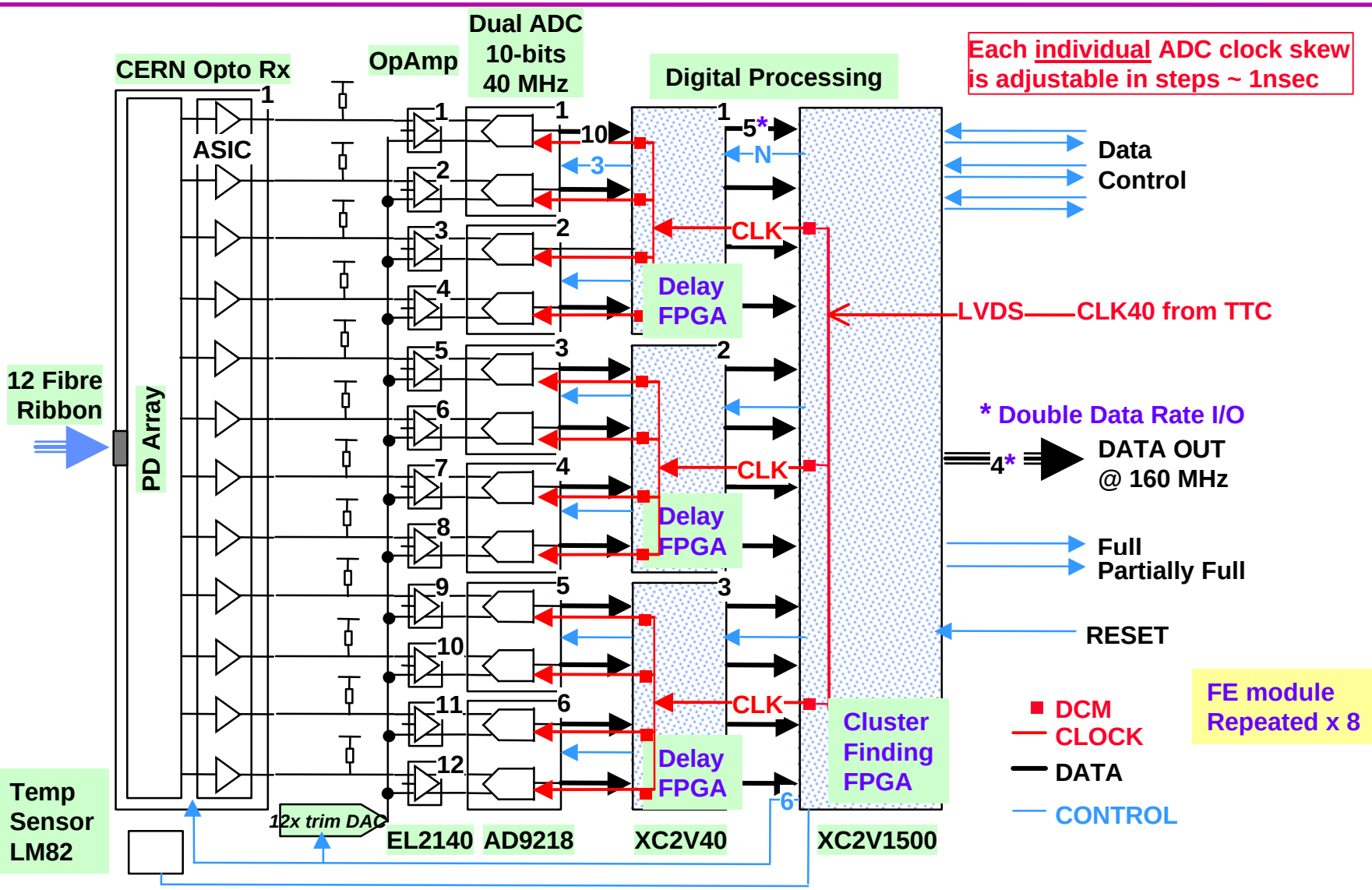
Front-End module



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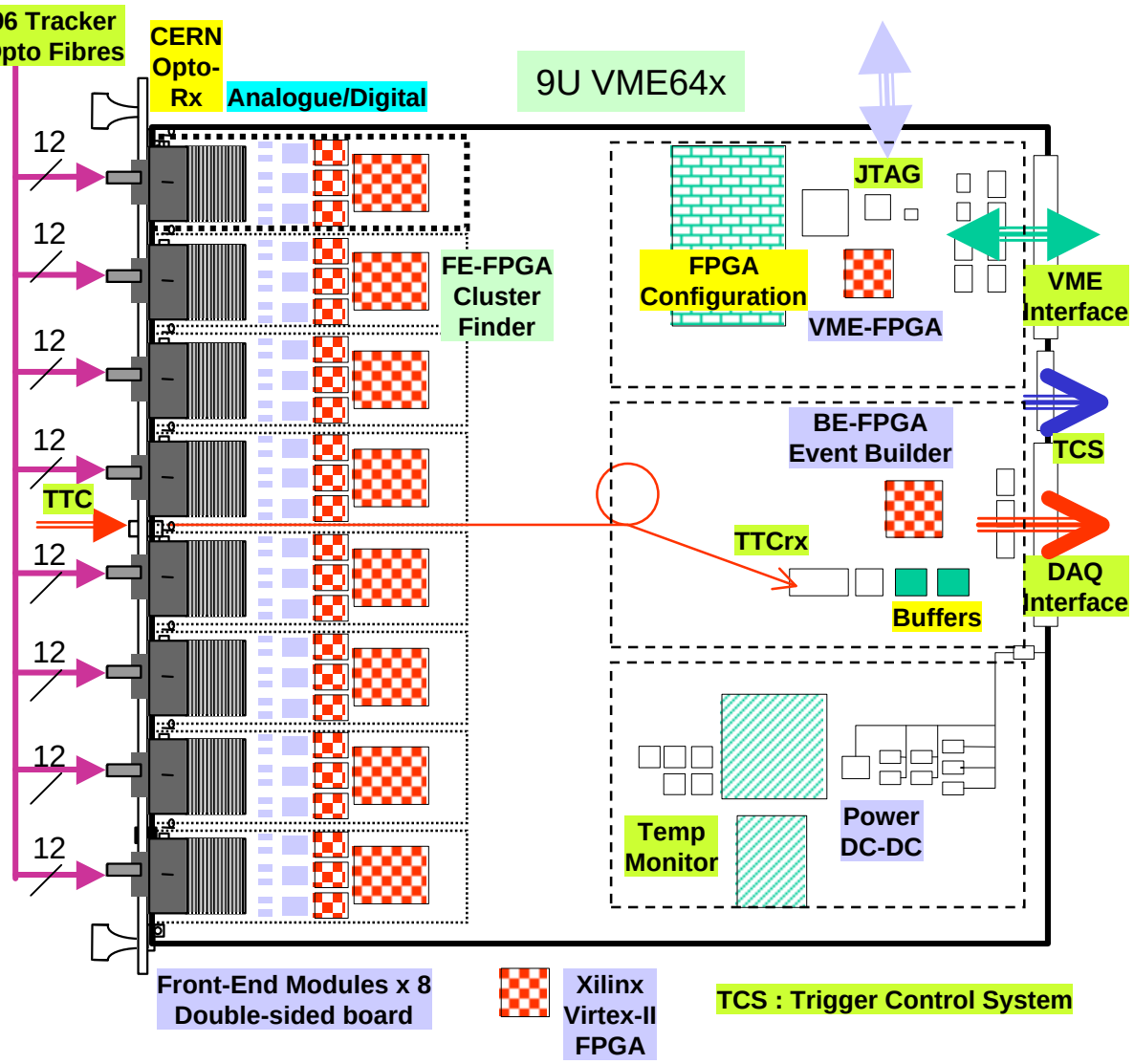

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Modularity matches Opto Links

8 x Front-End “modules”

OptoRx/Digitisation/Cluster Finding

Back-End module / Event Builder

VME module / Configuration

Power module

Other Interfaces:

TTC : Clk / L1 / BX

DAQ : Fast Readout Link

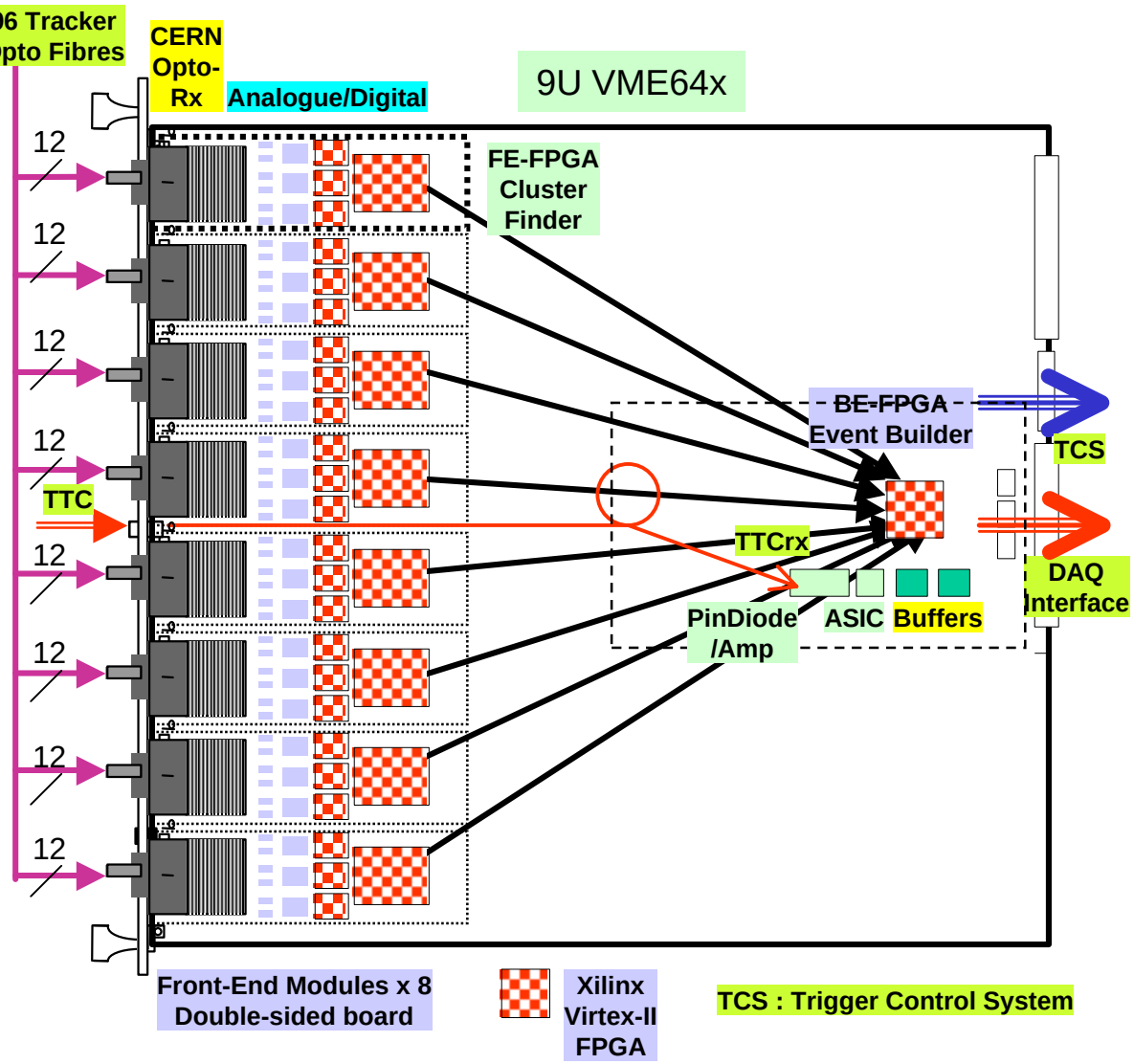
TCS : Busy & Throttle

VME : Control & Monitoring

JTAG : Test & Configuration

CMS Silicon Strip Tracker FED

Full-Scale 9U Layout



Back-End module

For each L1-Trigger:

Collects 8 x FE variable length data fragments

Formats FED event for DAQ

Appends TTC synch information

Buffers in External QDR SRAM

Sends data via DAQ Front-end Readout Link FRL

Signals to TCS : Busy/Throttle

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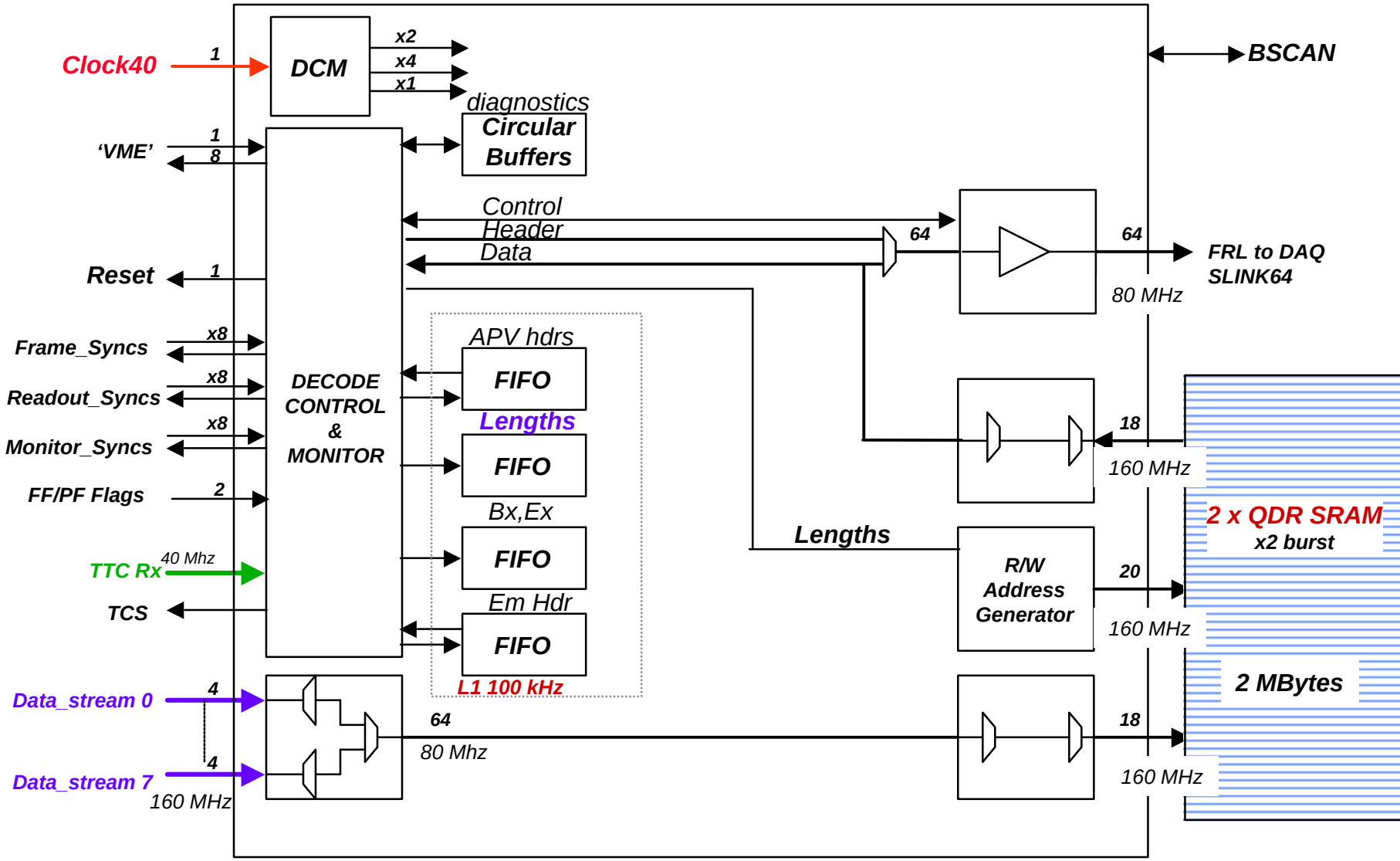
Back-End FPGA Logic



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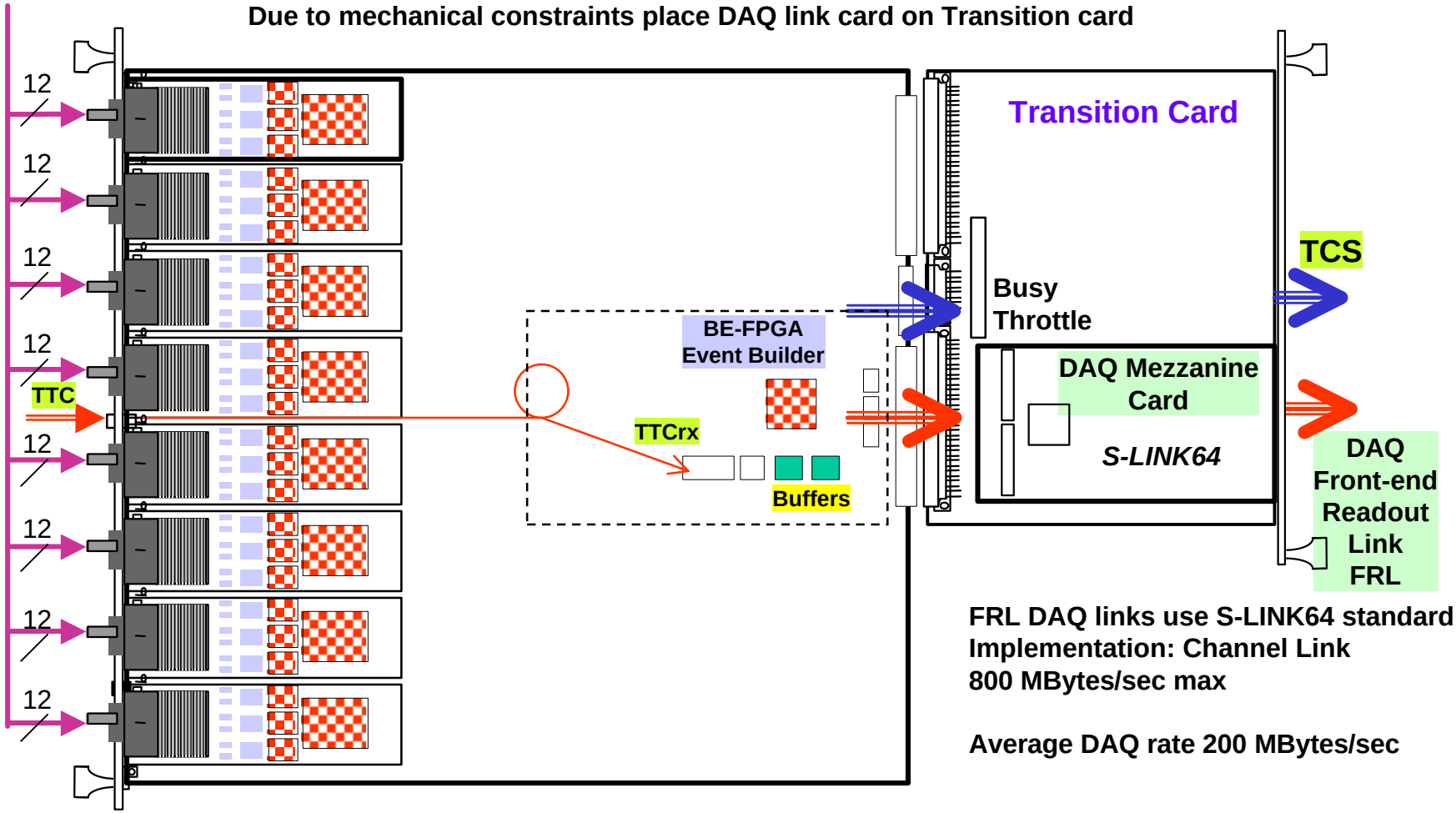
FED-DAQ Interface



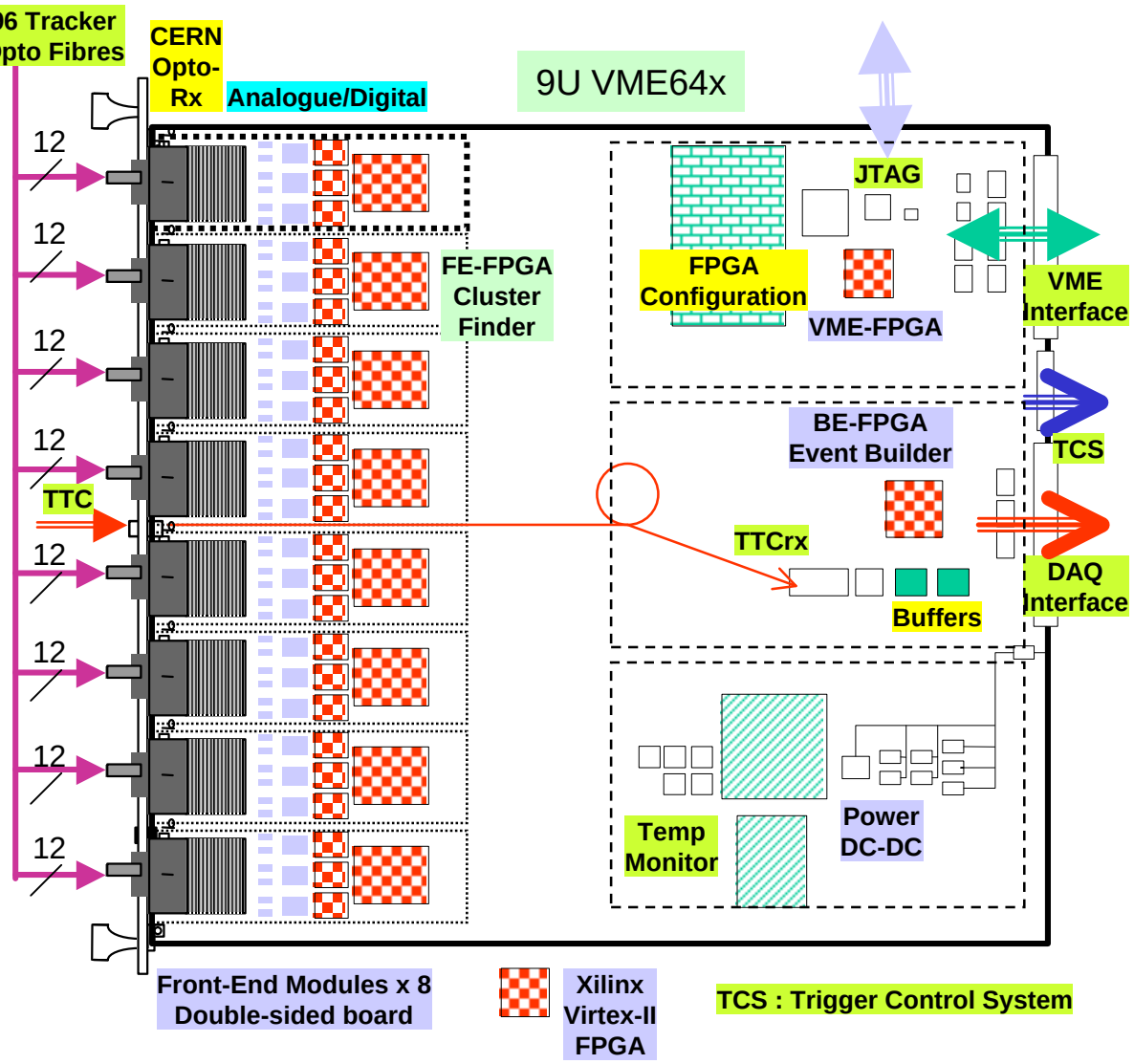
FRL DAQ links use S-LINK64 standard
Implementation: Channel Link
800 MBytes/sec max

Average DAQ rate 200 MBytes/sec

See talk “CMS Data to surface transportation architecture”: Attila Racz

CMS Silicon Strip Tracker FED

FED Layout



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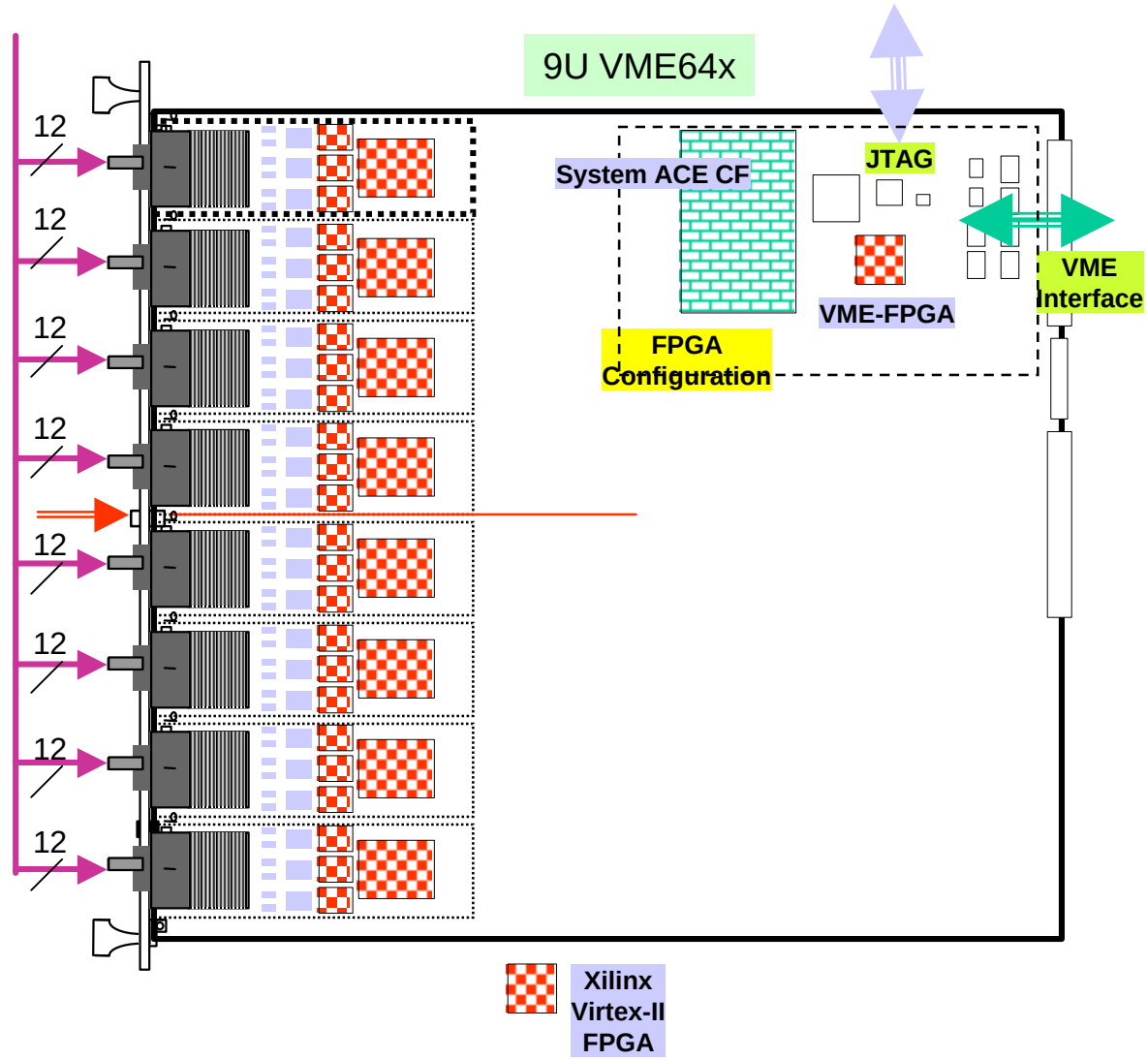
VME module



VME64x Interface:

A32/D64 Slave *& Master*

DMA engine

Interrupter

Plug & Play geographic addressing

Live Insertion Transceivers

FPGA Configuration:

Xilinx System ACE Compact Flash

MPU-VME interface for in-situ reprogramming via Crate Controller

JTAG for Configuration & Test

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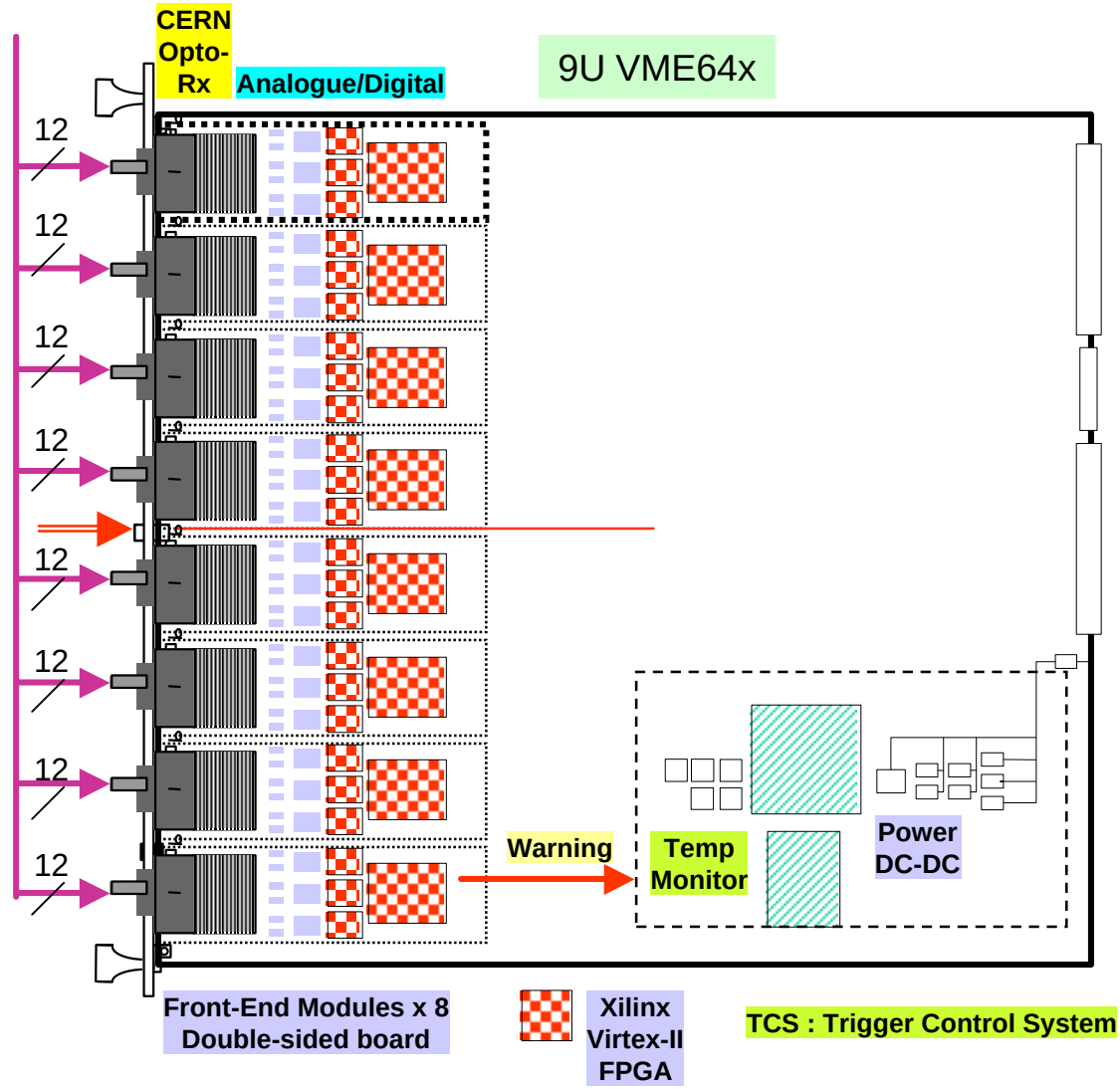
Power module



Standard LHC spec crate supplies:

+3.3V, +5V, +12V

Derive: *-5V, 1.5V, 2.5V* on board

Board Estimate ~ 80 W

Hot Swap Controllers:

Sequence power

Protection against out of range voltage & current

Over temperature shutdown

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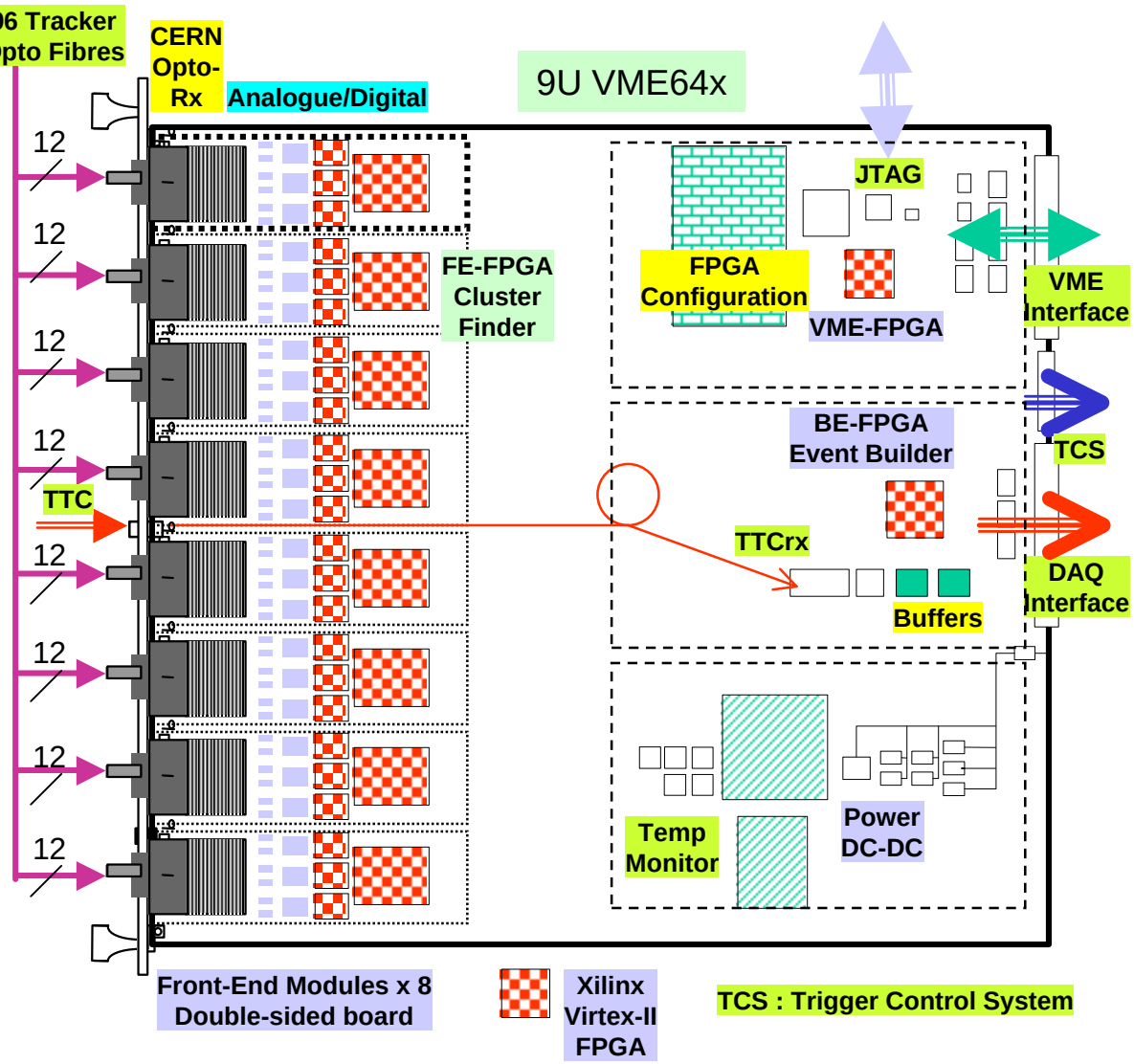
Testing



JTAG Boundary Scan: Digital connections

Chip Scope Integrated Logic Analyser Cores : Capture raw ADC data (without VME)

Opto-Tests or Inject electrical signals post-OptoRx

Special FPGA loads e.g. Pattern Generators

Additional Test Features:

Internal/External Clocks

External Triggers

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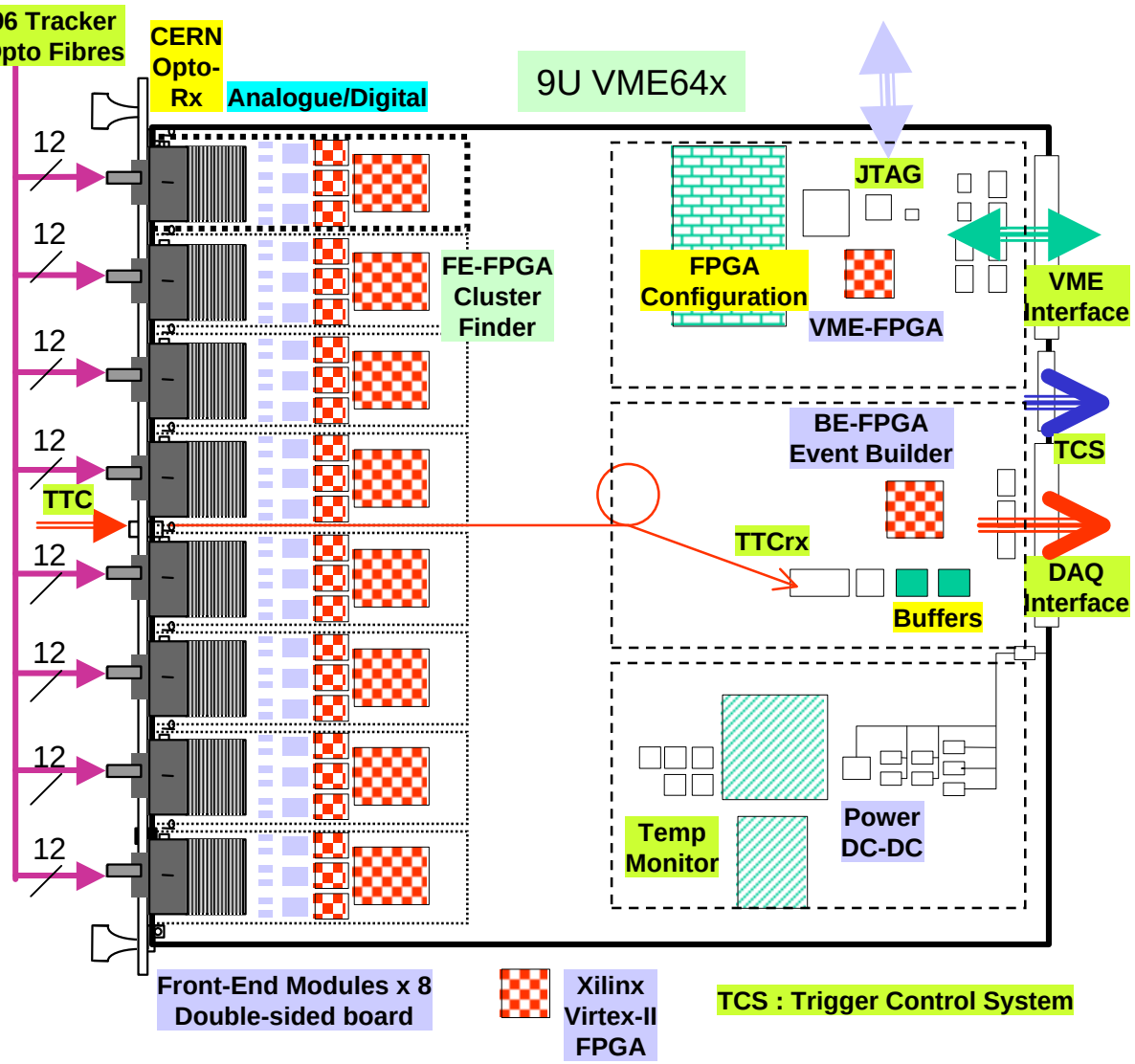
Monitoring



Performance & Status: VME slow monitor data

Cluster Finder Logic

SPY channel in Delay FPGA keeps selected copy of Raw data

Synchronisation

Tracker Front-End Synchronous

Compare APV25 Pipeline Location

APV Emulator cards broadcast Global Pipeline Location

Buffering

FE and BE-FPGAs monitor in real-time status of buffers. Throttle to TCS.

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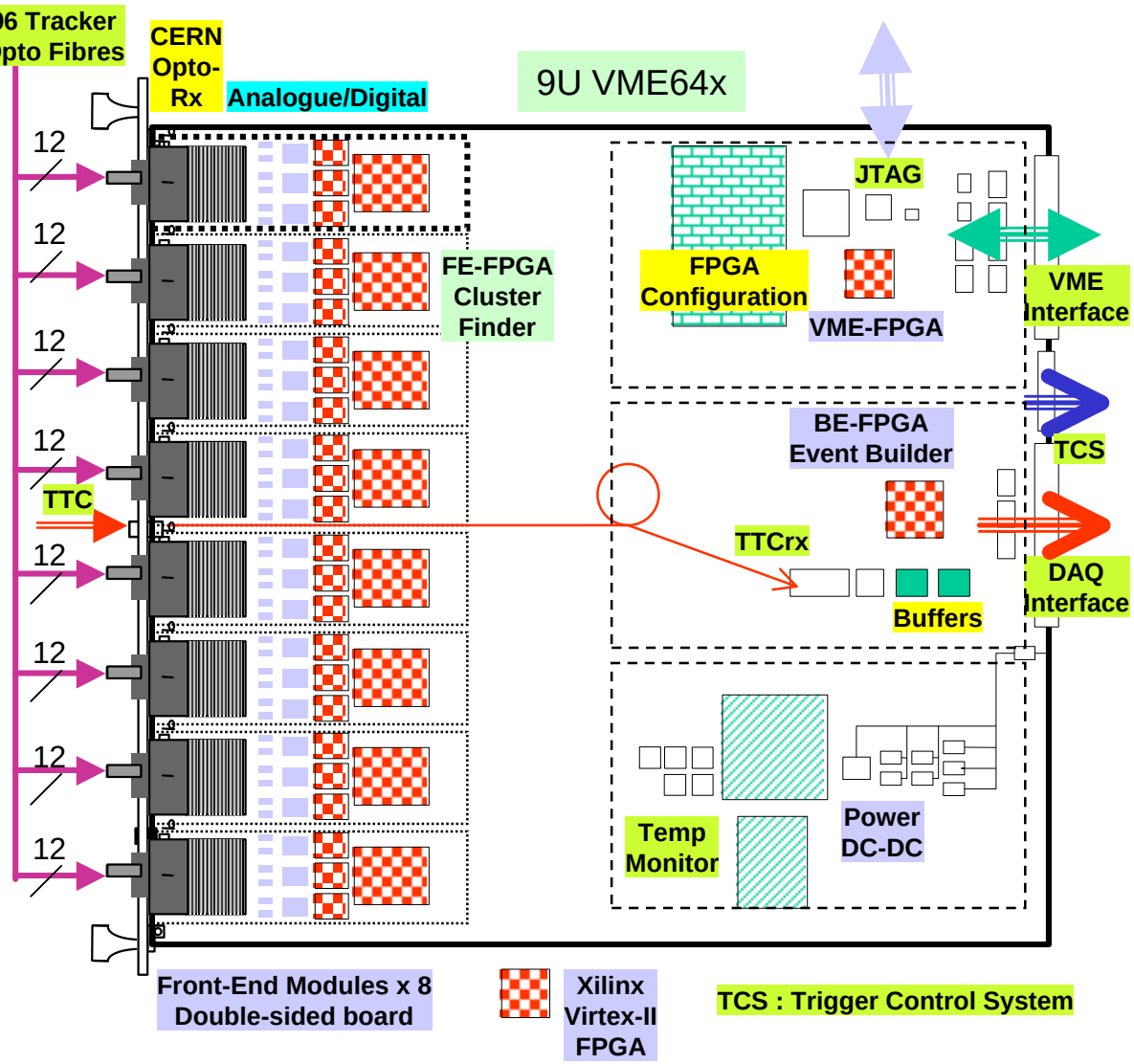
Status



Board Status

Hardware:	
Analogue Design	Complete
Digital Design	Complete
Power Design	Complete
Firmware:	
Cluster Finding	Complete
Event Building	50% Done
VME Interface	10% Done
Board:	
Layout & Routing	Front-End Module Complete Back-End 25% Done

CMS Silicon Strip Tracker FED

Summary & Schedule

Summary

Presented a 9U VME64x board

for off-detector readout of Silicon Strip Tracker

Digitisation

Zero Suppression

Event Readout

Meets SST data rate requirements

Analogue : 96 channel 10-bit ADC @ 40 MHz

Digital : Virtex-II FPGAs flexible logic

Test and Monitor features aid debugging

FF1 : Full scale Prototype
FF2 : Pre-production
FF3 : Final production

Schedule

2002/Q4 : 2 x FF1 @ RAL for test

2003/Q4 : ~10 x FF1 @ CERN

2004/Q4 : ~10 x FF2 manufacture

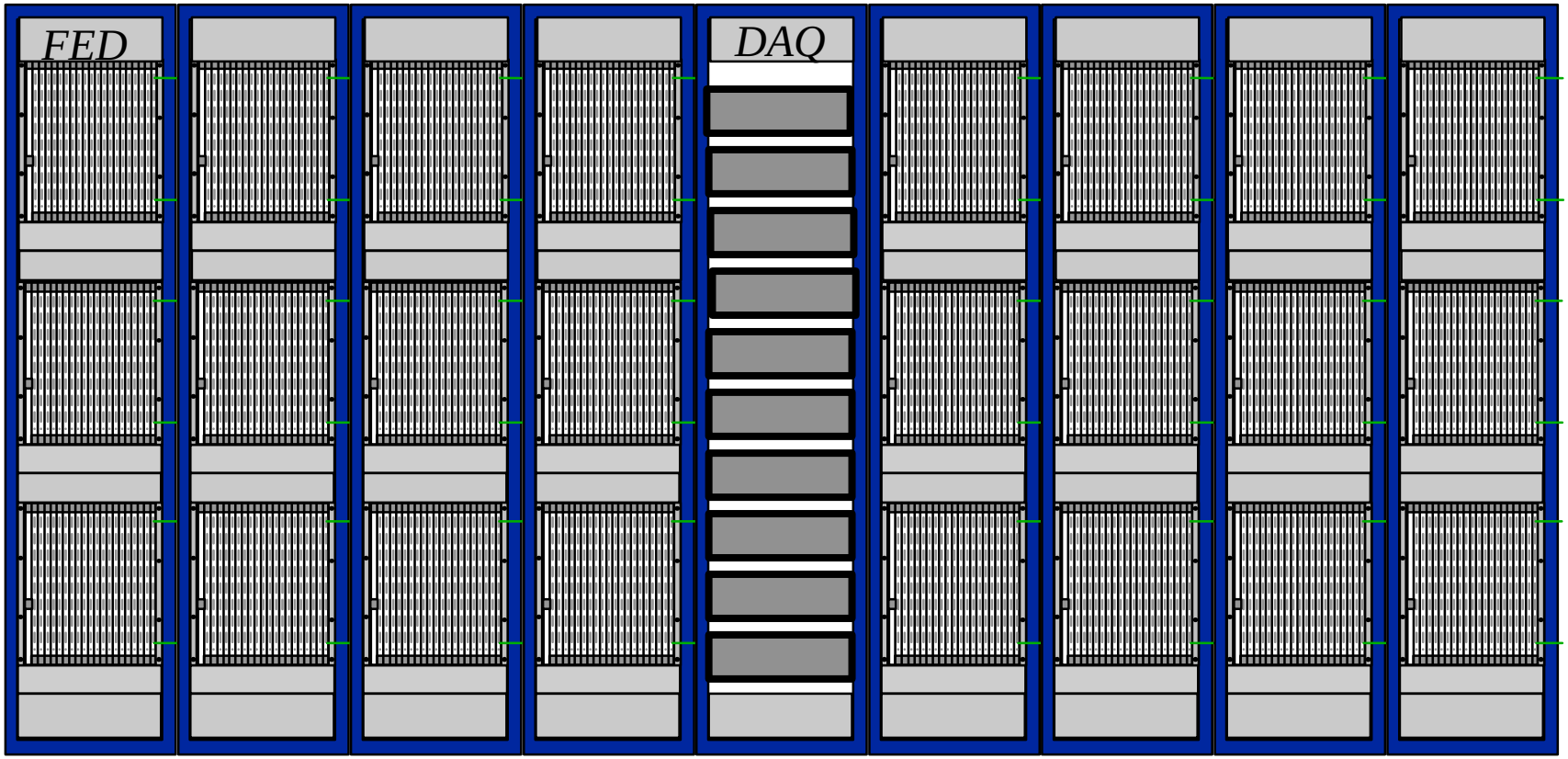
2005/Q2* : 500 x FF3 manufacture

(*funds permitting)

http://www.te.rl.ac.uk/esdg/cms-fed/index.html

CMS Silicon Strip Tracker FED

Counting Room Layout (illustration)

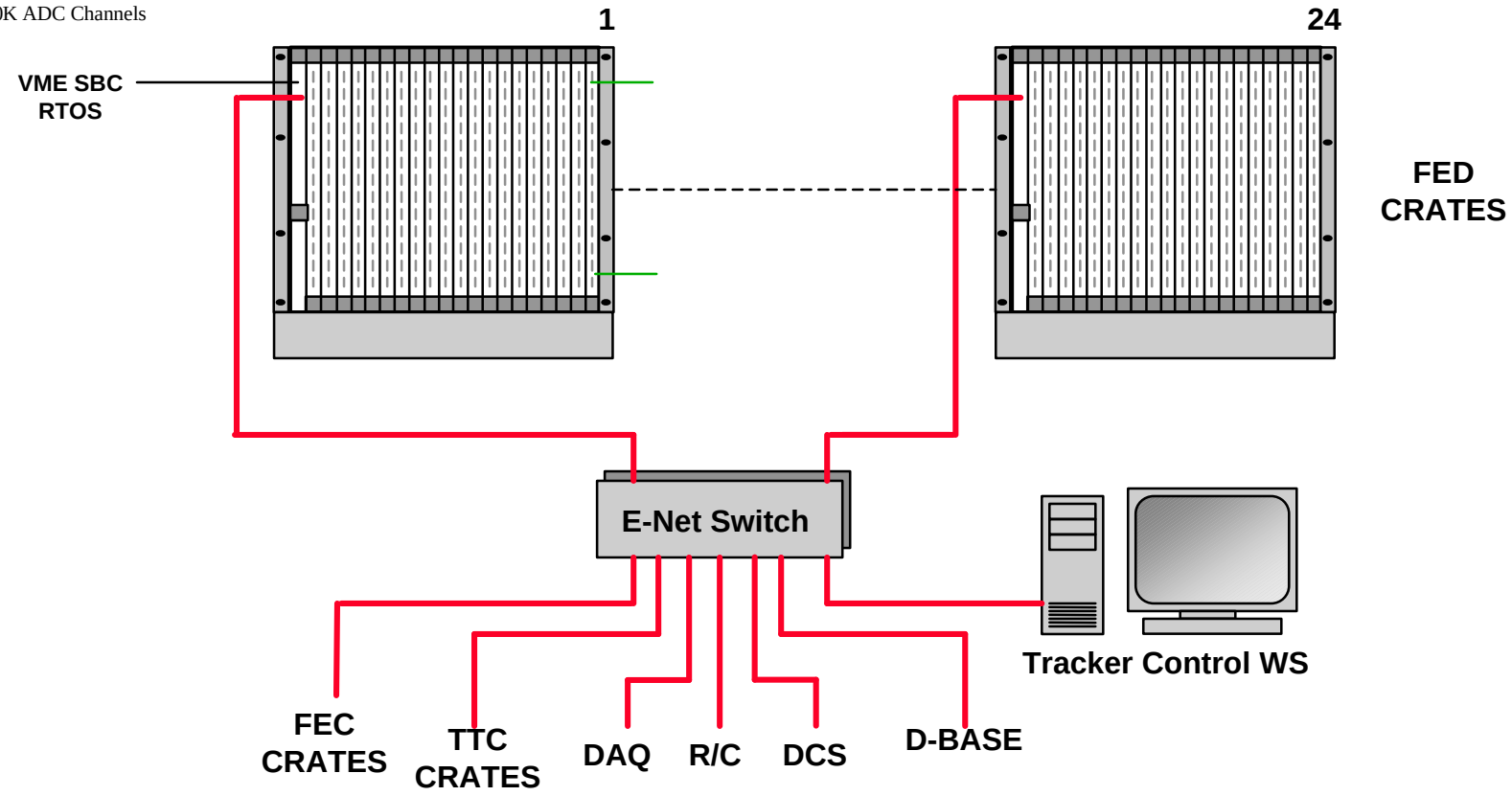


- *40 K ADC Channels* — *10 Bit@40MHz*
- *Max Trigger Rate* — *100 kHz*
- *Input Rate* — *1.5 T Byte/s*
- *Output rate* — *25 Gbyte/s/%*

- *440 Boards* — *96 ADC/Board*
- *24 Crates*
- *8 Racks*

4 TTC Partitions

CMS Silicon Strip Tracker FED
Control & Monitoring



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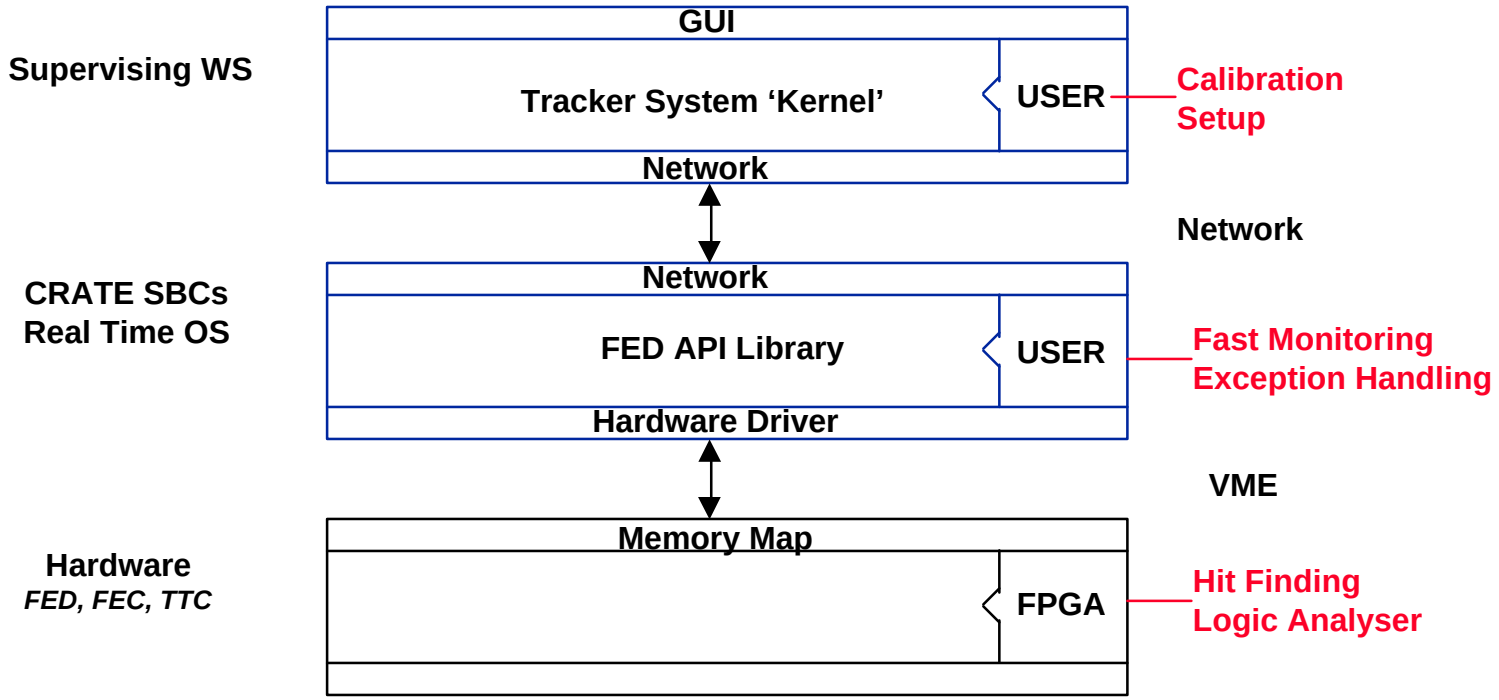
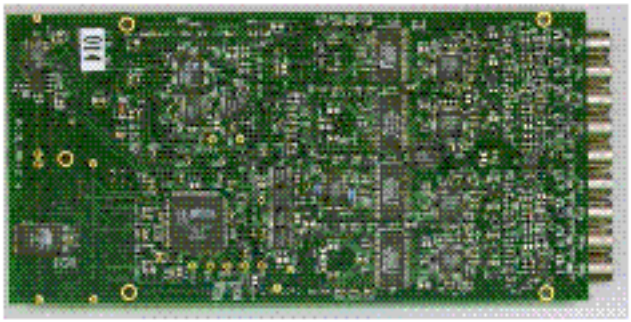
Software Architecture



- ***Software Architecture***
  CMS XDAQ & HAL

CMS Silicon Strip Tracker FED

PMC Prototype



- *8 x 10 Bit 40 MHz ADC*
- *64K Memory/per ADC*
- *40 K Gate FPGA Control*
- *PCI Interface*
- *Mounts on Commercial VME CPU Board (or with an adapter in a PC slot)*

- *60 in service*
- *Present Generation of ADC PMC*

Small scale module testing
System Test beams e.g. LHC 25 nsec

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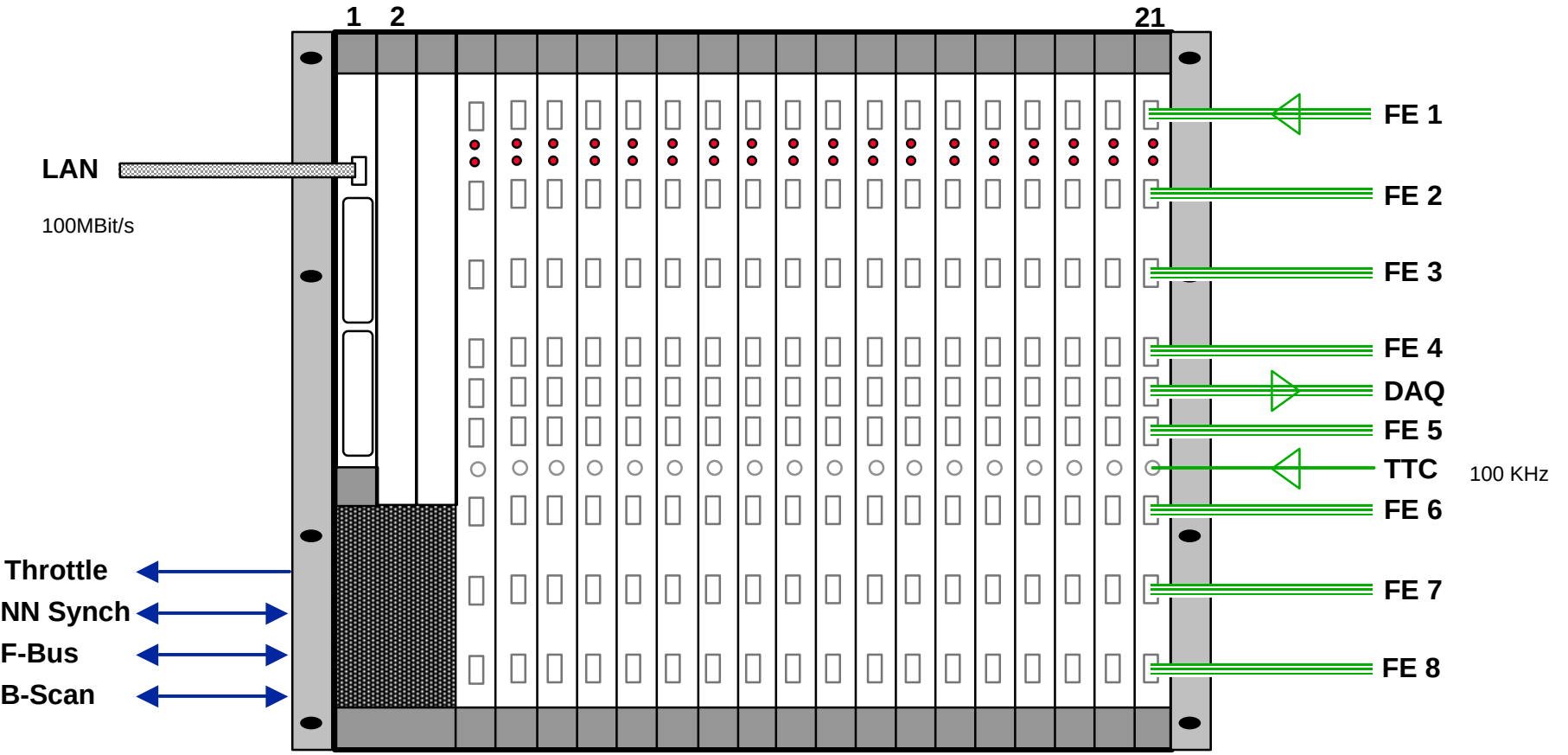
Crate Layout



- **Crate Input Data Rate** **~ 50 Gbyte/s**
- **Crate Output Data Rate** **~ 1 GByte/s per percent hit occupancy**

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FED-DAQ Interface (alternative)