The Front-End Driver Card for the CMS Silicon Strip Tracker Readout.

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Abstract

The first prototypes of the production version of the Front-End Driver (FED) card for the CMS silicon strip tracker are about to be manufactured. The FEDs provide the off-detector processing of the tracker readout system. They digitise and zero-suppress the multiplexed analogue optical data sent on each Level-1 trigger from the on-detector APV25 pipeline chips. This paper outlines the design and describes in detail the implementation of the 96 ADC channel, 9U VME64x form factor card. In total, 440 FEDs will be required to readout the silicon strip tracker.

I. INTRODUCTION

The silicon strip tracker readout (Figure-1) has more than 9 million detector channels and, at expected track occupancies, will generate around half of the final recorded data volume at CMS [1][2]. The system is clocked at the LHC bunch crossing frequency of 40.08 MHz and is designed to operate at sustained Level-1 trigger rates of up to 100 kHz.

Signals produced by the silicon strips are initially processed by on-detector APV25 ASICs [3], each of which reads 128 silicon strips. The APV25s amplify the signals and store them in a pipeline memory until the Level-1 trigger decision is made. On a positive decision, the data from multiplexed pairs of APV25s are transmitted along analogue optical links [4] to the Front-End Driver (FED) cards in the counting room.

The FEDs digitize the data and perform zero suppression (by cluster finding) before transmitting the data to the central DAQ. At projected CMS trigger rates, the total input data rate on each FED will be approximately 3 GBytes/sec. After zero suppression this is reduced to roughly 50 MBytes/sec/% strip occupancy. The average strip occupancy rates in different regions of the tracker will vary between ~0.5% and 3% in high luminosity LHC running.

In total, 440 FEDs will be needed to readout the 73k APV25s of the strip tracker. The production FEDs have to meet tight budgetary constraints whilst maintaining a high degree of data processing flexibility. The latter is necessary, as the demands on the cluster finding algorithms may not be fully known until the experiment is in operation.

The design is highly modular and has been implemented to minimise manufacturing costs. The FED has also been designed with the needs of large-scale production testing in mind.
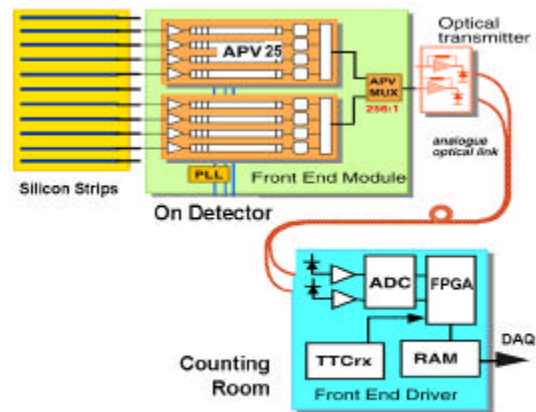

Figure 1: The silicon strip tracker readout system.

FED prototypes [5][6], with restricted functionality and reduced number of channels, have previously been used for silicon detector prototyping and in beam tests. The first fully instrumented prototypes of the production FED are about to be manufactured. These cards will have 96 ADC channels in a 9U VME64x form factor. The FED design has been described previously [7]. This paper concentrates on the implementation of that design.

II. ARCHITECTURE

The FED modularity matches that of the optical links. Each FED receives one optical cable carrying 96 fibres, with each fibre taking data from a pair of APV25s. The fibres are grouped in eight 12-way ribbons, which connect at the FED front panel (Figure-2).

The FED can be conveniently divided into a collection of logical modules, which are described in the following sections. The analogue and zero suppression digital processing is carried out in eight identical Front-End modules. Three further modules provide the remaining

digital processing and configuration functions, DAQ interfaces and power.

Digital processing is carried out in a collection of Xilinx Virtex-II FPGAs [8] ranging in size from 40k to 2000k equivalent gates. The use of FPGA based logic satisfies the requirements of design flexibility. The larger FPGAs have also been chosen in a range of varying gate count, pin compatible packages. This permits the final choice of FPGAs for production cards to be deferred without impacting on the board layout.

The design exploits many of the special features of the Virtex-II family. For example, the large number of Select Block (Dual-Ported) RAMs for data buffering, Digital Clock Managers, Double Data Rate I/O and Digitally Controlled Impedance I/O links.
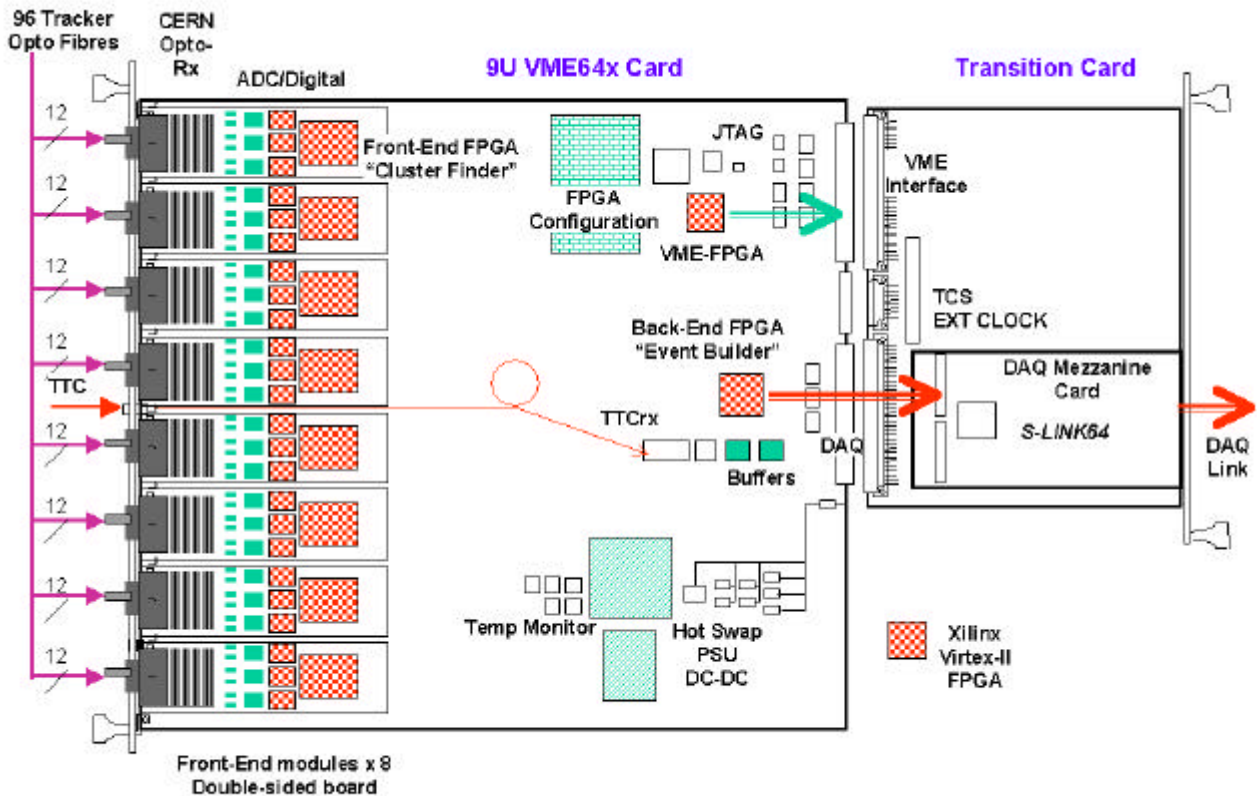

Figure 2: 9U FED board layout with transition card.

A. Front-End Module

Each Front-End module (Figure-3) processes data from a single 12-way ribbon. The optical signals are first converted to electrical signals by an opto-receiver [9]. Within this device, the photo-currents generated by a 12-channel pin-photodiode array are amplified by an ASIC resulting in 12 single-ended current outputs.

Single-ended voltage signals, generated across a load resistor on each channel, are converted to differential signals by high-bandwidth amplifiers [10]. Signal pairs are fed to dual 10-bit differential input ADCs [11] clocked at the LHC bunch crossing frequency. A programmable DAC permits individual voltage offsets to be introduced to each analogue channel in order to match the ADC input range. The digitised data from groups of 4 ADC channels are buffered in 3 "Delay" FPGAs (XC2V40). These FPGAs also have the function of distributing the ADC clocks, after applying appropriate delay skews, to sample the data on each ADC channel at the optimum time. The skew on each of the 96 channels may be adjusted individually in steps of 1 nsec or better. This logic makes full use of the Digital Clock Managers (DCM) of the Virtex-II devices.

A single large "Front-End" FPGA (XC2V1500) then processes the data from each of the 12 channels in parallel. For each channel the logic recognises the arrival of an APV25-pair data frame containing the analogue data from 2 x 128 silicon strips, from a given trigger, preceded by a digital header. The logic also extracts, from the header, the APV25 pipeline location from which the data originated. The pedestal values are subtracted from the data, which are also re-ordered from the APV25 output order into physical channel order.
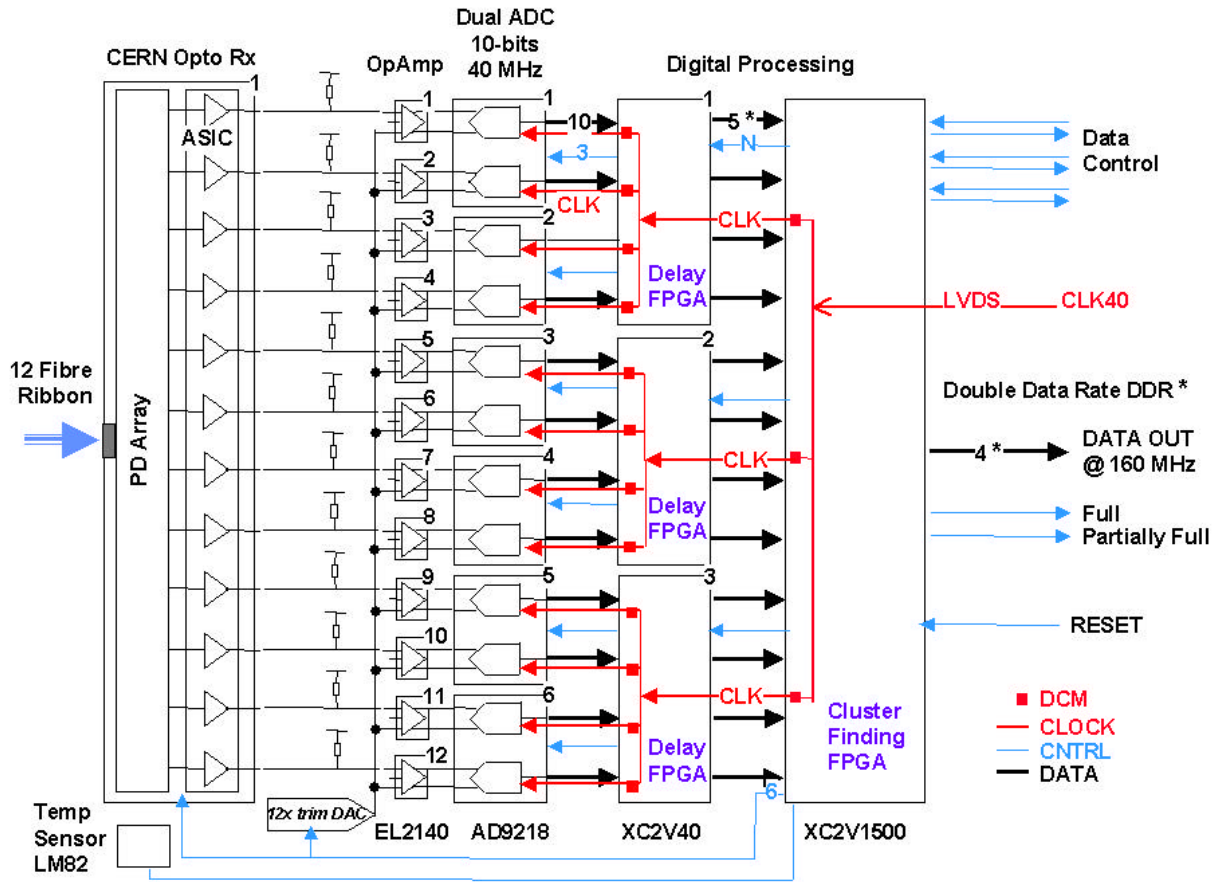
Figure 3: Functional diagram of Front-End module.

For each APV25 the common mode offset is computed from the median pulse height on the strips and then subtracted. A cluster finding algorithm is then run, which searches for groups of two or more neighbouring strips with a pulse height above a low threshold, or isolated strips with a pulse height above a high threshold. Only pulse height data from strips associated with clusters are stored in on-chip FIFOs. Before storage, the data are reduced to 8 bits (1 MIP is expected to correspond to approximately 80 ADC counts).

B. Back-End FPGA Module

The variable length clustered data fragments from all 8 Front-End modules are collected on point to point links (4 bits @ 160 MHz) by a single "Back-End" FPGA (XC2V2000). This builds a FED event for each trigger from the data fragments and formats and stores them in an external memory buffer (2 MBytes deep) to cope with fluctuations in the data rate. The event buffer is implemented by a pair of Quad Data Rate SRAMs [12].

The master LHC frequency clock and L1 trigger signal are provided by the TTC receiver system [13]. The latter comprises a photo-diode/amplifier and ASIC pair. Logic within the Back-End FPGA uses the TTC information to add bunch crossing and trigger labels to the header of each event, which can be used for verification of FED synchronisation by the central DAQ.

The buffered event data from each FED are transmitted to the next stage of the readout via DAQ Front-end Readout Links (FRL), which follow the S-LINK64 protocol [14]. The average zero-suppressed data rate per FED is dependent on which region of the tracker each FED reads out. Data from pairs of FEDs are therefore merged at the receiving end of the FRL in order to satisfy the DAQ requirement of an average rate of 200 MBytes/sec at the DAQ event builder switch inputs.

The FRL is electrical and is implemented, in the baseline design, by standard CMS-DAQ provided mezzanine cards utilising Channel Link [15]. Due to mechanical constraints it will be necessary for this card to be plugged on to a VME transition card (one per FED) located at the rear of the crate. An alternative link scheme, which exploits the ability of Virtex-II to directly drive a channel link interface, and which would obviate the need for a transition card, is also under investigation.

The Back-End FPGA also provides fast feedback signals (e.g. to request a reduction in trigger rate if the

FED buffers risk to overflow) as required by the central Trigger Control System (TCS) [16].

C. VME-FPGA Module

The "VME" FPGA (XC2V500) will provide a VME64x A32/D64 Master/Slave interface with interrupt and DMA functions. The VME path is used by the VME crate computer for controlling the FED, loading calibration constants and reading out data at a relatively low rate for monitoring and calibration purposes. A serial EPROM stores the card identification information. The firmware implements VME64x geographic addressing permitting plug & play VME configuration. Back-plane signals are buffered with (2eVME) transceivers [17], which are also compatible with board "Live Insertion".

The VME-FPGA has a dedicated EPROM for power on configuration. The other FPGAs are configured using the Xilinx System ACE CF product [18]. The FPGA configuration files are stored in standard removable Compact Flash cards. This allows several variants of the design (e.g. different clustering algorithms) to be stored and selected for configuration on computer command. The System ACE controller is also interfaced to the VME FPGA to permit in-situ upgrading of the design files (e.g. over a network connection via the VME crate computer).

D. Power Module

The FED uses on board converters to derive its power from standard VME64x supplies. The estimated board power consumption ~80 W satisfies the recommendations of the LHC VME crate technical specification [19]. Hot swap compatible controllers are employed to protect the on board circuitry from current and voltage out of range conditions and also to control the power up sequence. Power is also shut off in the event of over temperature warning signals from chips monitoring the temperatures of the Opto-Receivers and larger FPGAs. The card is designed to be capable of "Live Insertion".

E. General Design Considerations

The FED has been implemented to minimise PCB manufacturing and assembly costs. All components (apart from the DAQ interface card) are located on the 9U mother-board. Commercial components and solutions have been used where ever possible (e.g. System ACE for FPGA configuration).

The card is double-sided to accommodate the high density of components on the Front-End modules. The number of signal termination resistors is reduced by the use of the Digitally Controlled Impedance feature of Virtex-II. Digital links are kept separated from analogue signals to avoid interference.

The signal interconnection scheme has been kept as simple as possible to ease layout and routing. There are no inter-connections between neighbouring Front-End modules and almost all connections are point to point.

The number of FPGA signal interconnects is minimised by the use of Double Data Rate I/O links.

III. TESTING AND MONITORING

The FED has been designed with the needs of testing and monitoring in mind. The interconnections between all digital devices can be tested using JTAG Boundary Scan [20] test chains. The JTAG chain may also be used for FPGA configuration directly from a PC via a standard cable.

A dedicated opto-test card is under design, which will be able to drive all 96 FED optical channels simultaneously. The electrical part of the chain can also be tested independently by injecting signals on to connectors at the opto-receiver outputs.

In addition to the standard FPGA design configurations, special FPGA firmware will be used during the testing phase (e.g. for generating test patterns to verify S-LINK64 connectivity). In particular, the Xilinx Chip Scope Pro Core logic [21] will be used to implement on chip integrated logic analysers to readout (via JTAG chain) the raw data outputs of the ADCs before the cluster finding logic and VME interface are fully operational. This will permit the connections between the analogue components to be verified.

During special LHC running conditions non-standard operating modes may be selected in the FPGA logic by computer control. For example, during heavy ion running, at low trigger rates, the zero suppression logic may be disabled to permit raw tracker data to be readout. Additional special operating modes will be employed during the commissioning of the tracker system and for regular calibration runs.

For test purposes, the global clock can also be obtained from an on board oscillator, LVDS clock input on P0 VME connector or the VME system clock. Test triggers may also be input on P0.

During normal running the VME interface will be the main channel for monitoring and diagnostics. The Delay FPGAs contain spy memories, which capture a copy of the raw data for a selected number of events. This data can be recorded locally and compared later with the central DAQ data to verify the correct operation of the zero suppression algorithms.

The timing synchronisation of the front-end channels processed by a single FED (at the resolution of a single bunch crossing) is checked for each trigger by comparing the APV25 pipeline locations obtained from the frame headers of each channel. The tracker front-end system is fully synchronous and therefore all locations should be identical. A global check of the synchronisation of all front-end electronics across an entire TTC partition is performed by broadcasting (via the TTC system) the expected value of the pipeline for each trigger from a custom card, which emulates the behaviour of the front-end pipelines.

Various other data checks, such as buffer occupancy and APV25 header integrity, are carried out in real-time within the Front-End and Back-End FPGAs. The results may be read out via VME. Serious error conditions (e.g. loss of synchronisation) will generate local VME interrupts or cause warning signals to be transmitted to the central Trigger Control System.

IV. STATUS AND PLANS

The design of the 96 ADC channel FED is complete. Board layout and routing is being finalised and the first pair of prototype cards is about to be manufactured. Following a period of exhaustive testing of the design, a further dozen cards will be produced for large-scale silicon module testing in 2003. Full production of the 500 FEDs (including spares) required by CMS is expected to commence in 2005.

V. ACKNOWLEDGEMENTS

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