The MROD

The Read Out Driver for the ATLAS MDT Muon Precision Chambers

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Abstract

We present a status report and results on the development of the MROD unit, which is the Read Out Driver for the ATLAS MDT Muon Precision Chambers. First the results of a pilot study (MROD-0) are discussed. Next the results of a full scale prototype called MROD-1 are presented.

I. Introduction

The Monitored Drift Tubes (MDT chambers) form the main component of the ATLAS muon precision detector. Three layers of MDT chambers in the toroidal magnetic field form the muon spectrometer. The MDT system consists of some 1200 chambers and contains a total of about 300k individual drift tubes. The largest MDT chambers contain 432 drift tubes. A schematic overview of the read-out system is given in figure 1.

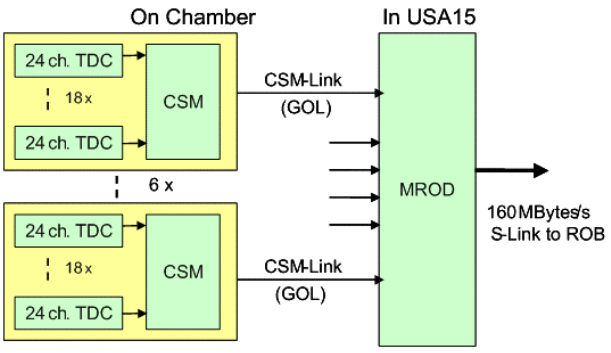

Figure 1: Schematic overview of the MDT read-out system.

On the chambers, front-end cards digitize the wire signals. Each front-end card serves 24 drift tubes. An on-chamber service module (CSM) [1] reads out the front-end cards (maximum 18) and sends the data off the chamber via a 1 Gbit/s optical link (GOL) [2], which is a strictly one-way connection. The CSM acts as a time division multiplexer for the front-end cards.

The task of the MROD, which is located in the USA15 underground area, is to receive and demultiplex the data stream coming from the CSM. One MROD receives and combines data from a number of MDT chambers, which form a "tower": a set of chambers, which together cover the same solid angle. A typical tower comprises six MDT chambers. Next to demultiplexing the data received from the CSMs, the MROD has to build the events from the data of six chambers and send the events over an S-Link connection to the Read Out Buffers (ROBs). In addition the MROD has to report (and possibly correct) errors and inconsistencies in the incoming data streams, to collect statistics and to allow spying on the data streams. Moreover, a number of data compression schemes may be executed by the MROD. The total amount of data to be moved by any MROD is estimated to be less than some 60 MBytes/s.

II. The MROD-0 Prototype

Given the amount of data to be moved, we opted for a test with a SHARC (ADSP-21060) DSP based system, which exploits the fast links between the SHARCs. Based on existing NIKHEF hardware [3] we were able to relatively quickly build the MROD-0 testbed to verify ideas on demultiplexing, event building and routing of data with real hardware. Some FPGA reprogramming had to be done but then the full MROD functionality could be emulated, in particular speed and event building techniques could be tested. The results of these tests were very positive (event rates between 50 and 70 kHz were seen for realistic sets of test parameters). Based on these results it has been decided to build a full scale prototype, allowing for six CSM inputs.

III. The MROD-1 Prototype

The MROD-1 prototype has a modular design. The MROD input and output sections are well separated. The ADSP-21160 (SHARC-II) DSP was used. The SHARC-II is the successor to the SHARC-I and has nominally twice the speed as well as double the bandwidth on the inter-SHARC links. A schematic view of the MROD-1 prototype is given in figure 2.

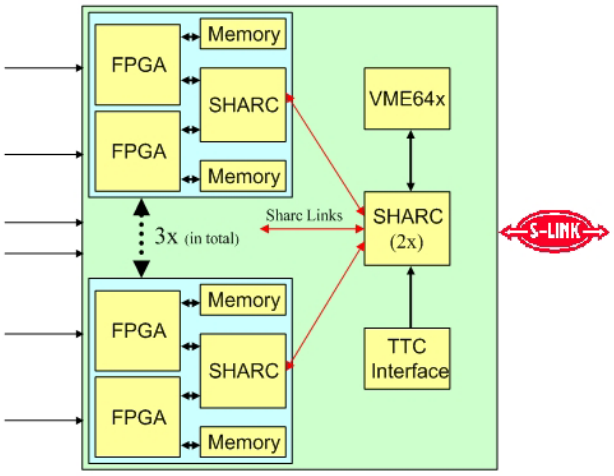

Figure 2: Schematic diagram of the MROD-1 prototype.

The MROD-1 unit is a 9U VME64x module consisting of three dual-input daughter boards called MROD-in, which sit on the motherboard called MROD-out. Each MROD-in has two Altera APEX 20K200 FPGAs and one SHARC-II. The MROD-out has two SHARC-II processors and one APEX 20K100 FPGA and interfaces to the VME64 bus and the TTC system.

IV. Results and Conclusions

Fully functional MROD-1 modules exist [4]: seven MROD-in boards and three MROD-out motherboards are available and have all been extensively tested, also in conjunction with simulated data via the input link. Preliminary results show a sustainable event rate of 125 kHz, with 18 simulated TDCs and five 32-bit TDC words/event for a single MROD-in input link and no MROD-out functionality. This is equivalent to 45 MBytes/s. This result is encouraging and improvements still seem possible.

Software to boot the SHARC DSPs via the VME bus and a run-time environment providing file and terminal I/O via a server program under both the LynxOS and Linux operating systems on the VME processor are available

System integration tests with both the CSM (input) and the DAQ-1 (test-beam DAQ) and the ATLAS ROD Crate DAQ will follow soon. Anticipating the connection to the CSM (still under development elsewhere), a GOL receiver card for the MROD-in is well underway. Moreover the MROD-1 will be applied in the read-out of a local cosmic ray test stand at NIKHEF.

Further tests with the MROD-1 will show whether we may still economize on the total number of SHARCs per MROD. It is foreseen that the next MROD prototype will be the so-called “production module 0”.

V. References

[1] UMHE-01-01, “CSM Design Manual”, J. Chapman, P. Binchi, Univ. of Michigan, Jaunary 30, 2001. Available from: http://atlas.physics.lsa.umich.edu/docushare

[2] http://proj-gol.web.cern.ch/proj-gol

[3] ATL-DAQ-2000-021, “A SHARC based ROB Complex: design and measurement results”, H. Boterenbrood, P. Jansweijer, G. Kieft, R. Scholte, R. Slopsema, J. Vermeulen, NIKHEF, 17 March 2000.

[4] http://www.nikhef.nl/pub/experiments/atlas/daq/mrod