Prototype Slice of the Level-1 Muon Trigger in the Barrel Region of the ATLAS Experiment

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Abstract

The ATLAS barrel level-1 muon trigger system makes use of the Resistive Plate Chamber detectors mounted in three concentric stations. Signals coming from the first two RPC stations are sent to dedicated on detector ASICs in the low-p_T PAD boards, that select muon candidates compatible with a programmable p_T cut of around 6 GeV, and produce an output pattern containing the low-p_T trigger results. This information is transferred to the corresponding high-p_T PAD boards, that collect the overall result for low-p_T and perform the high-p_T algorithm using the outer RPC station, selecting candidates above a threshold around 20 GeV. The combined information is sent via optical fibre to the off-detector optical receiver boards and then to the Sector Logic boards, that count the muon candidates in a region of $\Delta\eta\times\Delta\phi=1.0\times0.1$, and encode the trigger results. The elaborated trigger data is sent to the Central Trigger Processor Muon Interface on dedicated copper link. The read-out data for events accepted by the level-1 trigger are stored on-detector and then sent to the off-detector Read-Out Drivers via the same receiver boards used for trigger data, sharing the bandwidth.

A trigger slice is made of the following components: a splitter, a low-p_T PAD board, containing four Coincidence Matrix boards; a high-p_T PAD board, containing 4 CM boards and the optical link transmitter; an optical link receiver; a Sector Logic board; a Read-Out Driver board.

I. The ATLAS Barrel Level-1 Muon Trigger

The ATLAS muon spectrometer in the barrel, which covers a pseudorapidity region equal to $|\eta| < 1.05$, makes use of the Multi Drift Tube detectors for particle track precise measurement, and the Resistive Plate Chamber detectors for triggering.

The barrel first level muon trigger has to process the full granularity data (about 350.000 channels) of the trigger chambers [1]. The latency time is fixed and less then 2.5 μs. The maximum data output frequency to the higher-level triggers is 100 kHz.

A. Trigger Algorithm

Level-1 trigger main functions are:

- identification of the bunch crossing corresponding to the event of interest;
- discrimination of the muon transverse momentum p_T;
- fast and coarse muon tracking, used for higher-level trigger processors;
- second coordinate measurement in the non-bending projection with a resolution of ~1 cm.

The level-1 trigger is able to operate with two different transverse momentum selections, providing a low-pt trigger (p_T ~ 5.5 GeV), and a high-p_T trigger (p_T ~ 20 GeV). To reduce the rate of accidental triggers, due to the low energy background particles in the ATLAS cavern, the algorithm is performed in both η and ϕ, for both low-p_T and high-p_T triggers. Barrel precision MDT chambers can only measure the bending coordinate, thus the ϕ projection is used to give to the experiment the non-bending muon coordinate with a resolution of ~1 cm. The measured non-bending coordinate is used in addition with the data coming from MDT detectors for precise particle track reconstruction.

A section view of the trigger system is represented in Figure 1, showing where the three RPC stations are located inside the ATLAS Muon Spectrometer. The ATLAS muon trigger system is composed by three RPC stations. The RPC detectors are mounted on the MDT chambers.

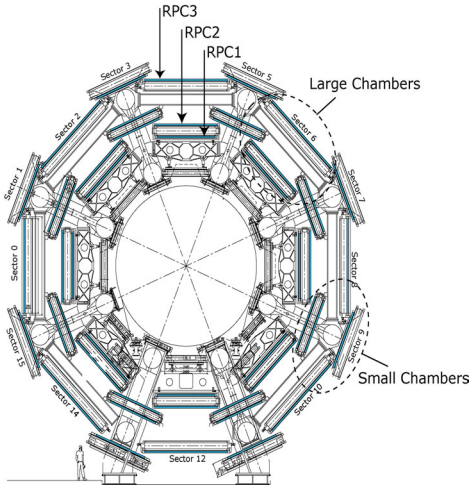

Figure 1: The ATLAS Muon Spectrometer Layout

Each RPC chamber is readout by two planes of orthogonal strips. The η strips give the bending projection, while the ϕ strips give the non-bending one.

Muon p_T selection is performed by a fast coincidence between strips of different RPC planes. The number of planes in the whole trigger system has been chosen in order to minimise accidental coincidences and to optimise efficiency. For accidental counting reduction, the trigger operates in both bending and non-bending projection.

Figure 2 shows the trigger scheme. The low-p_T algorithm makes use of information generated from the two Barrel Middle stations RPC1 and RPC2. The first stage of the algorithm is performed separately and independently in the two η and ϕ projections. If a track hit is generated in the RPC2 doublet (pivot plane), a search for the same track is made in the RPC1 doublet, within a window whose centre is defined by an infinite momentum track coming from the interaction point. The width of the window is programmable and selects the desired cut on p_T (the smaller the window, the higher the cut on p_T). Three programmable p_T thresholds in each projection can be applied simultaneously. To cope with the background from low energy particles in the cavern, a majority coincidence of the four hits of the two doublets in each projection is required.

The high-p_T algorithm makes use of the result of the low-p_T trigger system and the hits available in the RPC3 station. A coincidence between the 1/2 majority of the RPC3 doublet and the low-p_T trigger pattern is required.

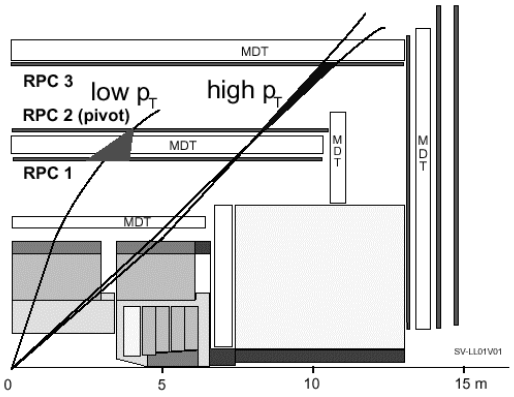

Figure 2: The ATLAS Barrel Level-1 Muon Trigger

B. *Trigger Segmentation*

The ATLAS barrel trigger system is composed of two independent trigger subsystems, the first in the region of positive η values, called barrel system 0, the second, the barrel system 1, in the negative η region [2]. Each barrel subsystem (6.7 m < r < 10.5 m) is made of 8 Large Sectors, 6 Small Sectors, and 2 Special Chambers Sectors in the feet region. Each Sector is organized in three Trigger Stations, RPC1 and RPC2 placed on the external sides of the Barrel Middle MDT chambers, and the RPC3 in the innermost or outermost side of the Small or Large Outer MDT chambers.

RPC stations dimension has been chosen to match the dimension of the corresponding MDT chamber. On each half-barrel plane (positive or negative η) there are 6 or 7 RPC modules along z, depending if the sector is respectively large or small. Each RPC module is composed by two RPC chambers, partially overlapping in the η direction (see Figure 3), and is read in two equal independent ϕ sub-sectors, called Trigger Sectors. Each trigger sector is segmented in PADs and Regions Of Interest.

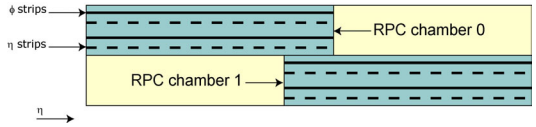

Figure 3: Schematic view of an RPC module

Each PAD covers a region of Δη×Δϕ ~ 0.2×0.2. Inside a PAD the trigger is segmented into RoIs, each one covering a region given by the overlap of one η and one ϕ Coincidence Matrix. The Coincidence Matrix is responsible for collecting signals from RPC η and ϕ strips, and performing the coincidence and majority logic. The dimension of a Coincidence Matrix is either Δη×Δϕ ~ 0.2×0.1 for the η CMAs, or Δη×Δϕ ~ 0.1×0.2 for the ϕ CMAs, the dimension of one RoI is Δη×Δϕ ~ 0.1×0.1.

The total number of PADs in the barrel is 832, the total number of RoIs is 1664.

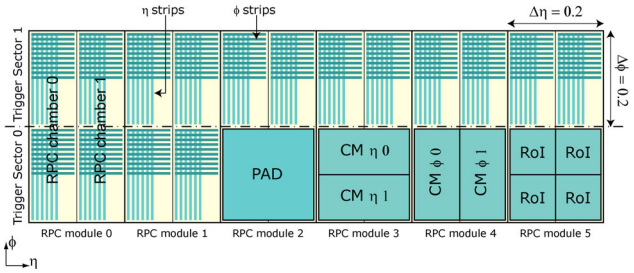

Figure 4: ATLAS Barrel Half Sector

II. HARDWARE IMPLEMENTATION

The trigger slice scheme is shown in Figure 5. Signals coming from the RPC detectors are amplified, discriminated and digitally shaped on-detector. The Amplifier Discriminator Shaper boards, each one containing eight channels, are mounted on the four sides of each chamber module, on one end of the RPC strips.

The level-1 trigger algorithm and data transmission electronics is contained in PAD Boxes mounted on the RPCs. Signals coming from the front-end electronics have to be sent via copper cables to the Coincidence Matrix ASICs (CMA), which have to perform the trigger algorithm [3]. Because of overlapping coincidence windows, a single RPC channel can drive more then one CMA input. For this reason, signals coming from RPC1 and RPC3 stations are sent to dedicated Splitter Boards that can fan-out incoming signals and send the output to the appropriate CMAs. Signals coming from the pivot plane RPC2 are directly connected to the CMAs.

RPC1 and RPC2 signals are sent to the low-p_T CMAs, while RPC3 signals and the output from the low-p_T trigger are sent to the high-p_T CMAs.

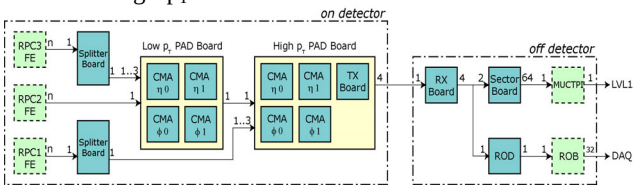

Figure 5: ATLAS Level-1 Barrel Muon Trigger Slice

Four low-p_T CMAs, covering a total region of $\Delta\eta\times\Delta\phi$ ~ 0.2×0.2, are mounted on a low-p_T PAD board, the four high-p_T CMAs are mounted on a high-p_T PAD board. The low-p_T PAD board collects data coming from the four low-p_T CMAs, and sends trigger data to the high-p_T PAD board, which collects low-p_T and high-p_T data and serially sends data off-detector via an optical fibre. The optical receiver, located in the counting room, receives serial data from the optical fibre, and sends them to the Sector Logic board and to the Read-Out Driver.

The on-detector electronics will be mounted on top on the RPC detectors as shown in Figure 6. A Splitter Box contains two or three splitter boards, depending on the required fan-out. In order to reduce the number of interconnections, each couple of ϕ strips in one RPC detector belonging to two adjacent RPC chambers is wire or-ed on detector.

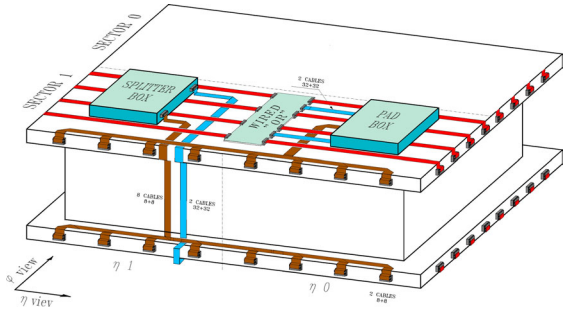

Figure 6: Schematic view of a Barrel Middle RPC station

A. *Coincidence Matrix ASIC*

The CMA is the core of the level-1 trigger logic, its main functions are:

- incoming signal timing alignment;
- input and output signal masking;
- de-clustering algorithm execution;
- majority logic;
- trigger algorithm execution;
- level-1 latency memory data storing;
- readout data formatting, storing and serial transmitting.

A schematic view of the chip internal architecture and its main block division is represented in Figure 7.

The CMA can be programmed to perform either the low-p_T or the high-p_T trigger algorithm. The chip can be used as a η CMA, covering a region $\Delta\eta\times\Delta\phi$ ~ 0.2×0.1, or as a ϕ CMA, covering a region of $\Delta\eta\times\Delta\phi$ ~ 0.1×0.2.

The chip has 2×32 + 2×64 inputs for the front-end signals [4]. In the low-p_T CMAs the 2×32 inputs are connected to the front-end signals, either η strips or ϕ strips, coming from a doublet of the RPC2 pivot plane, while the 2×64 inputs are connected to the signals coming from the RPC1 doublet. For the high-p_T CMAs the first 32 inputs are connected to the output trigger signals coming from the low-p_T PAD board, the second 32 inputs are not used, while the 2×64 inputs are connected to the signals coming from the RPC3 doublet.

The CMA aligns in time the input signals in step of one-eight of a bunch crossing period. For this reason the chip internal working frequency is 320 MHz, eight times the 40 MHz bunch crossing frequency. Input signals can be masked to the zero logic in order to be able to suppress noisy channels and to handle unconnected input signals.

RPC average cluster size is ~1.4, hence input signals are pre-processed and de-clustered in order to sharpen the p_T cut. The maximum cluster size to be processed in the de-clustering logic is programmable.

Processed input signals are sent to the coincidence logic, which performs the coincidence algorithm. The logic is repeated three times, so that three different coincidence windows can be simultaneously applied inside the chip. The three coincidence windows can be independently programmed, thus providing three different muon p_T cuts. Coincidence logic inputs can be masked to "one" logic, to simulate unconnected inputs. A programmable majority logic can be applied to the coincidence algorithm, choosing a 1/4, 2/4, 3/4 or 4/4 plane confirmation. The 32-bit trigger output pattern is then sent to the chip outputs.

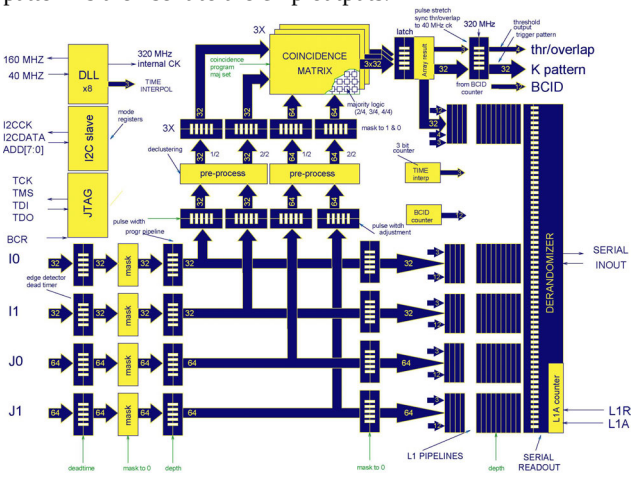

Figure 7: CMA block scheme

The CMA readout logic collects chip input data and trigger output data in a latency memory, used to store events during level-1 latency period [5]. Data corresponding to one event are accepted according to the Level-1 Accept signal arrival time and to the programmed acceptance window time. All other hits are discarded, while level-1 validated data are formatted and sent to de-randomising buffers for the serial readout.

The CMA chip has ~ 300 internal registers programmable via I^2C bus. Single Event Upset detection logic has been implemented for all registers, redundancy logic has been implemented for critical control registers.

CMA design has been realized with a 0.18 µm CMOS technology. The external clock frequency is 40 MHz, the internal working frequency is 40 MHz for register initialisation, 320 MHz for the pipeline and trigger logic, 160 MHz for the readout logic. An internal PLL has been used for clock frequency multiplication. JTAG boundary and scan chain logic has been implemented for test purposes. The CMA has ~ 500.000 basic cells, including ~ 80 kbit of internal memory. Chip area is ~ 20 mm^2, power dissipation is < 1 W.

B. PAD Logic boxes

The first step of the trigger algorithm is performed separately in the η and in the ϕ projections. Four CM boards, each one mounting one CMA, are plugged on one PAD board, which is responsible to collect data coming from two η CMAs and two ϕ CMAs, to elaborate incoming data and to associate muon candidates in the Region-Of-Interest $\Delta\eta\times\Delta\phi \sim 0.1\times0.1$. Globally the PAD logic board covers a region $\Delta\eta\times\Delta\phi \sim 0.2\times0.2$. A dedicated FPGA chip performs the PAD logic. It combines η and ϕ information, selects the higher triggered track in one RoI and solves overlaps inside the PAD.

Timing, trigger and control signals are distributed in the PAD boards from the TTCrx ASIC, which will be mounted on a dedicated plug-in board.

In the low-p_T PAD board, which is mounted on the RPC2 detector, low-p_T trigger result and the associated RoI information is transferred, synchronously at 40 MHz, to the corresponding high-p_T PAD board via copper cables, using LVDS signals. LVDS driver and receiver chips are mounted on the PAD board. The high-p_T PAD board, which is mounted on the RPC3 detector, is similar to the low-p_T one. It performs the high-p_T algorithm, collects the overall result for both the low-p_T and the high-p_T trigger and sends the readout data to the Read Out Driver via optical link. The custom built optical link is mounted on a dedicated board to be plugged on the high-p_T PAD board.

The Embedded Local Monitor Board, a general-purpose CANBUS plug-in board (CERN & Nikhef project) is used in both the PAD boards for JTAG and I^2C chip initialisation and for local control and monitoring.

Each PAD board is enclosed in a liquid cooled PAD Box that will be mounted on the RPC detector.

C. Off-detector electronics

The optical link board in the high-p_T PAD box transmits the trigger and readout data to the receiver board located in the USA 15 counting room. One Receiver board receives the inputs from four optical links and sends the output to the Sector Logic board and to the Read Out Driver board.

Proposed crate for containing Receiver boards, ROD boards and Sector Logic boards is 6U VME 64X format. A single crate contains 8 Receiver boards, 4 Sector Logic boards, 2 ROD boards and a ROD controller, as shown in Figure 8.

The Sector Logic covers a region $\Delta\eta\times\Delta\phi = 1.0\times0.2$, each SL board receives data from 7 high-p_T PAD logic boards in the small sectors and 6 high-p_T PAD logic boards in the large sectors [6]. It maps the signals coming from the Tile Calorimeter trigger towers to the triggered muons, it performs outer plane confirmation for all the three low-p_T thresholds, it solves the η overlap inside the sector, it selects the two higher thresholds triggered in the sector, associating with each muon a region of interest $\Delta\eta\times\Delta\phi \sim 1.0\times0.1$.

The outputs from the Sector Logic boards are sent to the Muon Central Trigger Processor Interface via parallel differential LVDS links.

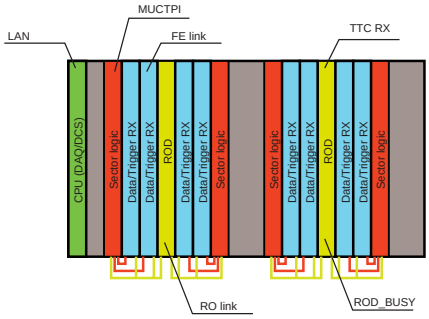

Figure 8: Off-detector crate with the contained VME cards

III. Radiation Assurance

Radiation effects for the level-1 muon trigger electronics have to be taken into account, since on-detector electronics will be mounted on the RPC detectors. Radiation levels for the RPCs have been simulated, Figure 9 and Figure 10 show the simulated total dose and the > 20 MeV neutron distribution inside the experiment.

Pre-selection and qualification of electronic components have to be made following the ATLAS Standard Test Methods [7]. Components have to be qualified for Single Event Effects and for Total Ionising Dose.

The ATLAS Radiation Tolerance Criteria for TID is: $RTC_{tid} = SRL_{tid} \cdot SF_{sim} \cdot SF_{ldr} \cdot SF_{lot} \cdot 10y$, where the Safety Factors depend on simulation accuracy, low dose rate effects and components lot differences. The Simulated Radiation Levels for the RPC are shown in Table 1. The resulting RTC_{tid} is of the order of 1 krad, depending on the electronics component type.

For Single Event Upsets the foreseen soft SEU rate is: $SEU_f = (\text{soft } SEU_m / ARL) \cdot (SRL_{see} / 10y) \cdot SF_{sim}$, where SEU_m is the number of measured soft SEU during test, and the Applied Radiation Level is the integrated hadrons flux received by the tested component.

SEE and TID pre-selection test have been completed for almost all the electronics components that will be mounted on the RPCs. All tested components successfully passed the radiation tolerance criteria. No Single Event Latchup was observed, and the foreseen soft SEU frequency for the components that had SEU is low enough for not compromising trigger functionality. All tested components functionality was not altered after the maximum foreseen total dose.

A few components have still to be tested. Final component pre-selection is supposed to be completed during 2002.

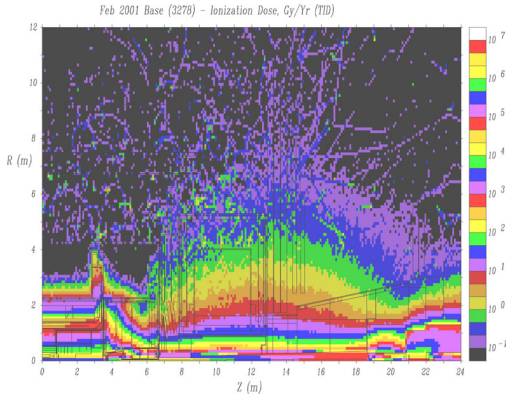

Figure 9: ATLAS Simulated Total Ionisation Dose

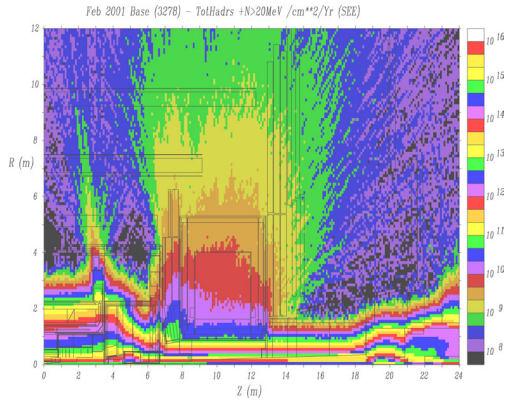

Figure 10: ATLAS Simulated Hadrons Distribution

Table 1: ATLAS Barrel RPC Radiation Levels

	SIMULATED RADIATION LEVEL		
	SRL_{tid} [$Gy \cdot 10y^{-1}$]	SRL_{niel} [1 MeV $n \cdot cm^{-2} \cdot 10y^{-1}$]	SRL_{see} [> 20 MeV $h \cdot cm^{-2} \cdot 10y^{-1}$]
BMF	3.02	$2.49 \cdot 10^{10}$	$4.69 \cdot 10^{9}$
BML	3.04	$2.82 \cdot 10^{10}$	$5.65 \cdot 10^{9}$
BMS	3.03	$2.50 \cdot 10^{10}$	$4.73 \cdot 10^{9}$
BOF	1.19	$2.14 \cdot 10^{10}$	$4.08 \cdot 10^{9}$
BOL	1.33	$2.20 \cdot 10^{10}$	$4.21 \cdot 10^{9}$
BOS	1.26	$2.10 \cdot 10^{10}$	$4.10 \cdot 10^{9}$

IV. CONCLUSIONS

All prototype components produced up to now successfully passed lab tests. Coincidence Matrix ASIC is missing to complete the Trigger Slice, and is planned to be available by the end of 2001. Further test on RPC chambers on cosmic ray is planned before having the CMA.

A C++ high-level simulation code for the level-1 electronics is being developed for trigger functionality confirmation. CMA VHDL simulation has been compared with C++ simulation, giving good crosscheck results.

Irradiation test for components pre-selection and qualification are planned to be finished before the end of 2002. First slice test will be performed during next year.

V. REFERENCES

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[3] E. Petrolo, A. Salamon, R. Vari, S. Veneziano *Barrel LVL1 Muon Trigger Coincidence Matrix ASIC User Requirement Document* (ATL-COM-DAQ-2000-050)

[4] E. Petrolo, A. Salamon, R. Vari, S. Veneziano *CMA ASIC Hardware Requirement document* (ATL-COM-DAQ-2001-005)

[5] E. Petrolo, A. Salamon, R. Vari, S. Veneziano *Readout Requirements in the Level-1 Muon Trigger Coincidence Matrix ASIC* (ATL-COM-DAQ-2000-052)

[6] V. Bocci, A. Di Mattia, E. Petrolo, A. Salamon, R. Vari, S.Veneziano *The ATLAS LVL1 Muon Barrel Sector Logic demonstrator simulation and implementation* (ATL-COM-DAQ-2000-051)

[7] ATLAS Policy in Radiation Tolerant Electronics http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/radhard.htm