The Sector Logic demonstrator
of the Level-1 Muon Barrel Trigger
of the ATLAS Experiment

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Abstract

The ATLAS Barrel Level-1 muon trigger processes hit information from the RPC detector, identifying candidate muon tracks and assigning them to a programmable p_T range and to a unique bunch crossing number.

The on-detector electronics reduces the information from about 350k channels to about 400 32-bit data words sent via optical fiber to the so-called Sector Logic boards.

The design and performance of the Sector Logic demonstrator, based on commercial and custom modules and firmware is presented, together with functionality and integration tests.

I. THE ATLAS FIRST LEVEL MUON TRIGGER IN THE BARREL

The ATLAS first level muon trigger in the barrel is based on fast geometric coincidences between three different planes of RPC trigger stations in the muon spectrometer. The trigger chambers are arranged in three different shells concentric with the beam line, each chamber has four planes of strips (two along η and two along ϕ) in order to reduce the fake trigger rate due to the cavern background. For the same reason the algorithm is performed both in η and in ϕ.

The trigger algorithm is executed for two separate p_T thresholds.

- For the low-p_T threshold, if a strip is hit in the pivot plane (RPC2) the trigger processor searches for an hit in the first trigger chamber plane (RPC1) looking inside a window whose axis is on the line that connects the hit point in RPC2 with the nominal interaction point, whose vertex is on the RPC2 plane and whose opening gives the cut on p_T. A valid trigger is generated if RPC1 and RPC2 are hit in coincidence.

- For the high-p_T threshold, if a valid trigger has been generated by the low-p_T algorithm, the processor searches for an hit in the third plane RPC3, searching for a coincidence between the trigger pattern given by the low-p_T algorithm and the hit on the RPC3 trigger station.

The schematic of the trigger principle is depicted in Figure 1. The trigger processor is composed of various modules.

- The low-p_T Coincidence Matrix ASICs (CMAs) are mounted on the RPC2 trigger chambers and perform the fast coincidence between the signals coming from RPC1 and RPC2. Each CM η board covers a region Δη x Δϕ =
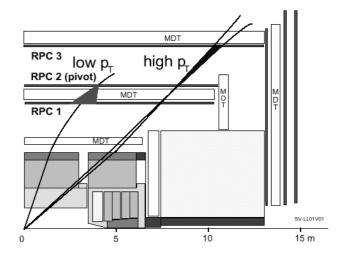

Figure 1: Trigger principle for the ATLAS first level muon trigger in the barrel. The selection is performed using three dedicated trigger chambers. For the low-p_T trigger if an hit is found in RPC2, an hit is searched for in the RPC1 trigger station inside a road defined by the p_T cut. The same algorithm is applied for the high p_T threshold using the low-p_T trigger output and the RPC3 trigger station.

0.1 x 0.2, while the CM ϕ board covers a region Δη x Δϕ = 0.2 x 0.1.

- The low-p_T Pad Logic Boards are mounted on RPC2 and collect the data from four coincidence matrices from a region Δη x Δϕ = 0.2 x 0.2. The low-p_T Pad board generates the low-p_T trigger information and sends it to the high-p_T trigger boards.

- The high-p_T Coincidence Matrix ASICs are mounted on the RPC3 trigger chambers and perform the fast coincidence between the signals coming from the low-p_T trigger and the RPC3 trigger station. The CM η board covers a region Δη x Δϕ = 0.1 x 0.2, while the CM ϕ board covers a region Δη x Δϕ = 0.2 x 0.1.

- The high-p_T Pad Logic Boards are mounted on RPC3 and collect the data from the low-p_T board and from four high-p_T coincidence matrix from a region Δη x Δϕ = 0.2 x 0.2. The high-p_T Pad board merges the bending (η) and non bending (ϕ) views, selects the muon with the highest threshold, associates the muon with a Region of Interest Δη x Δϕ = 0.1 x 0.1 and with a unique bunch crossing number. Trigger informations are sent to the Sector Logic board.

- The Sector Logic boards are located in the underground counting room. Each Sector Logic board covers a region Δη x Δϕ = 1.0 x 0.4, receives data from

up to 7 high-p_T pad logic boards and from 32 Tile Calorimeter trigger towers. The output of the Sector Logic board is sent to the Muon Central Trigger Processor Interface (MUCTPI).

- The MUCTPI elaborates the data from the Sector Logic boards and sends its output to the Central Trigger Processor.

In Figure 2 is reported a trigger slice from the RPC Front End electronics to the Muon Central Trigger Processor Interface and to the Read Out Buffer.
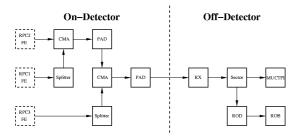

On−Detector   **Off−Detector**

Figure 2: Trigger slice from the RPC Front End electronics to the Muon Central Trigger Processor Interface and to the Read Out Buffers.

II. SECTOR LOGIC FUNCTIONS

Each Sector Logic board collects information from up to 7 high p_T pad logic boards and form 32 Tile Calorimeter trigger towers. 64 Sector Logic boards are foreseen in the first level muon triggere in the barrel. Each Sector Logic board performs various functions.

- Checks the correct timing of the input data. If some problem is found a flag is sent to the MUCTPI.
- Performs the Tile Calorimeter coincidence. A muon candidate is accepted only if an energy deposit is found in a region of the Tile Calorimeter associated to the region of the muon spectrometer in which the muon candidate has been detected. This option will be used in case of high background levels and is fully programmable.
- Performs the low-p_T filter. For each low-p_T muon coming from one of the input Pads it checks if an hit is found in the RPC3 trigger station. This check is performed at the sector level. This option is also to be used in case of high background levels and is fully programmable.
- Solves η overlap between different Pads inside the sector and flags all the muons crossing a region overlapping with a neighbouring sector (this overlap is solved by the MUCTPI).
- Selects the two muons with the two highest thresholds in the sector and associates each muon with a Region of Interest $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ and with a unique bunch crossing number. If more than two muon candidates are found, the Sector Logic flags this condition to the Muon Central Trigger Processor Interface.

III. SECTOR LOGIC HARDWARE IMPLEMENTATION

The Sector Logic is implemented with a pipeline processor working synchronously with the 40 MHz LHC clock.

Each Sector Logic chip receives the input from up to 8 Pad Logic boards (8 x 12 bit @ 40 MHz) and from 32 Tile Calorimeter trigger towers (32 bit @ 40 MHz) and sends the output synchronously to the Muon Central Trigger Processor Interface (32 bit @ 40 MHz). A spare Pad input has been added to the maximum number of 7 Pads input foreseen at the current time. The low-p_T filter and the Tile Calorimeter coincidence are fully programmable depending on the content of four configuration registers.

Sector Logic processing is perfomed in five pipeline steps. Each pipeline block consists of an input D flip-flop register (containing the data from up to 8 Pads and from 32 Tile Calorimeter trigger towers and the current result of the trigger algorithm) followed by the combinatorial logic implementing the desired functions on the current data. A block dagram of the Sector Logic chip architecture is reported in Figure 3.
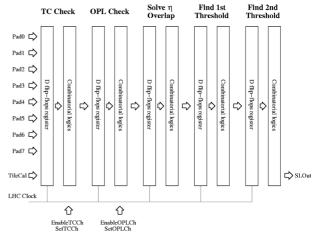

Figure 3: Block diagram of the architecture of the Sector Logic chip. The Sector Logic algorithm is implemented with a five steps pipeline, each step of the pipeline implementing one task of the algorithm.

We implemented the Sector Logic functionalities in an FPGA. We used the EPF10K130E-2 of the ALTERA FLEX 10KE family as target device.

A. Tile Calorimeter confirmation

The first step of the Sector Logic pipeline is the Tile Calorimeter confirmation block. This block maps the input coming from the pads to the input from the Tile Cal. A muon candidate is accepted only if a corresponding track is found in the expected region of the Tile Calorimeter. This option is fully programmable for each threshold and thus can also be disabled.

The Tile Calorimeter check can be programmed with two arrays EnTCCh(0:7,1:6) and SetTCCh(0:7,1:6,0:31) stored in the Sector Logic configuration registers. The Tile Calorimeter coincidence is enabled for all the muons crossing the i-th Pad with the j-th threshold if EnTCCh(i,j) is set to 1.

In the same way, for each muon passing in the i-th Pad with the j-th threshold, an energy deposit is searched in the k-th Tile Calorimeter trigger tower if SetTCCh(i,j,k) is set to1.
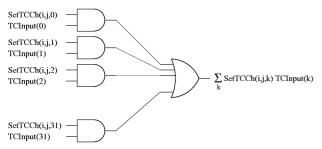

Figure 4: Tile Calorimeter coincidence implementation. For a given Pad and a given threshold a muon candidate is accepted if one hit is found in one of the corresponding Tile Calorimeter trigger towers.

The schematic of the Tile Calorimeter coincidence is reported in Figure 4. This coincidence is executed in parallel 48 times, for each Pad and for each threshold.

B. Outer Plane (OPL) low-p_T filter

The second step of the Sector Logic pipeline performs a filter on low-p_T muons. A muon with one of the three low thresholds is confirmed only if an hit is found in the outer plane of the spectrometer (RPC3 trigger chambers). This coincidence is performed at the sector level. This option is fully programmable for each threshold and can also be disabled.

The OPL check can be programmed with two arrays EnOPLCh(0:7,1:3) and SetOPLCh(0:7,1:3,0:7) stored in the Sector Logic configuration registers. The OPL coincidence is enabled for all the muons crossing the i-th Pad with the j-th threshold if EnOPLCh(i,j) is set to 1. In the same way, for each muon passing in the i-th Pad with the j-th threshold, an hit is searched in the k-th Pad of the RPC3 trigger station if SetOPLCh(i,j,k) is set to1.
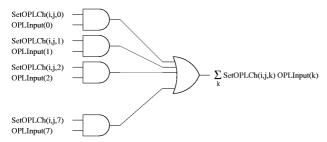

Figure 5: Low-p_T filter implementation. For a given Pad and a given low-p_T threshold a muon candidate is accepted if one hit is found in one of the corresponding RPC3 Pads.

The schematic of the low-pT filter implementation is reported in Figure 5. This coincidence is executed in parallel 24 times, for each Pad and for each low-pT threshold.

C. Solve η overlap

The η solving algorithm is aimed at avoiding to double count a muon passing in a region of overlap between two different chambers. The Sector Logic overlap solving algorithm looks at the data from the various Pads and if it finds two neighboring pads in which the same track has passed, discards one of the two tracks.

The η overlap solving algorithm is performed in various combinatorial steps:

- a check on all the overlap bits is performed; if a pad with the overlap bit set to 1 and the threshold set to 0 (anomalous condition) is found, the overlap bit is reset;
- the overlap solving algorithm is performed first on neighbouring Pads 0 and 1, 2 and 3, 4 and 5, 6 and 7 (even overlap solving);
- the same solving algorithm is performed next on neighbouring Pads 1 and 2, 3 and 4, 5 and 6 (odd overlap solving).

D. Find 1 st track

The fourth block of the pipeline selects the track with the highest threshold and associates to the muon candidate trigger informations. If there is more than one triggered track with the same threshold the track with lower pad number (lower η) is selected.

The 1st highest threshold selection algorithm is performed in various steps:

- the highest threshold associated to each Pad is compared with the highest threshold associated to all the other pads. The output of these comparison are ANDed. Eight bits indicating if the pad's triggered threshold is greater or equal than the thresholds associated to all the other pads are produced at the output of this block.

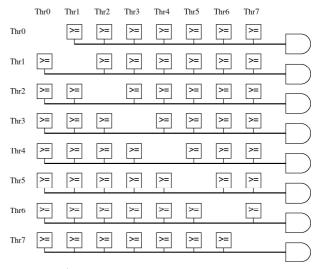A schematic of the highest threshold selection algorithm is reported in Figure 6.

Figure 6: 1st highest threshold search implementation. For each Pad the muon candidate threshold is compared with the thresholds of all the other Pads and the comparison output are ANDed for each Pad.

The output from the comparison block is sent in parallel to two different blocks:

- the first block is composed of an encoder and a data filter which transmit to the next step of the pipeline all the Pads data except the data from the Pad corresponding to the highest threshold (to avoid double counting of the same highest threshold);
- the second block is composed of a priority encoder and a selector which sends to the Sector Logic output pipeline the data corresponding to the Pad with the highest threshold.

E. Find 2nd track

This step of the Sector Logic pipeline is identical to the previous step, and is performed on the data from all the Pads excepted the Pad with the highest threshold (which has been reset to 0). The result of the search is synchronized with the output from the previous step and is written in the part of the SL output frame dedicated to the 2nd threshold. A flag is written in the output data pattern if more than two tracks were found in the sector.

IV. THE SECTOR LOGIC DEMONSTRATOR

F. The Multifunction Computing Core

In order to demonstrate the functionalities of our implementation we used the Multi Function Computing Core MFCC 8441 commercial board from CES. This commercial hardware has been proven to be reliable and efficient solution for the purposes of our tests.

The MFCC 8441 is a PCI Mezzanine Card which can be plugged on a RIO2 VME board also from CES.

The MFCC board is composed of:

- a POWER PC CPU running the Sector Logic C test control program;
- a PPC-PCI bridge implemented with an Altera FPGA of the FLEX 10KE family;
- on board SDRAM which can be used for demanding DAQ applications;
- a Front-End FPGA which is full user programmable; the Sector Logic VHDL code is loaded in this FPGA, the VHDL code needed to interface the Front-End FPGA with the PPC bus, with the FE adaptor, with the SDRAM and with the EPROM is produced by CES;
- a Front-End adaptor which must be designed for the specific application;
- a flash EPROM storing the firmware for the PPC-PCI bridge and for the FE FPGA; the EPROM can be programmed with a dedicated download cable and from the on-board PPC.

G. The test setup

In order to use the Sector Logic VHDL code with the MFCC test board an interface with the CES VHDL code has

been created. The architecture of this interface is depicted in Figure 7.

The Sector Logic Core is interfaced with an Input Block constituted of 32-bit wide 32-bit deep RAMs, with a Parameter Block in which are stored the Sector Logic Initialization registers and the control registers and with the Output Block constituted of a 32-bit FIFO.
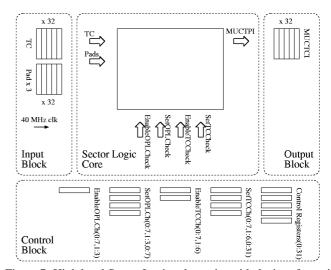

Figure 7: High level Sector Logic schematics with the interface with the test board. The Sector Logic core receives the input from the Input Block, the configuration parameters from the the Parameters Blobk and sends its output to the Output Blobk. All the registers in the Input, Parameters and Output Bloks are accessible via the MFCC Power PC bus.

A test session is performed in the following steps:

- the Sector Logic parameters are loaded in the initialization registers;
- the inputs are loaded by the PPC in the 32-bit internal FIFOs;
- a series of 40 MHz clock cycles is applied, it is also possible to perform an infinite loop on the data loaded in the input RAM (this feature has been used in the Sector Logic MUCTPI integration tests);
- the data are elaborated by the FE FPGA which has been programmed with the Sector Logic demonstrator code;
- the output data are sent both to the FE Adaptor and to the output FIFO; the data stored in the output FIFOs can be read by the PPC and analized and checked off-line, the data at the output of the FE Adaptor can be analized with the scope or sent to the MUCTPI.

H. MFCC Front End adaptor card

The Frontend Adaptor card has been designed to translate the 32 Sector Logic output bit from the FE FPGA to suitable LVDS logic levels to be sent along a 10 meters 40 MHz parallel cable to the MUCTPI.

In Figure 8 is reported a photo of the MFCC with the MUCTPI interface card.
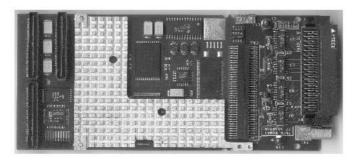
Figure 8: Layout of the MFCC with the FE adaptor card translating the MFCC Sector Logic output to LVDS logic levels used to interface the Sector Logic demonstrator with the MUCTPI prototype.

V. Sector Logic tests

Two kind of thests were performed to validate and test our design: off-line logic tests and integration tests with the MUCTPI prototype.

I. Off-line logic tests

The input data from Pads and from Tile Calorimeter trigger towers were loaded in the input RAM, elaborated and read from the output FIFO. The output data were checked with a C++ Sector Logic simulation program. This C++ code will be inserted in the official first level muon trigger simulation program.

J. Integration tests with the MUCTPI

The Sector Logic demonstrator and the MUCTPI prototype were connected with a 10 meters 32 LVDS logic levels transmission cable. The Sector Logic and the MUCTPI run with the same 40 MHz LHC clock, but the two clock signals are not required to be in phase. All the Sector Logic output data are assumed to be in phase. The data are sampled on the falling edge of the MUCTPI clock signal.

Theree kind of tests and measurements were performed.

- Phase measurement. In order to allow a correct sampling the phase spread of the changing edge of the Sector Logic output data must be low. The phase spread of a given bit at the output of the MUCTPI has been measured with a TDC and a RMS less than 1 ns was found.

- After the phase spread measurement has been performed, a window sampling depth measurement were performed. A fixed sequence of 27 input patterns were loaded in the input RAMs and an infinite test loop on the input data were started. The length of the pattern was chosen in order to be a submultiple of the number of BCs in an orbit. The data at the input of the MUCTPI are sampled at a given BC in the orbit and so the MUCTPI receives always the same known input data from the Sector Logic. The phase of the sampling edge was moved by 1 ns steps inside the 25 ns clock period corresponding to the chosen BC and the sampled data are checked. The width of the allowed sampling window was found to be 19 ns over 25 ns.

- Data integrity check. Correct data transmission was checked over a one night run and no error was found.

VI. Conclusions

The Sector Logic demonstrator has been developed using a commercial board, the PCI Mezzanine Card MFCC 8441 from CES with dedicated firmware running on FPGA.

A custom FE Adaptor Card has been designed to connect the Sector Logic demonstrator with the Muon Central Trigger Processor Interface.

The design has been checked with the official Sector Loigc C++ simulation program.

Various kind of tests were performed to validate the design. The performance of the Sector Logic demonstrator are adequate for the 40 MHz operation and maximum latency of 125 ns.

This work has proven that the use of commercial hardware is a valid solution during the first part of the development of custom boards, because it reduces the demonstrator development time and gives the designer good support during the test phase.

The first Sector Logic VME board prototype is currently been designed on the basis of the present demonstrator.

VII. Acknowledgments

VIII. References

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