Design of ladder *EndCap* electronics for the ALICE ITS SSD

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Abstract

The design of the control electronics of the front-end of the ALICE SSD is described. This front-end will be built with the HAL25 (LEPSI) chip. The controls are placed in the ladder *EndCap*. The main *EndCap* functions are; power regulation and latch-up protection for the front-end, controlling the local JTAG bus, distribution of incoming control signals for the front-end and buffering of the outgoing analogue detector data. The system uses AC coupled signal transfer for double-sided detector readout electronics.
Due to radiation-, power-, and space requirements, two ASIC's are under development, one for analogue buffering and one with all other functions combined.

I. INTRODUCTION

For the control- and readout functions for the ALICE **S**ilicon **S**trip **D**etector (SSD) of the **I**nner **T**racker **S**ystem (ITS)[5], additional electronics is needed between the Data acquisition and the front-end modules. The SSD consists of 2 layers of ladders, the inner with 34 and the outer with 38 ladders. The inner ladders contain 23 modules and the outer 26. The detector modules will be connected to the DAQ- & Control system via *EndCap* units mounted at the end of each side of the ladder via Kapton™ cables (Figure 1). So one *EndCap* controls ½ a ladder and we need 144 *EndCap's* in total. The available space is ~ 70x70x45 mm for one unit.

The limited available space requires a dense design, which immediately adds the requirement for low power. In addition, the volume of the cabling should be kept as low as possible. Therefore serializing and multiplexing of data and the use of low-mass cables is necessary. The latter requires regeneration of signals in order to guarantee a proper quality at the front-end.

The SSD is based on Double Sided Detectors with 768 strips on each side. The detectors will be read out by the HAL25 (Hardened ALice128 in .25µCMOS) front-end chip developed by LEPSI/Ires Strasbourg. This chip contains 128 analogue channels with preamp and shaper. An analogue multiplexer provides a serial readout. All bias voltages and currents are programmable via internal DAC's and the chip has binary controls for readout, test and status check functions. These functions can be addressed via a serial bus that uses the JTAG protocol.

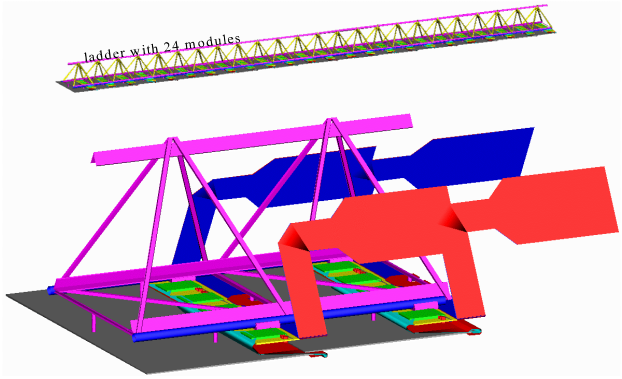

Figure 1 Two modules with cable on a ladder.

Because double-sided detectors are used, the readout electronics on both sides operate at a different potential (detector bias max. 100V). To avoid ADC- and control modules to operate at these bias potentials, all signals will be AC coupled to the corresponding voltage level. In addition, the analogue readout data will be AC coupled to a multiplexer/buffer, which is able to drive the differential signal to ADC modules (over 25m @ 10MHz). The front-end chips of the detector modules are readout successively; the P- and N side of one detector module occupy one ADC channel.

The required low voltage power for the front-end chips (2.5V) of the P- and N-side is regulated inside the *EndCap*. This circuit not only provides the latch-up protection for the front-end but also for the control electronics and buffers in the *EndCap* itself.

Since the front-end electronics is controlled via the JTAG bus, the bus is also used to control and monitor the *EndCap* functions. Errors like latch-up can be detected and appropriate action can now be taken. Defect front-end chips can be disabled and can be put in "by-pass" mode. This information is available for the DAQ system. During the assembly and test phase of the *EndCap*, the JTAG bus will be used to test interconnections inside the module during the production.

The *EndCap* will communicate with the **F**ront-**E**nd **R**ead **O**ut **M**odule (FEROM) placed at a 25m distance from the detector. LVDS levels are used to reduce interference between the signals and the environment. Inside the *EndCap*, only the JTAG signals will be carried out with single ended CMOS levels (2.5V).

A. Radiation Environment

In the initial phase of the design, no clear numbers were available for the expected radiation levels inside the SSD area of the ITS. The Front-end would be designed in 1.2µm CMOS and the *EndCap* would consist of commercial components.

Radiation studies showed that **S**ingle **E**vent **L**atch-up (SEL) would occur once every 5 minutes in these SSD front-end chips [1]. For this reason it was decided that a latch-up protection circuit must be included in the power supply. The supply circuit itself must also be insensitive for SEL. Due to the uncertainty of the expected dose levels and the expected SEL frequency at that time, the step was made to switch to 0.25µ CMOS with the use of radiation tolerant design techniques to improve the susceptibility for latch-up and total dose irradiation damage. Now all SSD electronics inside the detector volume is designed using a 0.25µ CMOS process.

Radiation calculations [2] predict max 100Gy (10krad) total dose and $4*10^{11}$ neutrons/cm^2 1Mev equivalent over 10 years. With the use of a 0.25µm CMOS process, the design can be made with an acceptable susceptibility for radiation.

II. FUNCTIONALITY

The overall functionality is that the *EndCap* is the interface for and distributor of the control and data signals between the detector modules and the Data acquisition 25 m further on. We can classify four main functions:

- Power control and protection
- Signal buffering and coupling
- Readout Control
- JTAG detector control and monitoring

A. Power Control

By nature, the front-end chips need burnout protection for SEL. This means that if the supply current reaches a specified level, the power of the corresponding *hybrid* must be switched off. Of course, the other electronics in the *EndCap* needs the same protection. For that reason, the ASIC's inside the *EndCap* will receive their power from an identical circuit as the hybrids. The supply itself must be insensitive for SEL. The output voltage is programmable and the supply can be switched on/off via the JTAG bus. A local voltage reference defines the proper value for the output voltage. The status as well as the output voltage can be monitored via the control bus. If a latch-up or other error occurs, an OR-ed error signal of all supplies in the *EndCap* will notify the DCS immediately. The DCS can readout the status and can find out which supply (hybrid of *EndCap* control) is switched off. The power supplies provide a power on reset for the front-end chips as well as for the local controllers and coupler circuits.

The *EndCap* has separated power for P-side, N-side, and Interface electronics at ground potential.

B. Buffering and coupling

All signals will cross the detector bias potentials once (Figure 4). This means that after the signals are at the right bias potential, the local bus in the *EndCap* and the drivers work at this potential. All connections to the outside of the detector volume are at ground potential. Since all signals cover a distance of ~25m, they have to be regenerated before being send to the front-end chips. After these receivers, the signals are coupled (AC) to the corresponding bias potential.

In case of a SEL on a hybrid that must be reset, the outputs of the signal drivers to the hybrids must go in high impedance state so they are not able to conduct any current to the front-end.

The output signals of the *EndCap* are 1 error signal and 14 analogue outputs. The analogue output multiplexer (Figure 3) makes it possible to readout a P- and N-side hybrid successively. This results in one analogue signal per module. In order to create a signal with one polarity, one of the two signals is inverted (Figure 2).

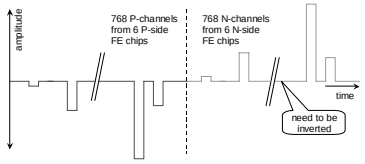

Figure 2 Simplified Analogue Output

C. Readout control

The serial readout of the front-end chips is based on token passing. Once the token has entered the chip, the 128 channels will put its sampled voltage on the output at each 10MHz clock cycle. The front-end chip needs some additional clock cycles before and after the readout for token handling.

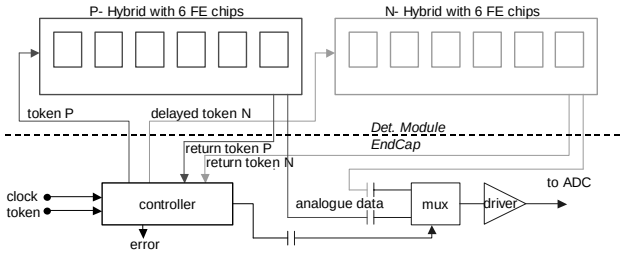

Figure 3 Token Readout principle

The readout is organised in a way that clock and token are being send to the Detector, and *all modules* are read out in parallel. One detector module consists of one P- and one N-side detector hybrid with 6 front-end chips (HAL25). *One* module connects to *one* ADC input, so the two signals are multiplexed to one line at ground potential (Figure 3). This means that halfway the readout a multiplexer has to switch, and that the two hybrids receive their tokens successively. The switching and token handling will be done in the *EndCap*, via a programmable token delay. It is programmable because a broken front-end chip requires a decrease of the number of clock cycles for the readout. A "bypass" capability

will maintain the token passing for the readout. Once the last chip in the chain is read out, the token is passed to the controller again. It checks if it arrived at the correct time. If not, an error signal will be generated, indicating a problem in the readout sequence.

In case of a 'Fast Clear" during readout, all delays will be reset and the event can be cleared from all buffers. Within a few clock cycles, the system is ready for a new readout cycle.

D. JTAG control and monitoring

The control of the front-end chip goes via the JTAG bus. Therefore, it is obvious that it should also be used to control and monitor the *EndCap*. An important function in the *EndCap* is that the power will switch off in case of a SEL in a hybrid. The controller looks after an uninterrupted JTAG chain. The controller restores the original chain after the hybrid power is switched on again.

The *EndCap* JTAG logic has registers for the power supply voltage DAC's, readout control, the ADC to monitor temperature and detector bias current, and for Boundary Scan interconnection tests.

III. *ENDCAP* IMPLEMENTATION

Since the Detector Control and Data Acquisition electronics are at ground potential, the interface connections work on the same level. Therefore, the signals should cross the bias levels inside the *EndCap* before they are connected to the corresponding detector side.

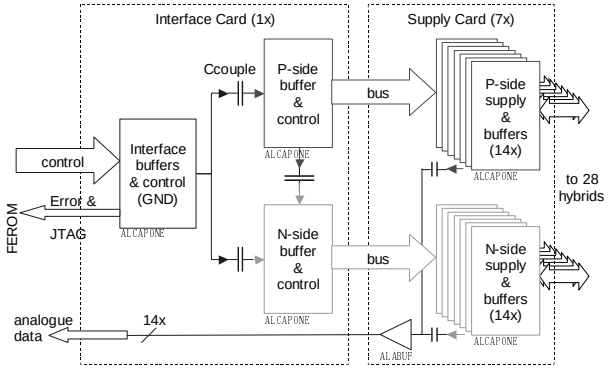

Figure 4 *EndCap* architecture

To minimise space and power, AC coupling has been chosen to cross the bias potentials for differential and single ended digital signals. The analogue output that is clocked out at 10MHz is also carried out with differential AC coupling. This concept has been proven in the HERMES Lambda-wheels (HERA, DESY).

As shown in Figure 4, the *EndCap* is built out of 8 PCB's, 1 InterfaceCard, and 7 SupplyCard's. These PCB's will be placed on a back plane using miniature connectors. Kapton™ cables (max 70cm) connect each SupplyCard to 4 hybrids on the ladders. The FEROM is connected to a patch panel using "standard" cables and from here to the InterfaceCard with a Kapton™ cable.

All functions of the *EndCap* electronics are being integrated into two ASIC's; the control chip "**AL**ice **C**ontrol **A**nd **PO**wer **NE**xus" named ALCAPONE, and the analogue buffer "**AL**ice **A**nalogue **BUF**fer" named ALABUF. The ALCAPONE chip integrates the control- and power functions plus the LVDS and CMOS buffers that are used for the AC coupling of the digital signals (Figure 6). The multiplexer and analogue buffers that send the serial data to the ADC are placed in the second chip. The InterfaceCard houses 3 ALCAPONE chips (Figure 4), one at ground potential for the interface and two at the detector bias levels after the AC coupling. By using the same IC process for the ASIC's as the front-end chip, the signal levels are fully compatible.

A. The control chip, ALCAPONE

This ASIC (Figure 5) has the following main features:

- LVDS & CMOS (AC) buffering
- JTAG control of readout, monitor and power functions
- Power supply and reference.

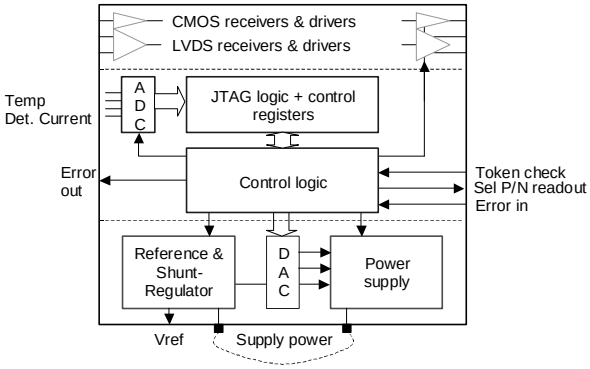

Figure 5 Block diagram of the ALCAPONE ASIC

For the receivers "standard" cells are used. The drivers have an additional tri-state output capability. The positive feedback (Figure 6) of the receiver output creates a latch function after the AC coupling. An additional reset circuit for the latch ensures that the correct signal polarity after power on can be determined.

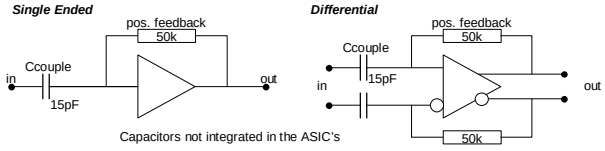

Figure 6 Digital AC coupling with receivers

The design of the JTAG interface is according to the IEEE standard. Additional is a parity check for all bits in the registers to detect a **S**ingle **E**vent **U**pset. Control- and status registers exist to check for power- and readout errors. Errors can be masked in case of real defects.

The chip is designed in such a way that it can be used as *EndCap* interface, AC coupler, and hybrid driver. Hence, the ALCAPONE chips exist with 3 different functions in the *EndCap* on 2 different types of PCB's.

B. *Power supply*

The power supply has two main parts, a regulator with voltage reference, and the supply circuit. Since the incoming power voltage is about 3V, it needs to be regulated down to 2.5V. The Bandgap- and the supply circuit voltage may not exceed this value. This is realised with a shunt regulator in parallel with the Bandgap reference.

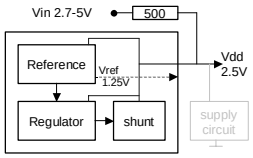

Figure 7 Shunt regulator diagram

Now that the primary power voltage is generated, the supply circuit (Figure 8) can be turned on. It uses a start-up circuit that includes a timer that switches off the current limit during the first 250µs (charge up of load capacitance). It also generates a power-on reset signal to clear the error latch.

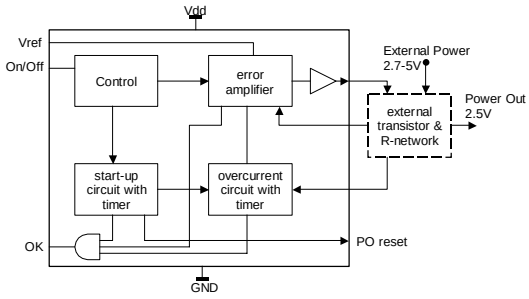

Figure 8 Block diagram of the power supply

An external sense resistor (75mΩ for 320mA) defines the current limit. In case of over current, the over current timer will delay the signal for 25µs before the output is switched off. Other external components (7 x Res., 2 x Trans.) are used for current- and voltage feedback and power regulation. The transistors are necessary because the externally delivered voltage (>2.7 V) is higher than the maximum allowed voltage for the used IC process (2.5V). The minimum dropout voltage is 200mV and the maximum output current with the used components is 2A. The current used by the circuit itself is 600µA.

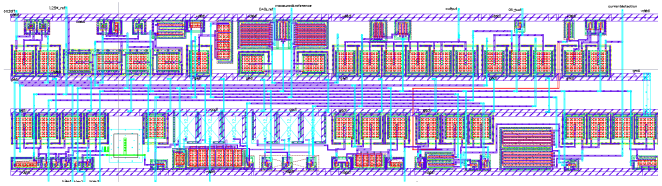

Figure 9 Layout of the supply circuit (280 x 70 µm)

C. *The analogue buffer chip, ALABUF*

The analogue buffer must be able to drive the signal over a 25m distance with 10-bit accuracy in the required range. The range of the front-end chip is 0-13 MIP, but the highest accuracy is required below 5 MIP detector signal. The required linearity below 5 MIP must be better then 1%. Settling time at the output should be max. 20ns. Additional RMS noise < 1mV.

Because a SupplyCard contains the electronics for two detector modules, the ALABUF chip (Figure 10) is equipped with two buffers with analogue multiplexers. The analogue multiplexer (Figure 11) connects the hybrid outputs of one module to the analogue buffer. Between two readout cycles, the outputs are connected to a reference voltage to avoid any voltage drift during this quiet state.

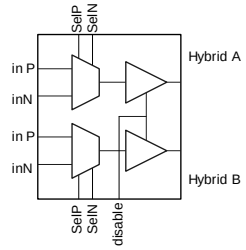

Figure 10 ALABUF ASIC

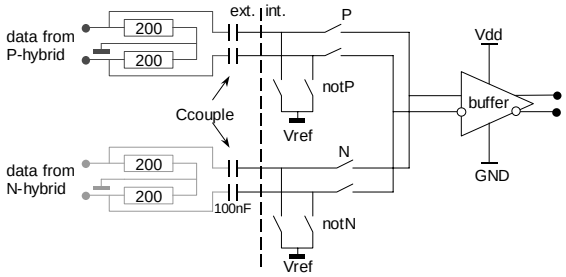

Figure 11 Analogue multiplexer diagram

The OPAMP used in the buffer (Figure 12) is a fully complementary Self-biased CMOS differential amplifier [4]. Additional RC networks have been added for stability of the complete circuit to ensure that some expected capacitive load would not influence the behaviour.

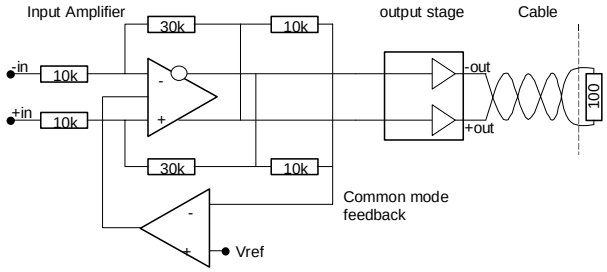

Figure 12 Simplified Analogue buffer schematic

The buffer must amplify the signal from the front-end chip to maximum output range in order to minimise any “pick-up” while being transferred over the cable. The differential input amplifier has an extra feedback OPAMP. This feedback circuit reduces the common-mode error and ensures that the output voltage “zero level” has the value of Vref (½ the supply voltage).

In order to drive a 100Ω cable, the output must be able to drive 20mA for an output voltage of 2V. Therefore, the driver circuit as in Figure 13 is used. This circuit has a gain of 1, so the input amplifier defines the gain of the complete buffer (gain = 2.6). The buffers are provided with a disable function to reduce the power consumption between readouts. Two of these circuits create the differential output.

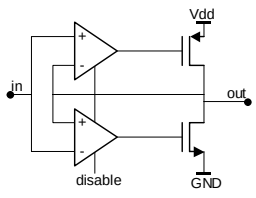

Figure 13 Buffer output stage

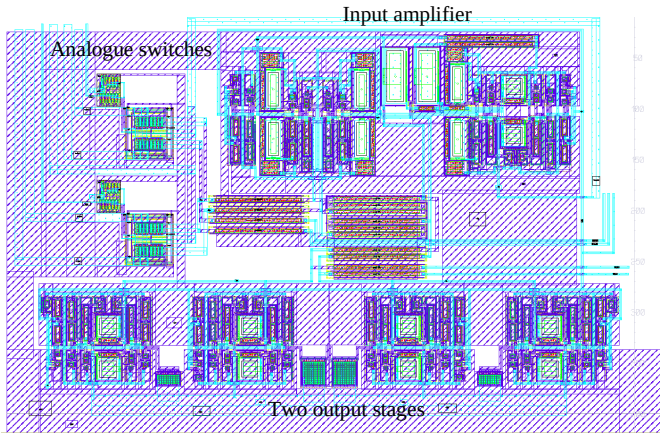

Figure 14 Analogue buffer Layout (600 x 400µm)

D. *InterfaceCard*

On the InterfaceCard, the AC coupling and the control power supplies are located (Figure 4). The *EndCap* receiver's –in one ALCAPONE- are connected (AC) to two buffer ALCAPONE chips. These two chips drive bus lines to the SupplyCard's. The shunt regulators are used only at this Card, to generate the local power for the control electronics.

E. *SupplyCard*

The Hybrid power supplies are placed on the SupplyCard. Each card contains 2 P-side- and 2 N-side supplies (4x ALCAPONE), plus one ALABUF chip at ground potential to drive the two analogue module outputs to the ADC. These ALCAPONE chips are powered from the InterfaceCard.

IV. MECHANICS

Because of the space limitation, the temperature control of the *EndCap* needs extra attention. Therefore, the PCB's will be made of an Aluminium carrier with Kapton™ multi layer PCB's on both sides. At the short sides, the cards have the hybrid cable connectors and at one long side the back plane connector. The other long side is used for a heat bridge to the cooling tubes that are used for cooling the detector modules. The power budget for one *EndCap* is 10W, and simulations and measurements indicate that it is feasible.

V. SIMULATION AND MEASUREMENTS

Irradiation of the transistors of the power supply with 10^{13} neutrons/cm^2 1Mev equivalent shows degradation in β of 60%. The supply can work within specifications after this 25 times higher flux than expected in 10 years of operation.

First measurements of the buffer shows a difference in gain, exp. 2.6, measured 2.3. The circuit is not stable due to larger capacitances of the NWELL resistors then expected.

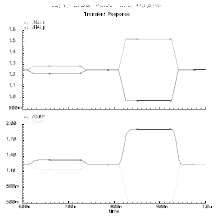

Figure 15 Simulation of the buffer

The simulation (Figure 16) of the power supply shows the start-up sequence of the circuit with an over current detection. After the start-up timer is finished, the over-current is detected. After the over-current timer is finished the output power is switched off. Measurements on the prototype show that the functionality is correct. The specifications need to be verified.

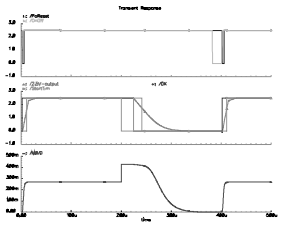

Figure 16 Simulation of the power supply

VI. STATUS AND PLANS

At this time, (Sept. 2001) the *EndCap* is in the design and prototype phase. Two test IC's have been submitted and just became available for tests. The produced circuits are the analogue buffer + AC coupling, power supply, and the power supply shunt regulator that delivers the power for the supply circuit.

Later this year a prototype of the ALCAPONE is planned, together with the final prototype of the ALABUF chip. The circuits will be irradiated to test their tolerance. The first complete *EndCap* is planned for Q2 2003.

Mechanical prototyping has started to investigate the cooling, cabling, and PCB handling.

VII. CONCLUSIONS

Full SEL protection of all *EndCap* electronics is possible. Simulations of the individual circuits showed the feasibility of using the 0.25µ CMOS process for the electronic components of the *EndCap*.

VIII. ACKNOWLEDGEMENTS

Acknowledgements go out to the ALICE Pixel chip design collaboration for the use of the design of the voltage DAC (designed by D. San Segundo Bello, NIKHEF, Amsterdam), the CERN microelectronics design group for the use of the Bandgap voltage reference cell (Paulo Moreira) and the support for prototype production. Most "components" of the ASIC's come out of the Library delivered by RAL [3].

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