Design and Test of a DMILL Module Controller Chip for the ATLAS Pixel Detector

Presented By: Roberto Beccherle / INFN – Genova

E-mail: Roberto.Beccherle@ge.infn.it

For the

ATLAS Pixel Detector Collaboration


References:

ATLAS Home Page:

http://atlasinfo.cern.ch/ATLAS/Welcome.html

Copy of This Talk:

http://www.ge.infn.it/ATLAS/Electronics/home.html

ATLAS Pixel Detector

- 40 MHz bunch crossing.

- 100 kHz L1 Trigger rate.

- 2.5 μs Trigger latency.

- New insert able layout.

- 3 barrels:

  ✓ In 2 external layers: 50 x 400 μm^2 pixels (8.85 and 12.25 cm).

  ✓ The innermost layer (B-Layer): 50 x 300 μm^2 pixels (5.05 cm from beam).
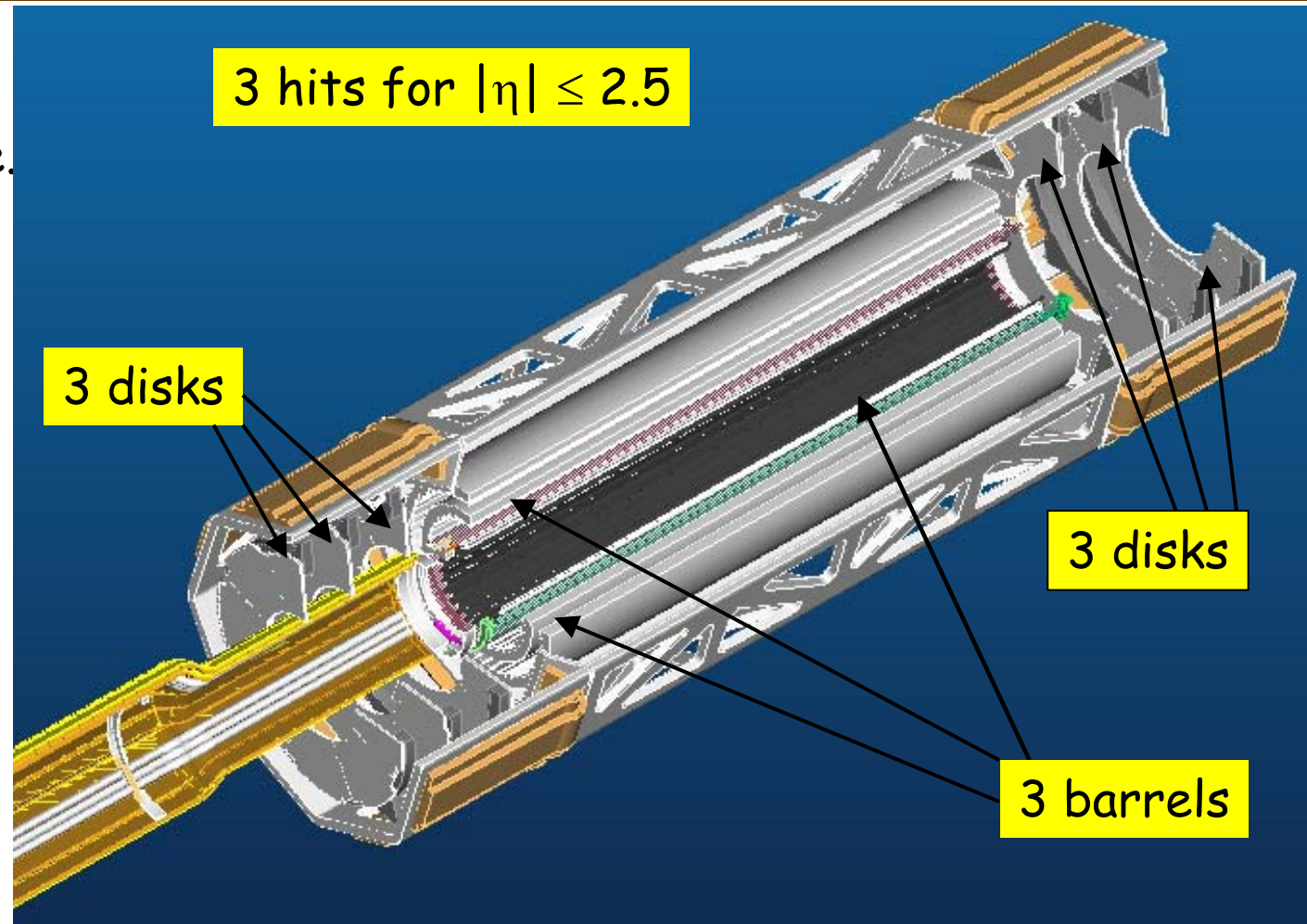
- 3 forward and backward disks.

- About 2 m^2 of silicon, ~ 100 x 10^6 Pixels divided in 1744 modules.

- Up to 50 Mrad for the B-Layer during the first years of operation.

3 hits for $|\eta| \leq 2.5$

3 disks

3 disks

3 barrels

Basic Building Block: Module
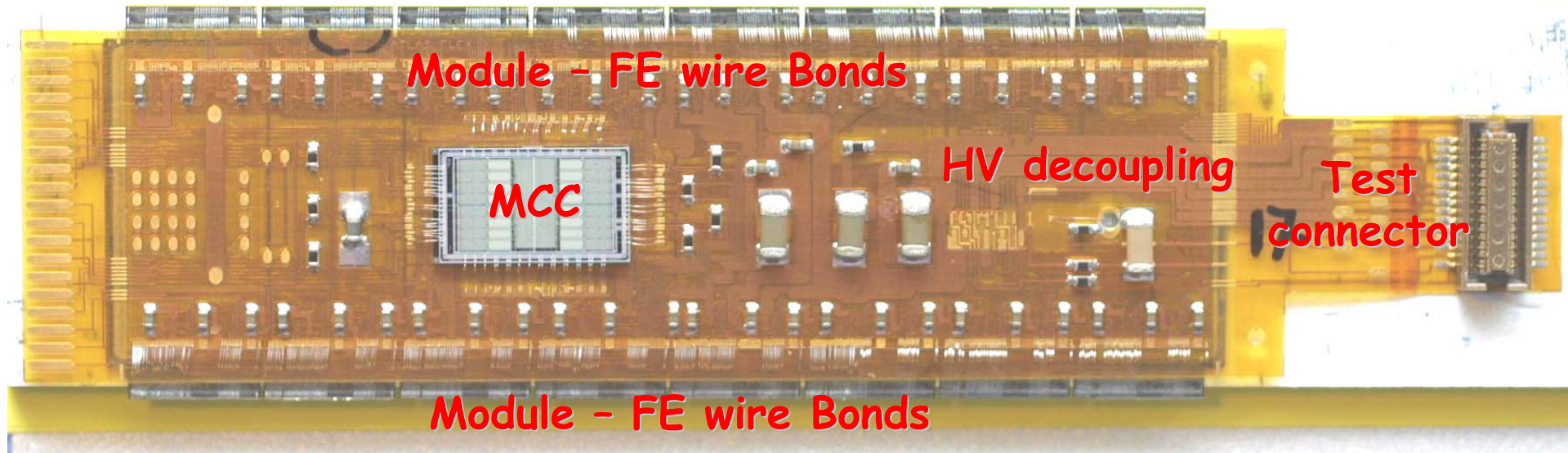
- The basic building block of the whole detector is a Module.
- Each module is built with 1 sensor, 16 Front End chips (bump bonded to the sensor) and one Module Controller Chip (MCC).
- Sensor: 200 μm oxygenated silicon, V_{bias} max. 600V.
- A Flex Hybrid circuit is glued on top of the FE electronics and is wire bonded to the FE chips.
- The MCC is wire bonded to the Flex circuit.
- 2 LVDS Output links provide up to 160 Mbit/s data speed.
- Optical encoder and decoder IC's are placed on the Module supports.

Front End Chip

- 2880 50x400 μm^2 channels: 160 rows x 18 columns.

- 800k transistors on a 0.8 mm^2 die

- 3000 e$^-$ threshold.

- σ_{noise} and σ_{th} 150 e$^-$.

- Each pixel can be addressed and fine tuned independently.

- One global control register to store configuration information into each pixel.

- EoC buffers provide storage of data before event formatting and transmission(40Mbit/s serial link).

- One RadSoft (AMS 0.8) and one RadHard (DMILL 0.8) versions.
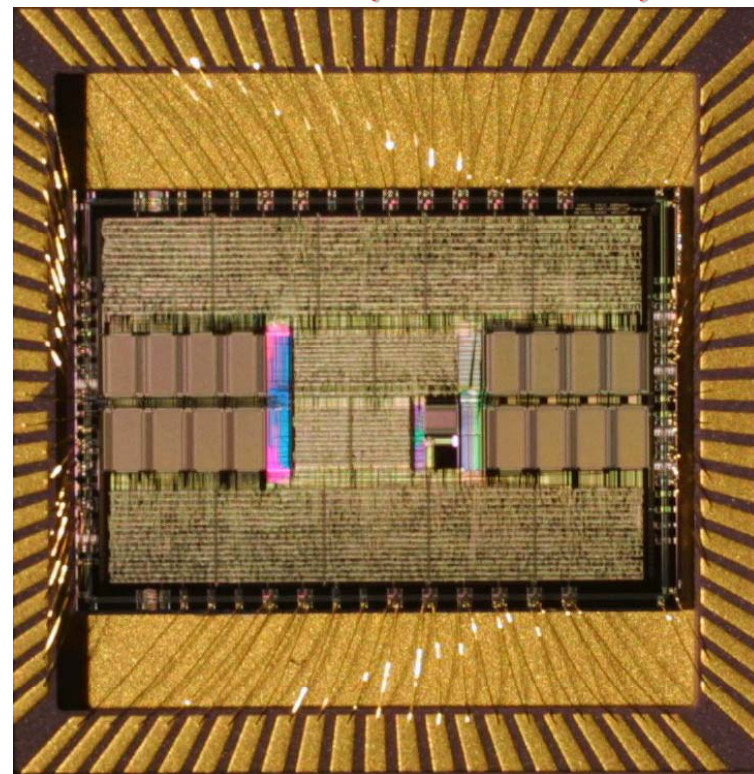
- LHC constraints have been met on the RadSoft version.

Pixel preamplifier/discriminator

End of Column logic
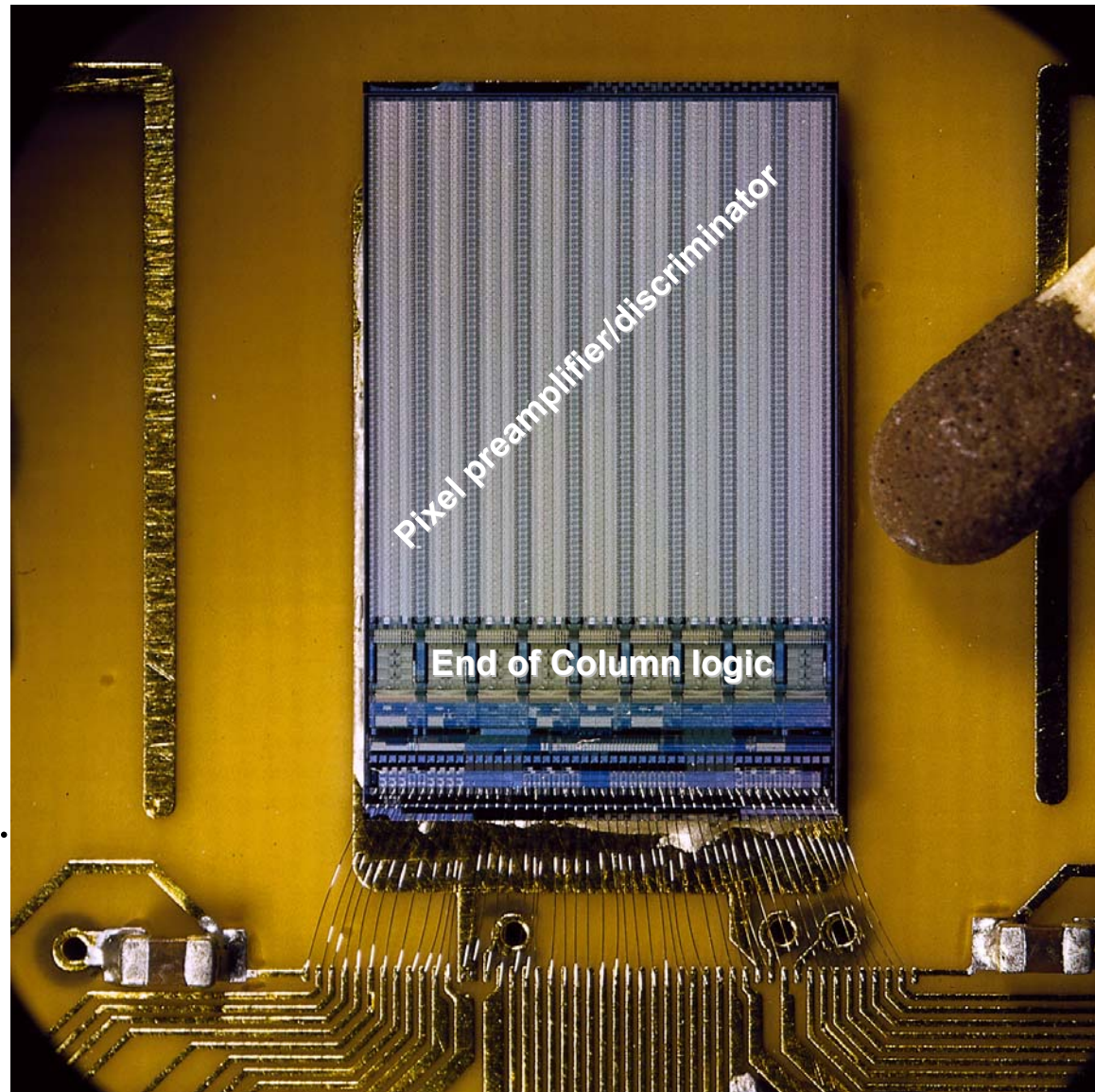
Module Controller Chip

MCC–D0 (~20 mm²)
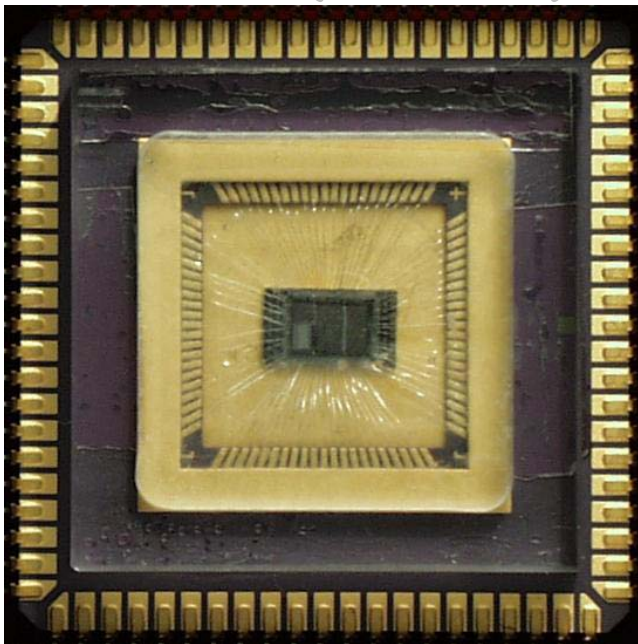
MCC–D2 (~100 mm²)

- Two chips were realized with DMILL technology:
  - ✓ **MCC-D0:** Test chip with only one FIFO and full Command Decoder. This chip was irradiated up to 30 Mrad at the CERN PS beam.
  - ✓ **MCC-D2:** Full functional MCC to be used to build RadHard modules.
- Final chip size (MCC-D2) is 100 mm² (50% bigger than the AMS version)
- In this design we have ~ 350.000 transistors in the design.

System Architecture
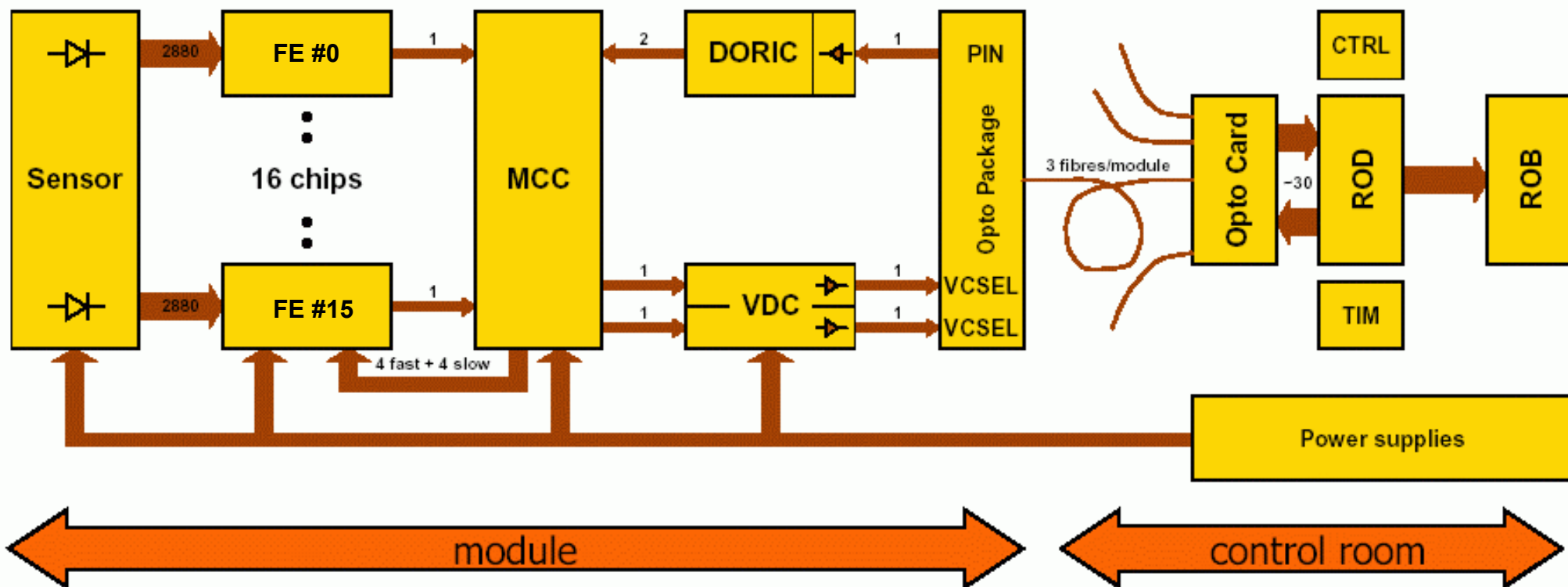
- Data push architecture: All FE chips are connected to the MCC with a star topology (point to point data links). 1 link between each FE and the MCC.
- All module operation is controlled via the MCC with a serial protocol.
- All data links active during data taking mode are LVDS.

MCC: System Functions

System Configuration:

- Individual FE addressing to R/W configuration data before a run starts.
- MCC configuration and ability to test FE chips during module assembly.

Event Building:

- As soon as a FE receives a hit the information is sent to the MCC.
- Data storage in 16 full custom FIFO's until all FE's terminate transmitting hits belonging to the same event.
- Data are formatted with some event compression and are sent to the ROD.
- Ability to provide error detection during Event Building.

Trigger Timing and Control:

- Trigger distribution to all FE chips keeping the synchronization.
- Error detection in case of buffer overflows and truncated / lost events.

Testability:

- Ability to disable one or more FE chips without stopping the whole module.
- Capability of testing internal structures in case of errors.
- Transmission error detection.

MCC: Architecture

- Serial data coming from FE chips are stored in 16 full-custom 25x32 bit deep FIFO's until event building occurs.

- Trigger, Timing & Control circuitry

- Command Decoder:
  5-bit Trigger command is recognized correctly, without any loss of synchronization even with a single bit-flip in the command.
  It is not possible to mix up configuration and data taking commands in case of bit-flips in the commands.

- Event Builder

- Register Bank:
  Holds configuration information and stores eventual error flags.

- Output Port:
  Formats data on two output pins allowing data speeds from 40 to 160 Mbit/s.
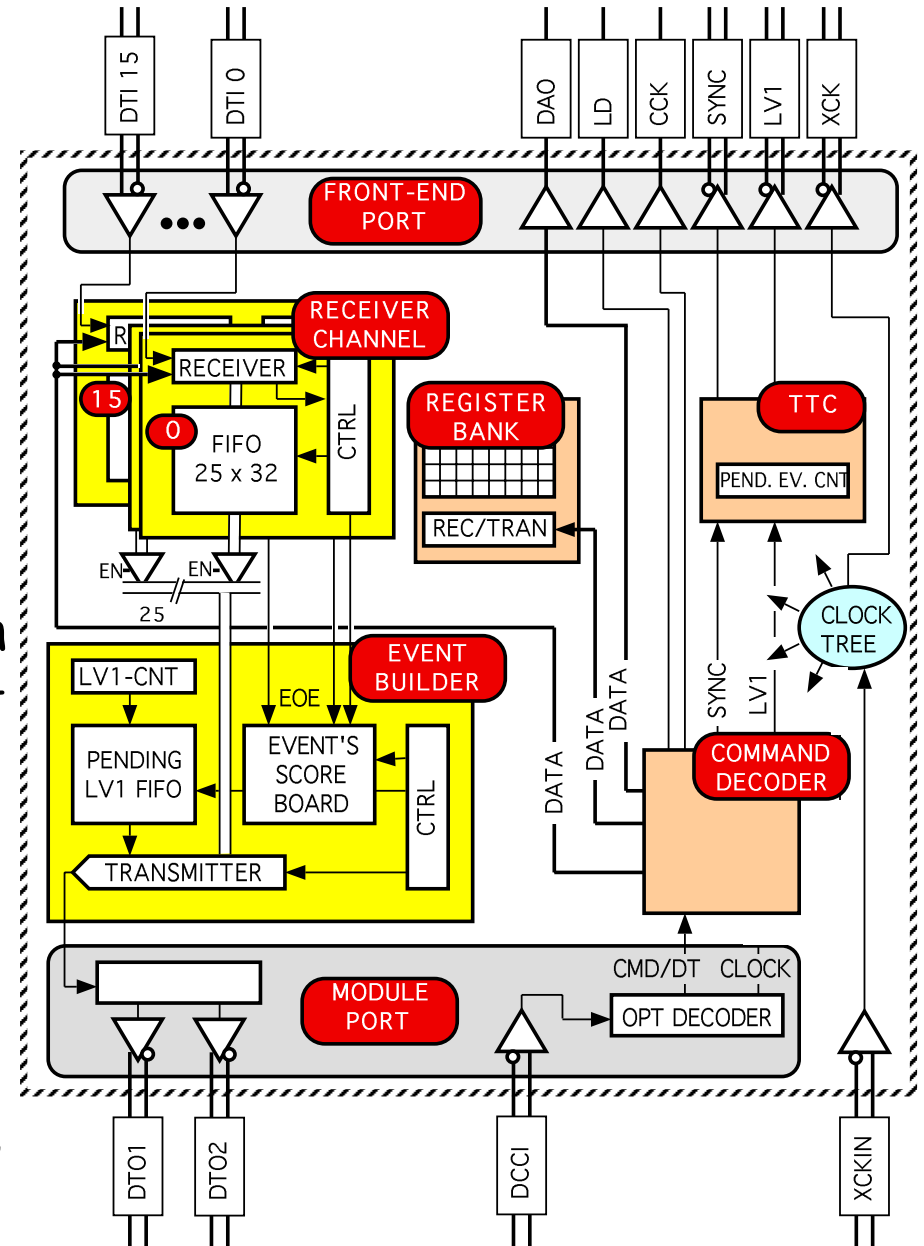
MCC: Design Methodology

- **Design Entry:**
  - ✓ Behavioural description using Verilog.
- **Logic Synthesis:**
  - ✓ Synopsys and Prime Time.
  - ✓ Design mapped on DMILL Std cells.
- **Place & Route:**
  - ✓ Full custom FIFO's hand placed.
  - ✓ Distributed buffer Clock tree.
  - ✓ Std cells + IO pads with Cell Ensemble.
- **DRC & LVS:**
  - ✓ Flat DRC and LVS.
- **Test Vectors:**
  - ✓ Behavioural and gate level simulations.
  - ✓ No back annotated netlist simulations.
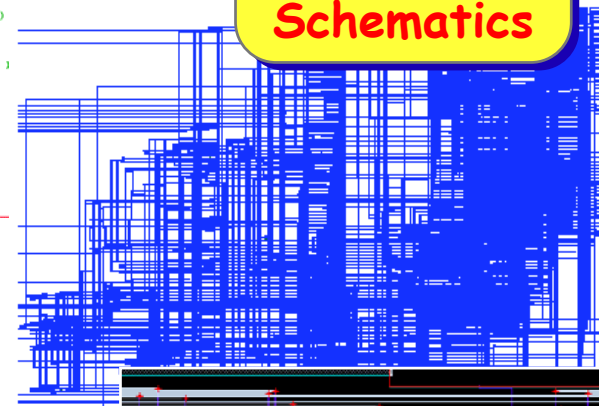 - ✓ Scan chain allows ATPG.

Verilog

Synthesized Schematics

Routed
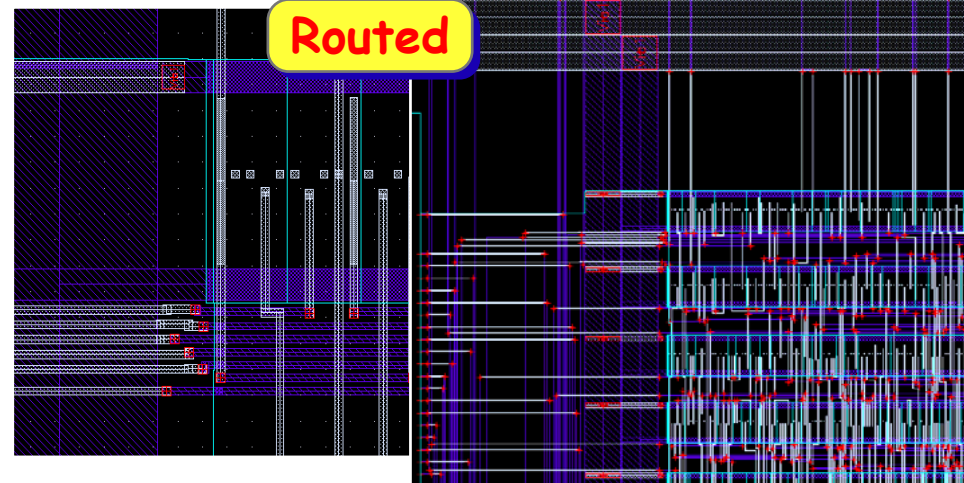
MCC: Test Setup

- Complex Event Building algorithm is very hard to debug.

- We decided to develop a custom test system based on a VME board.

- The system is based on a main board "MCC exerciser"

- Additional "memory" boards allow simulated FE data to be sent to the MCC.

- Each one of the daughter boards allows to stimulate /sample two input/output lines from the MCC.

2 channel Memory Card

- This allows to store data that simulate up to 16 FE chips and provide input data to the MCC while sampling one of the two output lines.

- The whole system is synchronous with a 40 MHz clock.

- A C++ software allows to fully control the operation of the boards.

SimPix Simulation Framework

- SimPix is a multi purpose C++ simulation environment developed in Genova.

- This tool allows three main tasks:

  ✓ System architecture simulations used to study the impact of different electronics architectures and inefficiencies on physics. This is done simulating the whole Pixel detector starting from GEANT events. Lev2 Trigger studies done using this mode.

  ✓ Simulation of both FE and MCC electronics and direct comparison of the results with Verilog simulator via a TCP/IP link. Used to validate behavioural test vectors.

  ✓ Hardware test using the MCCex board. This operating mode allows also to interface the simulation with our Logic State Analyzer. Used to test hardware (MCC-D0,MCC-D2). Used during irradiation at the PS at CERN.
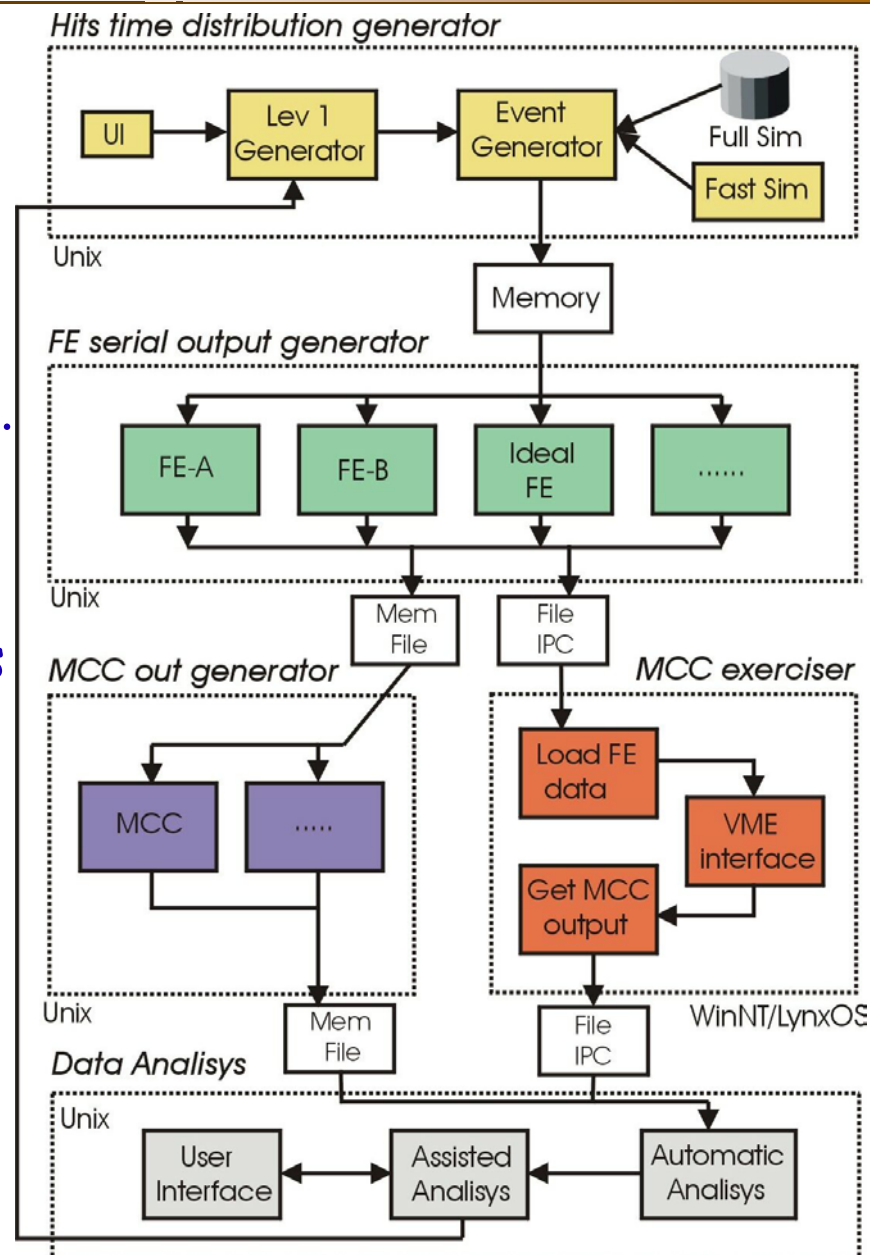
SimPix: an example
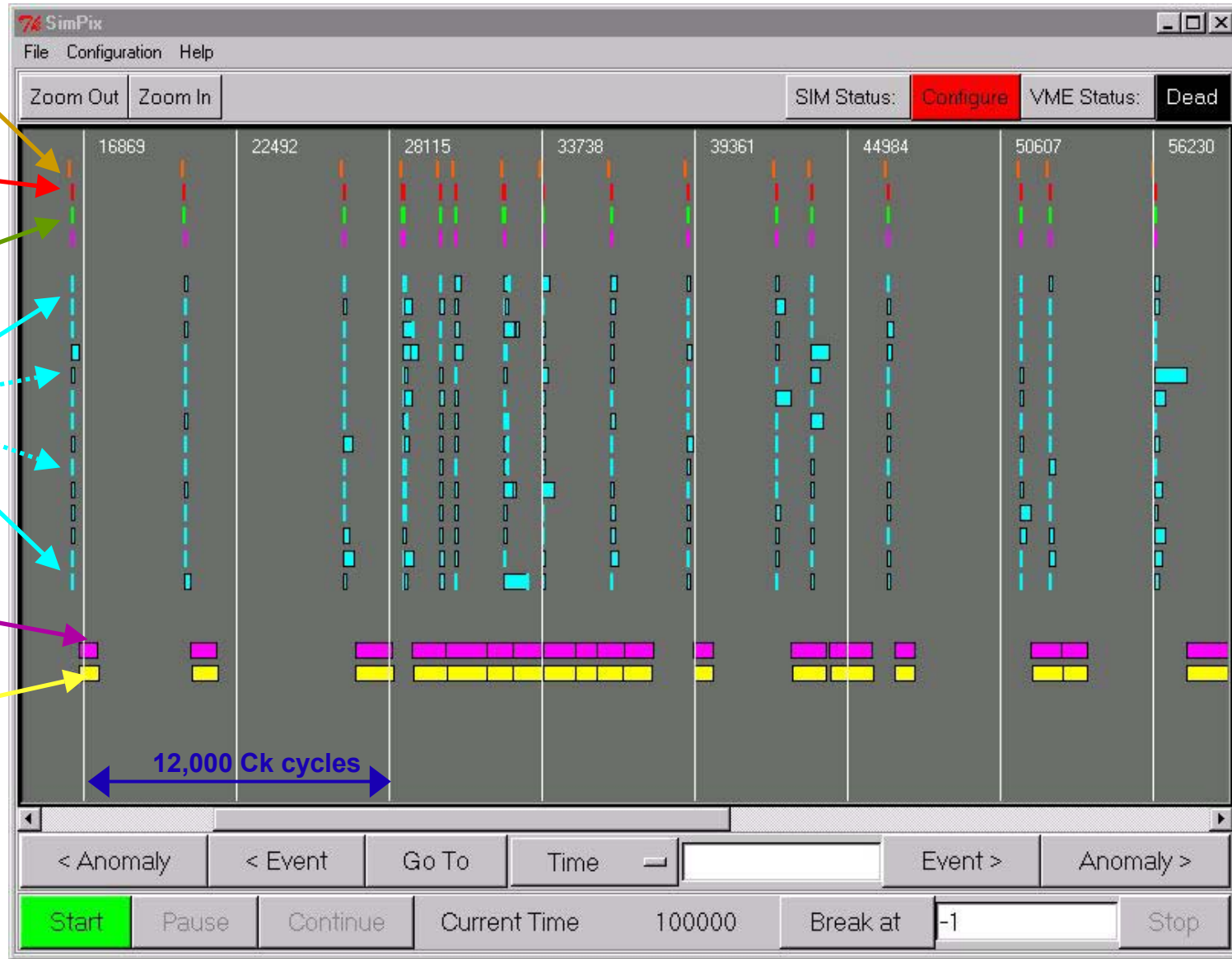
- An example of an MCC-D2 test using SimPix and the MCCex VME board.

MCC-D0 Laboratory Tests

Chip #	Transparent Mode	Registers PLL	Registers MCCex	Chip FIFO	FIFO Wr pointer	Max Clock (MHz)
1	OK	OK	OK	OK	OK	-
2	OK	OK	OK	OK	OK	-
3	Fail	OK	OK	OK	OK	95
4	Dead	Dead	Dead	Dead	Dead	Fail
5	OK	OK	OK	OK	OK	95
6	OK	OK	OK	OK	OK	90
7	OK	OK	OK	OK	OK	98
8	OK	OK	OK	OK	OK	100
9	OK	OK	OK	OK	OK	90
10	OK	OK	OK	OK	OK	93
11	OK	Bits blocked	Bits blocked	Fail	Fail	Fail
12	OK	OK	OK	OK	OK	90
13	OK	OK	OK	OK	OK	92
14	OK	OK	OK	OK	OK	96

- As all DMILL chips were not tested upon arrival we packaged 14 MCC-D0's and performed a full test in our lab using the pattern generator driven by SimPix and found that 3 chips were not working correctly.

- All working chips were fully functional up to 90 MHz (synthesized at 80 MHz).

The MCC-D0 Irradiation Setup

MCCex + Adapter

MCC Selector

Repeater

40

64

40

MCC-D0 CARDS

VME PATTERN UNIT

64

Repeater

40

POWER SUPPLY

29 m

5 m

MCC-D0 CARDS
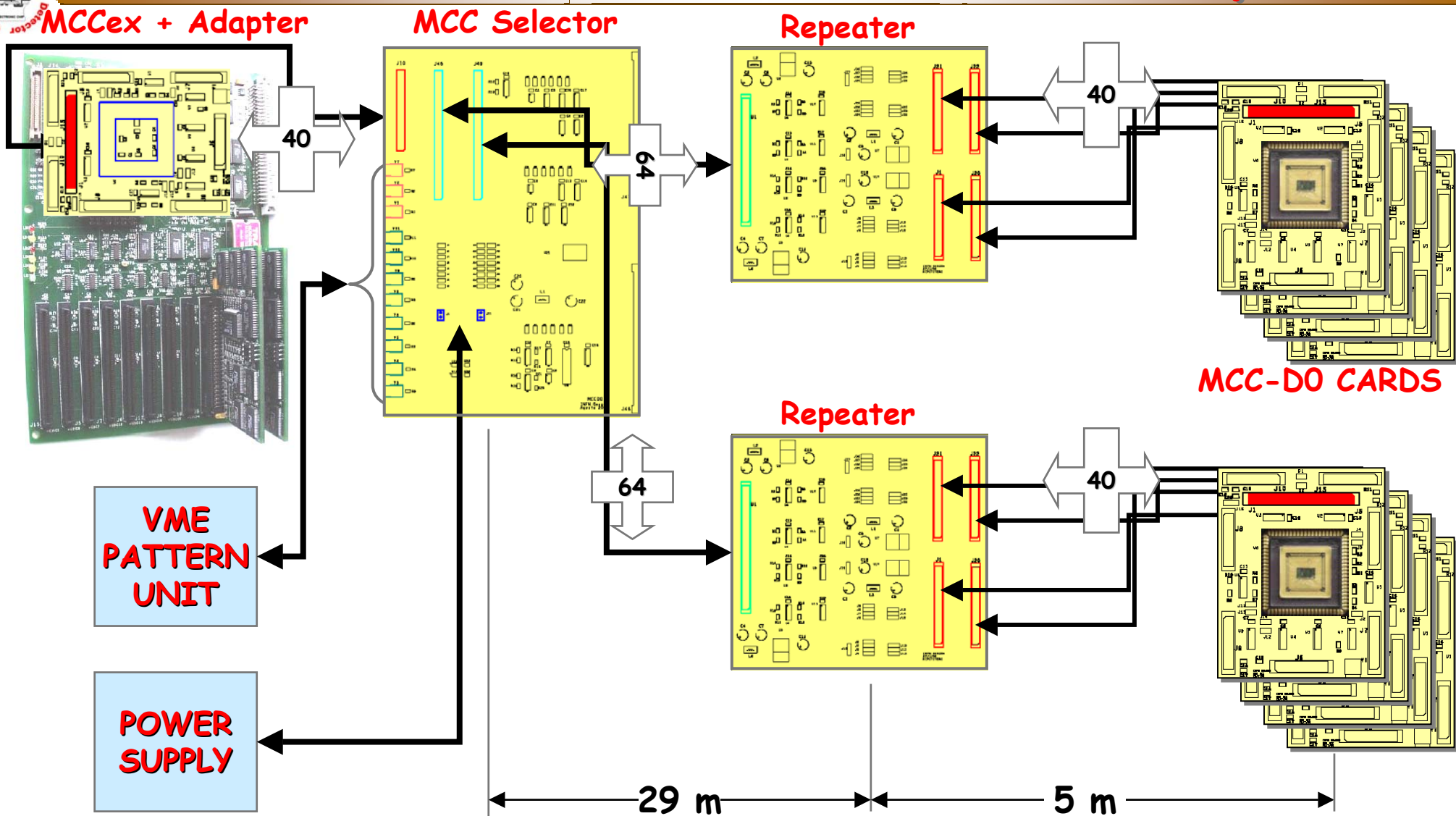
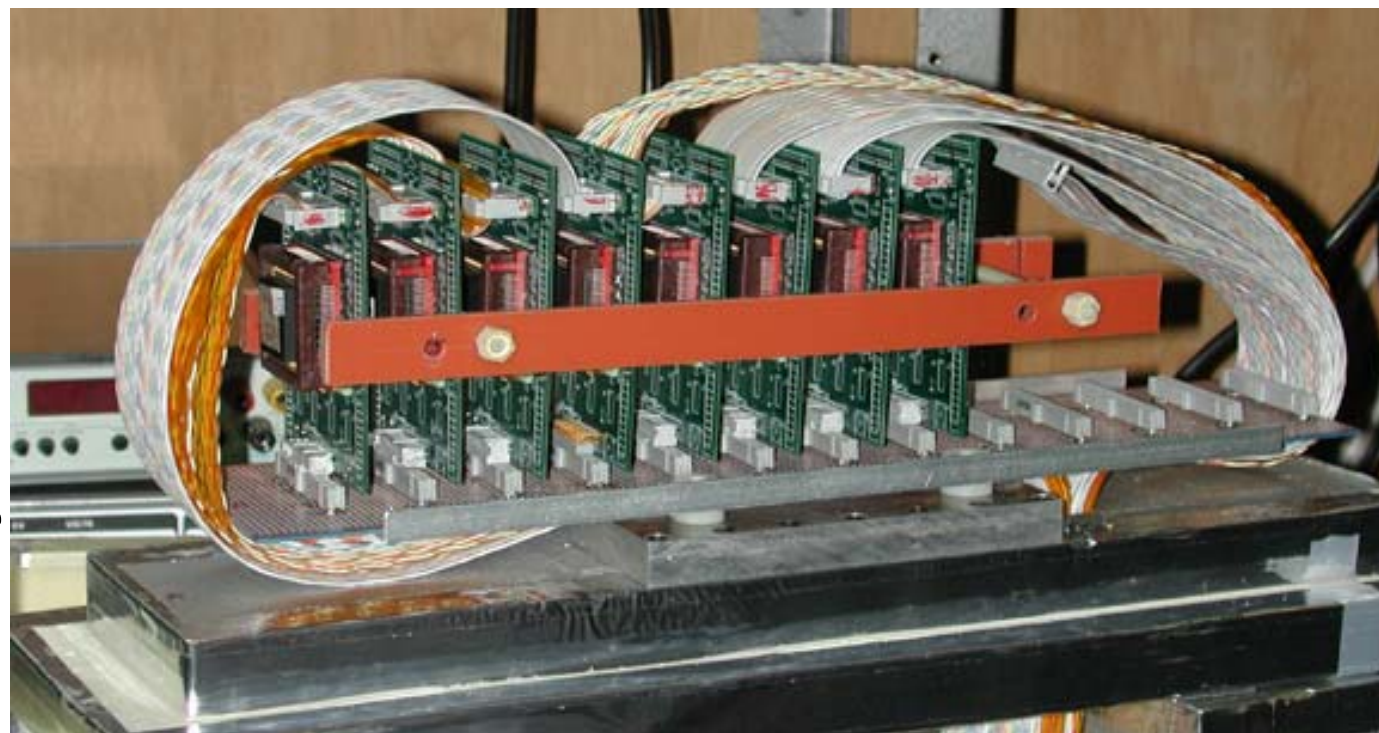- The whole setup was driven by SimPix and allowed continuous data monitoring and strobing to all 8 chips while being irradiated (SEU studies).

Test Beam Measurements

- Beam is 2x2 cm^2, each spill lasts 200 - 250 ms.
- 8 chips were irradiated.
- Cold box at –3 C^o.
- We could move the box out of beam any time.
- Dose recorded by scaler and not with data.
- 30 Mrad in 5 days.

- As only one chip can be active at a time at every PS cycle one MCC executes two different tests: a "dynamic" test on the active MCC and a "static" one on all other chips. The active chip is changed automatically after each spill.
- Static test: We wrote a known configuration pattern in all FF's and in the full custom FIFO before the spill and checked data after the spill for SEU.
- Dynamic test: In this case configuration data are written during the spill and checked against bit-flips on data lines and internal structures.

Test Beam Results

- The system was very stable during all operations.

- The only problem was related to our full custom LVDS pads in one of our chips after .5 Mrad. Resetting the whole chip before each spill the problem disappeared.

- Data read phase is always performed 3 times in order to avoid read out errors.

- We observed negligible errors during the write phase.

Full custom FIFO

Standard cell scan flip flops

Dose (Mrad)

- We measured a pure static bit flip probability per spill, of about 1.2% for the standard cell scan flip flops and 2% for the full-custom FIFO.

- After irradiation the maximum clock frequency dropped by 40%.

- Immediately after irradiation we found that all chips were perfectly working, but after several weeks of cool down we found that only 4 chips were still working! We tried to anneal them in a oven (100° for 7 days) but they never worked again. We suspect problems in the LVDS pads but we are not sure…
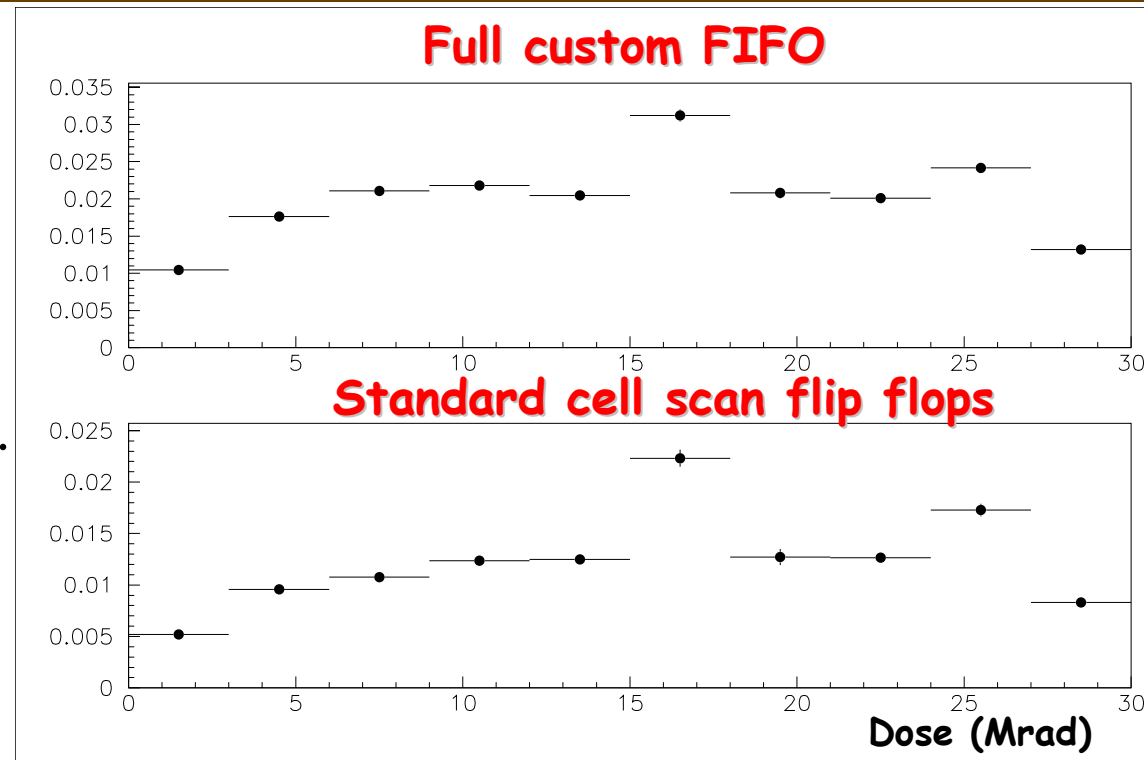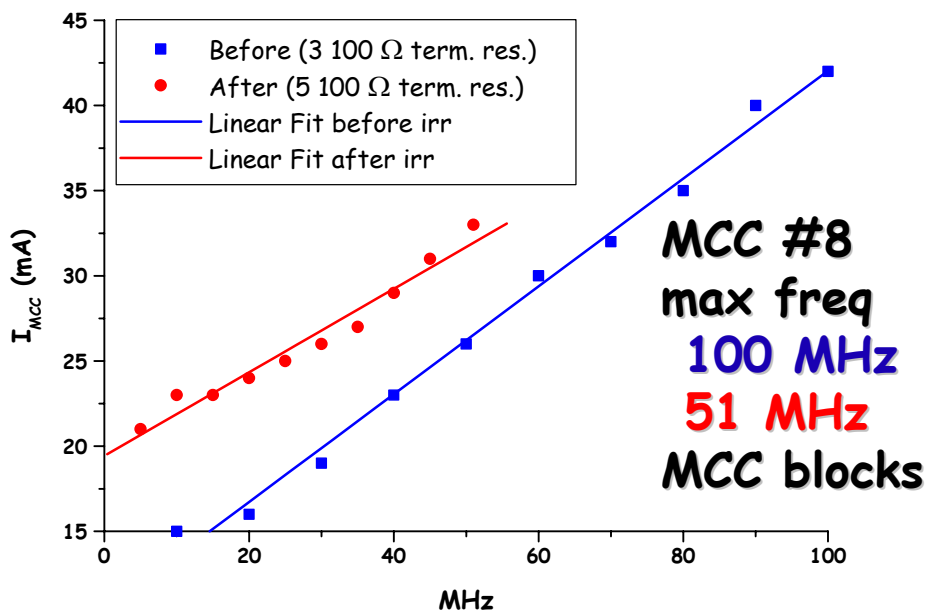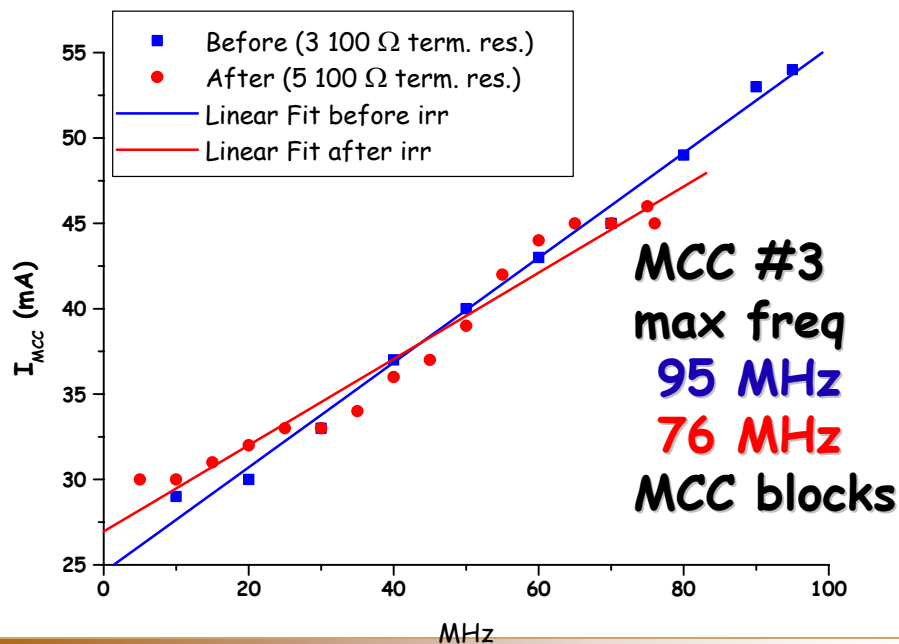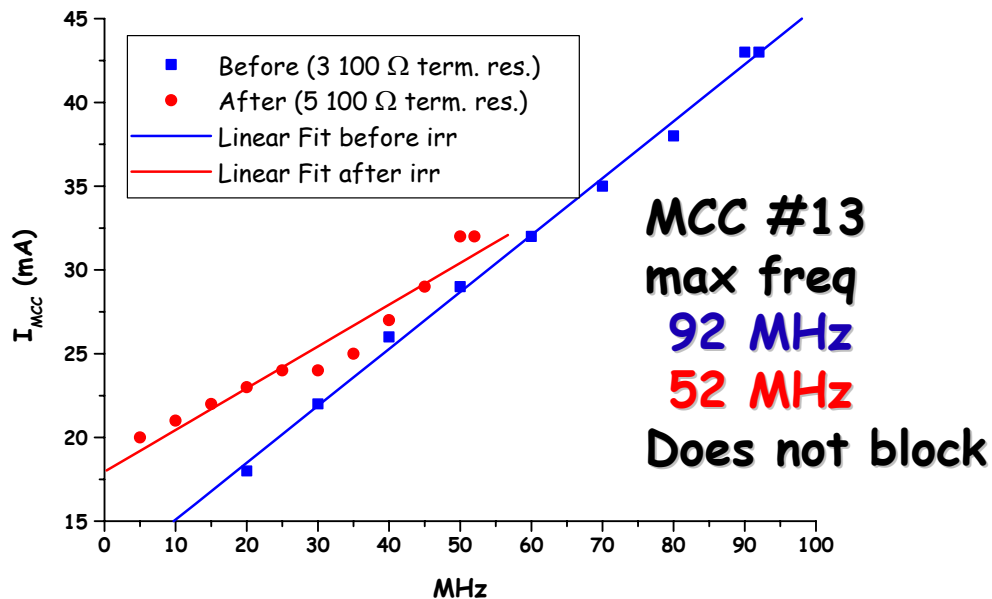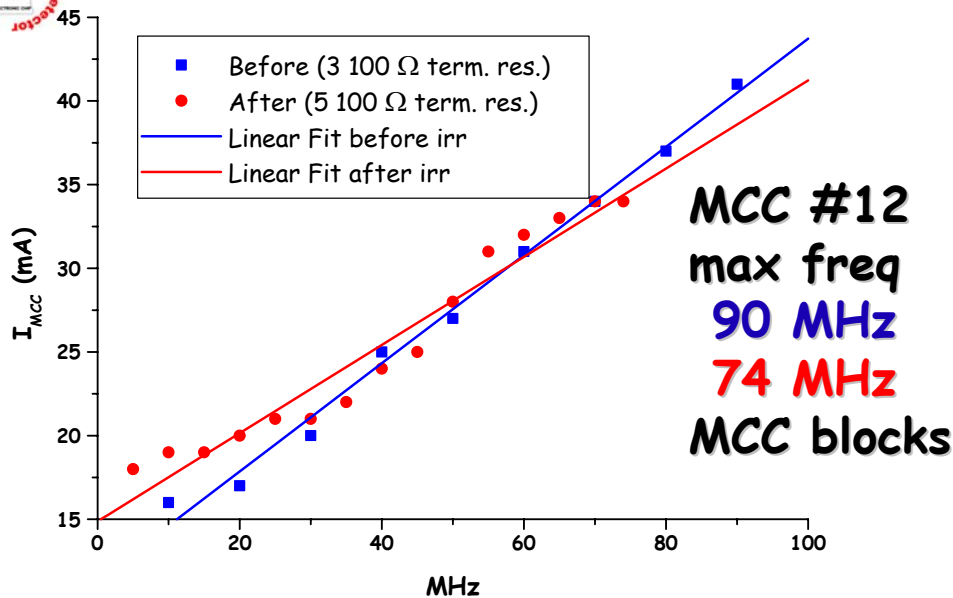
LVDS drivers measurements

Non-irradiated MCC-D0

# 6	p	n	diff
DTO	1.065	1.383	0.318
LV1	1.080	1.400	0.320
STRO	1.060	1.380	0.320
XCK	1.147	1.447	0.300
SYNC	1.100	1.418	0.318
	start	reset	run
Imcc	23	29	21
	mA	mA	mA

MCC–D0's working after irradiation

# 3	p	n	diff
DTO	1.587	1.824	0.237
LV1	1.642	1.876	0.234
STRO	1.504	1.760	0.256
XCK	1.556	1.800	0.244
SYNC	1.793	1.540	0.253
	start	reset	run
Imcc	13	37	29
	mA	mA	mA

# 8	p	n	diff
DTO	1.510	1.760	0.250
LV1	1.482	1.747	0.265
STRO	1.640	1.875	0.235
XCK	1.660	1.888	0.228
SYNC	1.667	1.907	0.240
	start	reset	run
Imcc	4	29	20
	mA	mA	mA

# 12	p	n	diff
DTO	1.440	1.705	0.265
LV1	1.516	1.770	0.254
STRO	1.480	1.738	0.258
XCK	2.622	2.622	0.000
SYNC	1.780	1.470	0.310
	start	reset	run
Imcc	2	24	16
	mA	mA	mA

# 13	p	n	diff
DTO	1.377	1.650	0.273
LV1	1.326	1.610	0.284
STRO	1.310	1.600	0.290
XCK	1.343	1.615	0.272
SYNC	1.616	1.328	0.288
	start	reset	run
Imcc	2	29	19
	mA	mA	mA

MCC-D0's NOT working after irradiation

# 5	p	n	diff
DTO	0.062	0.062	0.000
LV1	0.055	0.055	0.000
STRO	0.067	0.066	0.001
XCK	2.615	2.615	0.000
SYNC	0.061	0.061	0.000
	start	reset	run
Imcc			4
	mA	mA	mA

# 7	p	n	diff
DTO	2.655	2.655	0.000
LV1	2.683	2.683	0.000
STRO	2.695	2.695	0.000
XCK	2.637	2.637	0.000
SYNC	2.664	2.664	0.000
	start	reset	run
Imcc	4	6	6
	mA	mA	mA

# 9	p	n	diff
DTO	0.000	0.000	0.000
LV1	1.293	1.590	0.297
STRO	1.441	1.116	0.325
XCK	1.432	1.116	0.316
SYNC	0.060	0.060	0.000
	start	reset	run
Imcc	4	23	16
	mA	mA	mA

# 10	p	n	diff
DTO	0.000	0.000	0.000
LV1	0.000	0.000	0.000
STRO	0.000	0.000	0.000
XCK	1.327	1.610	0.283
SYNC	0.000	0.000	0.000
	start	reset	run
Imcc	2	14	10
	mA	mA	mA

MCC-D2 Laboratory Tests

- We performed 3 different types of tests on 19 packaged chips:

1. DC test:
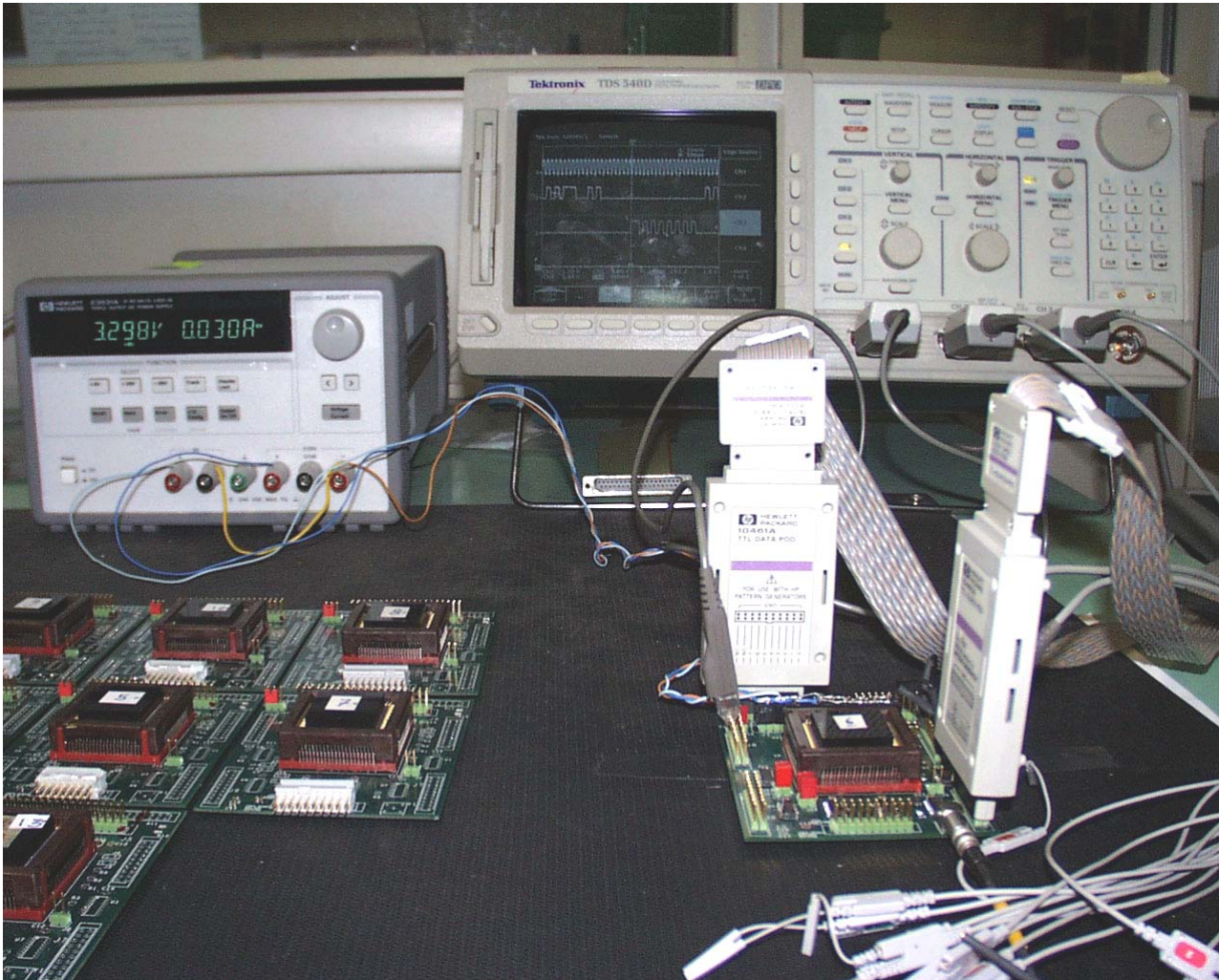   Static power consumption.

2. Logic State Analyzer:
   Variable CK frequency test, command decoder test, power vs. CK frequency.
   Estimated 10% coverage.

3. MCC-exerciser:
   Complete test of all FIFO's and registers, FE configuration and complete Event Building. The system runs at a fixed frequency of 40 MHz. Estimated 70% coverage.

- We did not perform tests on a wafer using a probe card.

Power consumption vs. CK frequency

- We tested power consumption writing and reading back patterns of data both in the full custom FIFO's and in the Register Bank.

- All 19 packaged chips have been tested up to the maximum frequency where the read back patterns were still correct.

- Maximum clock frequency turned out to be between 70 and 72 MHz in good agreement with synthesis (78 MHz).

- Power consumption was between 140 and 150 mA for all working chips.

- 3 chips did not pass the DC test.
  1 chip did not turn on
  2 chips drew > 200 mA.

- Yield after DC test 84%.

IDD versus CK Frequency

Command Decoder and Trigger Tests
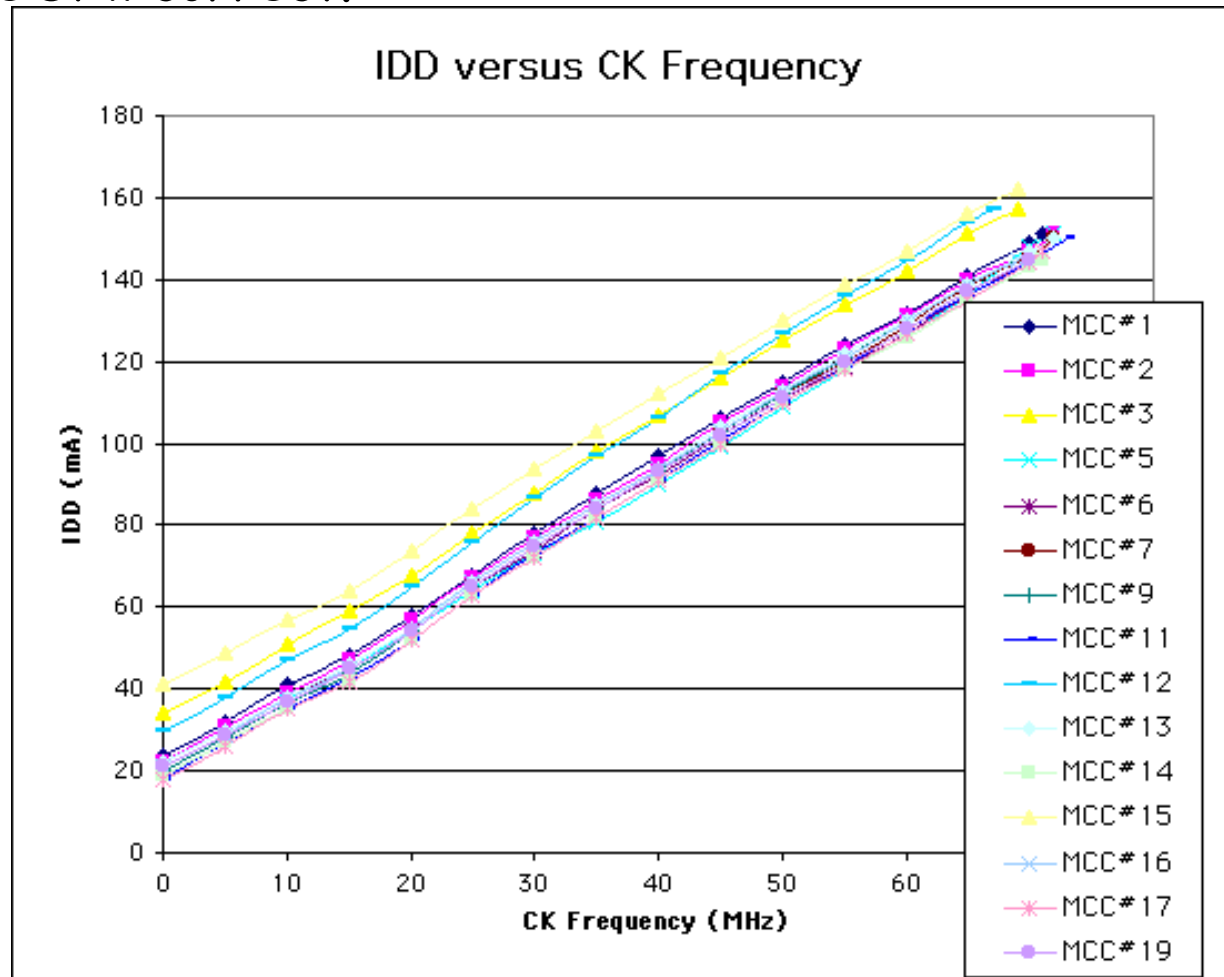
Command Decoder tests

- During all test performed on the chips we never observed a problem with the chip blocking and not being able to recover with a GlobalResetMCC command even running at very high frequencies (150 MHz).

- ✓ This indicates that we can really operate the chip without a Reset pin.

- The Trigger command works correctly.

  1. One can issue consecutive Trigger (11101) commands.

  2. All single bit flips inside a Trigger command are correctly decoded.

- ✓ No problems found inside the Command Decoder.
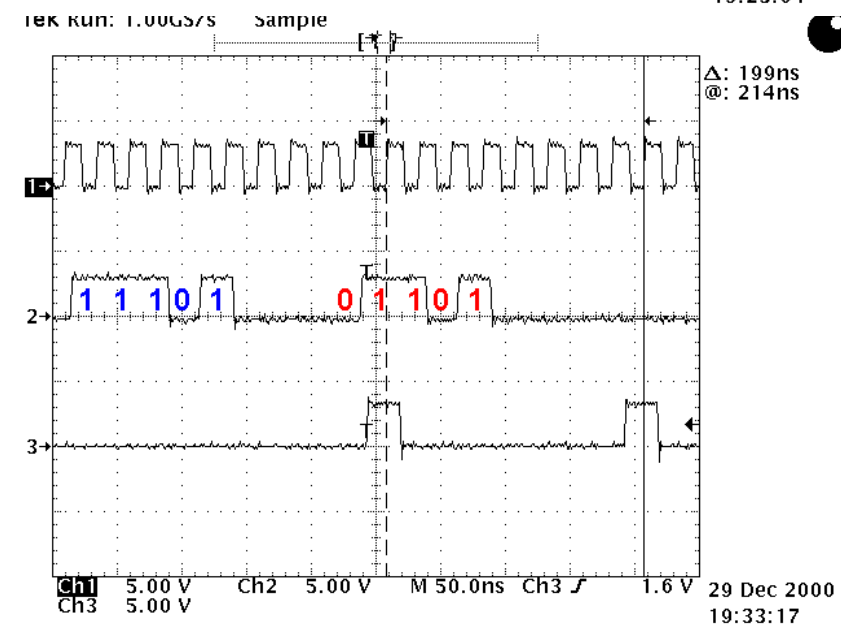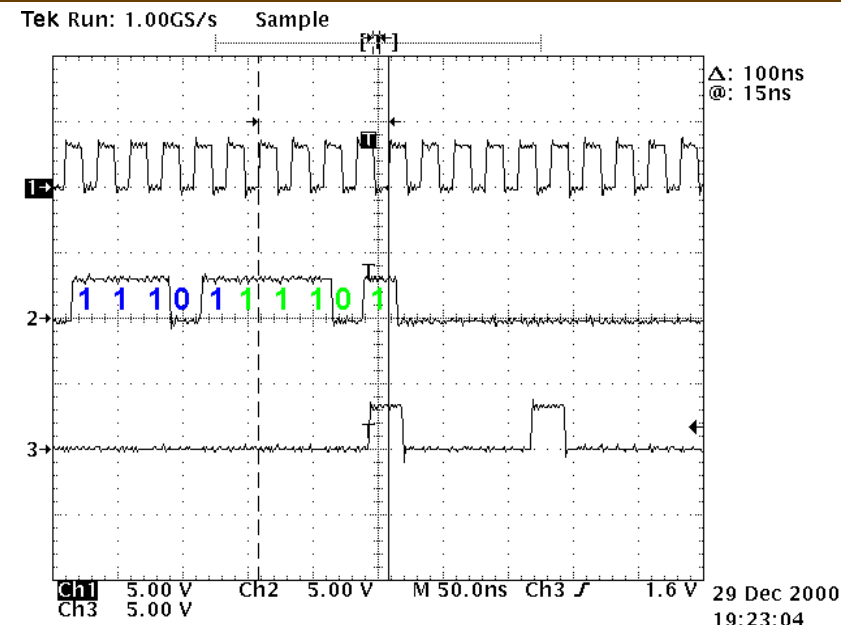
MCC-D2 Test Results

Logic State Analyzer Test results

- MCC #4 and MCC #8 show no output at the Clock pin.
- MCC #6 and MCC#15 have one output pin stuck at "1".
- MCC #13 and MCC #17 have a test pin stuck at "1".

Only 11 out of 19 chips pass this first 2 tests (Yield ~58%).

MCCex Test results

- This test writes into all the FIFO's and into all the Registers patterns of all zeros (all ones) but one bit. This allows a test of all locations of the chip.
- A couple of chips (#3, #16) have at least one FIFO that can not be written.
- Some chips (#1, #12, #16) have problems in accessing certain FIFO locations, i.e. problems in the Read/Write pointers.
- Many chips have some bits of at least one FIFO stuck at 0 or 1.
- Chips #1 and #16 have some bits in configuration registers that are stuck.

Only MCC #11 and MCC#19 are completely OK !!! (Total Yield ~11%).

Complete event building turned out to work only at 33 MHz! (syn @78 MHz)

- This can be due to lack of back-annotation and/or wrong timing models.

Conclusions and Outlook

- We submitted two different versions of the Module Controller Chip using the 0.8 μm DMILL technology.

- A small test chip containing all main building blocks, including the full custom FIFO and LVS drivers/receivers, was successfully irradiated up to 30Mrad.

- Some problems, probably related to LVDS pads, were detected.

- Detailed SEU studies were performed.

- The full chip (100 mm^2) turned out to have an unacceptable low yield, taking into account that the full custom parts are VERY conservative and that the chip is built using Standard Cells.

- We developed a very versatile test system and test strategy that will be fully used in all future developments of our electronics.

- This system is very useful both for functional/hardware verification and allows detailed irradiation studies.

- The collaboration also submitted two distinct versions of the FE chip(80mm^2), which showed many problems related to the technology itself, which turned out to produce a yield less than 1%.

- The collaboration decided to investigate the 0.25mm technology developed at CERN and now maintained by RAL and both an MCC and a FE chip are under development and will be submitted at the end of September.