A Remote Control System for On-Detector VME Modules of the ATLAS Endcap Muon Trigger

Y. Nakamura*, K. Hasuko, H. Kano, H. Sakamoto
International Center for Elementary Particle Physics (ICEPP)
University of Tokyo, Tokyo 113-0033, Japan
M. Ikeno, O. Sasaki
High Energy Accelerator Research Organization (KEK)
Tsukuba 305-0801, Japan
R. Ichimiya, H. Kurashige
Kobe University, Kobe 657-8501, Japan
K. Mizouchi
Kyoto University, Kyoto 606-8502, Japan
C. Fukunaga, Y. Ishida and K. Tanaka
Tokyo Metropolitan University, Tokyo 192-0397, Japan
*Correspondent: yoshio@icepp.s.u-tokyo.ac.jp

Abstract

A remote control system has been developed for on-detector VME modules of the ATLAS endcap muon trigger. The system consists of an on-detector remote controller and a local interface in a Readout Driver (ROD) crate. The controller and interface are connected with dedicated optical links based on Agilent G-LINK. The local host can master the VME bus to access the on-detector slave modules using G-LINK words through the intermediate modules. The control system can fully control and configure FPGA-embedded modules whose configuration data is susceptible to SEUs. The system supports periodical read back and reconfiguration to assure correct configuration data against SEUs. We present the idea, prototype and the results of performance tests of the system.

I Introduction

We have developed a remote control system for VME modules located in a radiation environment. The primary purpose of our development is for trigger and readout modules in the end-cap muon trigger of ATLAS at LHC [1], [2]. They must be located on the circumferences of the trigger-dedicated detectors, i.e., Thin Gap Chambers (TGCs). Hence a remote control system is necessary to configure and control these on-detector modules.

The trigger modules (High-pT (HPT) modules [3]) have been built using ASICs; the HPT modules are controlled by configuring some registers in the ASICs. The readout modules (Star-Switch (SSW) modules [4]) are relay modules between on-detector readout buffers and Read-Out Driver (ROD). In addition, SSWs have functionalities to relay configuration data for the downstream on-detector modules. Hence they have been built using FPGAs for flexibility of development to satisfy such the various requirements. All the functionalities of SSW are controlled by configuration and control of these FPGAs.

We introduce a VME module as an on-detector remote controller and this module controls HPT and SSW modules via VME bus. However configuration data of FPGAs are susceptible to radiation-induced upset; Single-Event Upset (SEU), and the functionalities of FPGAs might be crushed because of SEUs. Hence the VME bus is used as a byte-based configuration path for the FPGAs. The SSW modules are built using Xilinx Virtex series FPGAs [5], which support such the configuration and read-back schemes as SelectMAP mode. The combination of the VME controller and SelectMAP mode performs a watch-dog beside FPGAs by periodical read-back procedure. On the other hand, VME protocol encoders on HPT and SSW modules as well as the remote controller are based on CPLDs which have risk of SEUs. The controller can provide an extra path, IEEE 1149.1 (JTAG), to configure CPLDs to prepare for SEUs.

The choice of FPGAs and CPLDs is possible in the endcap muon trigger system since the radiation level where HPT and SSW modules are placed is not expected to be extremely harsh [6]. This gives us a large advantage of good cost performance for development.

In this paper, the design and prototype implementation of the remote control system is described in the next section. Functionality is summarized in Section III, and then results of performance tests are discussed in Section IV. Development for final version is reported in Section V; the conclusion is finally given in Section VI.

II System Design and Prototype Implementation

In this section, both the design of the remote control system and the prototype implementation are described. The overview of the system is shown in Fig.1.

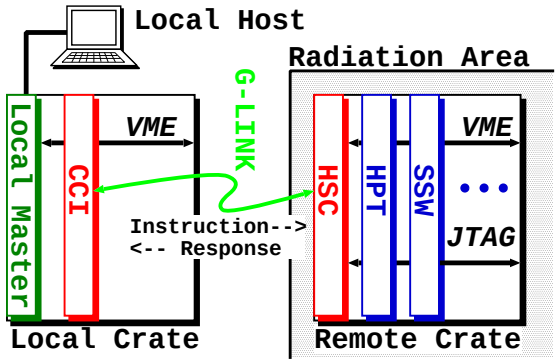

Figure 1: An overview of the remote control system

The goals of the system are 1) to control and configure the on-detector slave modules from a local host via VME bus, and 2) to restore VME functionality if failed. To mediate between the local host and the slave modules, two additional VME modules, Hi-pT/Star-Switch Controller (HSC) module and Control/Configuration Interface (CCI) module, are introduced [7]. The HSC module is in a on-detector VME crate (called remote crate). As a master module, it controls all the slave modules (HPT and SSW modules) in the remote crate. The CCI module is a slave module in ROD crate outside the experimental hall (called local crate). It is managed by a local host via a VME master module in ROD crate.

The HSC and CCI modules are connected with dedicated links for a full-time controlling. Optical links based G-LINK are chosen for the system. The host can control the on-detector slave modules with instructions using G-LINK words, and also receive their responses using returning words. 90-meter optical links in the trigger system are used to connect the HSC modules with the CCI modules.

A block diagram of the HSC and CCI modules are shown in Fig.2. Details are described below.

A HSC (Remote Controller)

The HSC module receives (transmits) G-LINK words as instructions from (to) the local host via the CCI module and optical fibers. When the instructions on VME control are received, the HSC module can master the VME bus to access slave modules in the remote crate. FPGAs on SSW modules are configurable; configuration bit streams can be read and written via the VME bus. On the other hand, CPLDs implemented in both HSC and slave modules are configured via JTAG bus structured on the backplane of the remote crate. Dedicated instructions are prepared to control the JTAG bus.

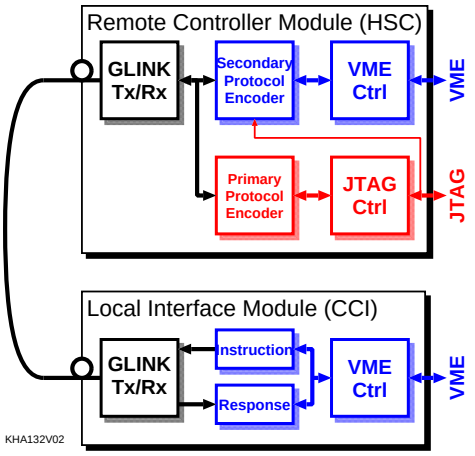

Figure 2: A block diagram of the HSC and CCI modules

The HSC module has two blocks to encode (decode) instructions to (from) the CCI module. The one is for JTAG control, and the other for VME control. The former is more fundamental and called Primary Protocol Encoder (PPE), while the latter is called Secondary Protocol Encoder (SPE). At least, the PPE and JTAG controller should resist any radiation effects. Functionalities of the SPE including VME access control can be restored with JTAG via the PPE and JTAG controller. Instructions to reset functional blocks are interpreted at PPE.

B CCI (Local Interface)

To communicate with the HSC module, the same G-LINK parts. Instructions from the local host are at first stored into instruction registers on the CCI module, and then transmitted to the HSC module. Responses from the HSC module are stored into response registers and kept for the local host. There are some other registers for the control/status and special VME functionality such as interrupts. All the registers can be accessed via VME bus.

C Prototype Implementation

The HSC module has been built as special 9U VME module, whose size is 367.7mm height $\times$ 160.0mm depth. This size is required from the area limit in the end-cap muon trigger system. For G-LINK parts, Agilent HDMP-1032/1034 transmitter/receiver are used to support 16-bit duplex transmission [8]. A 40MHz oscillator provides the synchronization clock to operate at 640Mbits/sec serial data rate. For EO/OE conversion, Infineon V23818-K305-L57 is used [9].

Main functionality has been built using programmable logic devices, Altera MAX7000 series CPLDs [10]. QFP144 is used for PPE and QFP208 for SPE and VME

control. In the PPE, JTAG-related instructions are interpreted into 8-bit data with 3-bit address to access an embedded JTAG controller, embedded Test Bus Controller (eTBC) manufactured by Texas Instruments [11]. The function of eTBC is to master a JTAG Test Access Port (TAP) under the commands of host. In the SPE, A32/A24 D32/D16 access is supported, but no block transfer access.

JTAG bus is built in the J3 backplane of the remote crate. 3.3V for devices on the HSC module is also provided from this backplane.

The CCI module has been built 6U VME64 extension module required from the specification of ROD crate. Main functionality has been built using a FPGA, ACEX1K manufactured by Altera Corp. The CPLD-base VME controller supports all single access.

Fig.3 shows a photograph of the HSC and CCI modules with optical fibers.

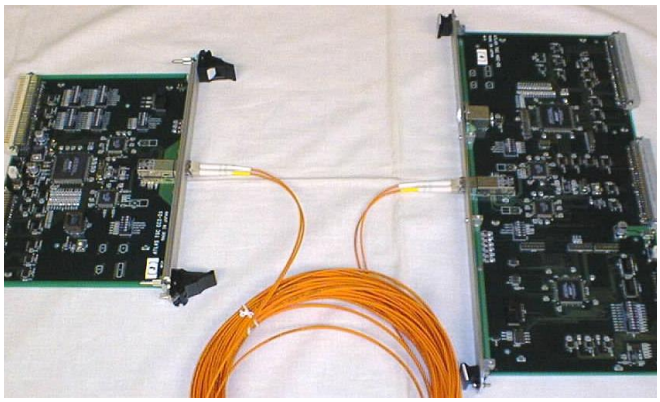

Figure 3: A photograph of the CCI (left) and HSC (right) modules

III Functionality

A *Instruction Set*

Controlling using the HSC and CCI modules is based on an instruction set summarized in Table I. It is defined with G-link words. Each instruction is executed from the local host with a 14-bit control word. On VME access, or interrupt handling, additional two of 16-bit data words are also used. After the action according to the instruction, the HSC module returns a response to the CCI module and the instruction is finished. The instruction and its response are stored into the dedicated registers in the CCI module. The response register has an update bit to indicate whether the register is renewed with the response correspond to the last instruction or not. The local host can check the result and status of the corresponding instruction through the CCI module.

Instruction	Function	Handled by
idle	report HSC status	CCI
setVMEA	set VME Address	SPE
setVMED	set VME Data	SPE
configVME	access VME	SPE
interruptVME	interrupt requests	SPE
enableInterrupt	interrupt handling	SPE
inhibitVME	disable VME access	SPE
resetHSC	reset	PPE
configJTAG	select N-line	PPE
configeTBC	access eTBC	PPE

Table 1: Summary of the instruction set

B *Task Flow*

A main flow in the endcap muon trigger system is discussed. After the initialization with reset instruction, the HPT and SSW modules are configured via VME access. A write access is accomplished by a series of VME-related instructions. During experimental runs, the local host executes a polling task to read back configuration data of the FPGAs periodically via VME read access using returning words. If incorrect bits are detected (probably due to SEUs), the target FPGA is instantly reconfigured with VME write access. The polling frequency can be optimized by considering the SEU rate of the whole endcap muon trigger system. If a VME access is failed and time-out response is reported from the HSC module, the VME controller on the target slave module is probably failed because of SEU. The corresponding CPLD is reconfigured via JTAG bus. If there is no response from the HSC module on VME instructions, the SPE of the HSC module is failed and it is reconfigured with the same manner.

VME interruptions from on-detector slave modules are handled as follows. The HSC module receives an interruption request (IRQ) and status ID from an interrupter, and then sends the interruption information to the CCI module using the dedicated instruction. Receiving the interruption information, the CCI module moves its interrupter to request the local host with its own IRQ level and the status ID succeeded from the HSC module. The interruption handling can be disable in both the HSC and CCI modules independently using instructions.

IV Results of the Performance Tests

A *Setup of the Performance Tests*

Four sets of the HSC and CCI modules have been implemented as prototype versions. Performance tests for them have been done in the setup as shown in Fig.4. The VME bus of the local crate is connected with the PCI bus in an IBM PC/AT compatible PC via a SBS PCI-VME adapter (Bit3) [12]. The host PC runs Linux OS with vmehb [13] as a device driver for the Bit3. The test software is written

in C++ and uses a VME library, vmelib [14].

The optical fibers are connected between CCI and HSC. As the target slave modules, a memory module with 32-bit width registers and a HPT module are used. The former supports A32/A24D32 access and the latter supports A24D16 access.

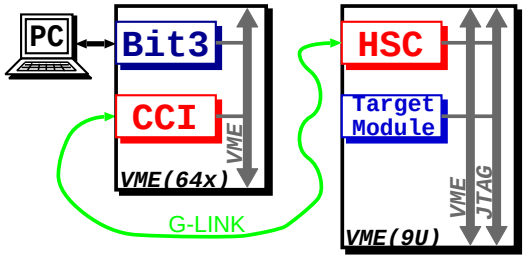

Figure 4: Setup of the performance tests

B Power-on Link

Building links between the HSC and CCI at power-on has been confirmed at first. There are some difficulties to build the G-LINK in the HSC-CCI system because of the slight difference on clock timing between the Tx and Rx chips. Hence both HSC and CCI have functionality to reconfigure the input sampler blocks in the Rx chips until the links are built. Using this functionality, the links between the HSC and CCI are always built at power-on and maintained during operations.

Furthermore we used the 100m-length optical cables, and tested VME and JTAG access as described below.

C VME access

We tested VME access to the slave modules in the remote crate from the local host.

We could access both HPT and memory module without problems, and could read/write data from/to registers. The interrupt function was also tested. We found the system could handle the interrupt process.

The reliability of VME access via CCI/HSC modules have been checked with long-term running test. A memory module was used for the test. 32-bit random data are written continuously in a certain register. It is read back to verify data for each write/read cycle. We have found no errors in 10^{10} continuous read/write cycles.

D JTAG distribution

We also tested JTAG distribution from the local host via CCI/HSC. We used the HPT module as a target module which has a CPLD for VME protocol converter and JTAG port in J3. The figure about JTAG bus in a remote crate is shown in Fig.5.

Each module in the remote crate has a Addressable Scan Ports (ASP) [11] for the gate of JTAG port in the CPLD.

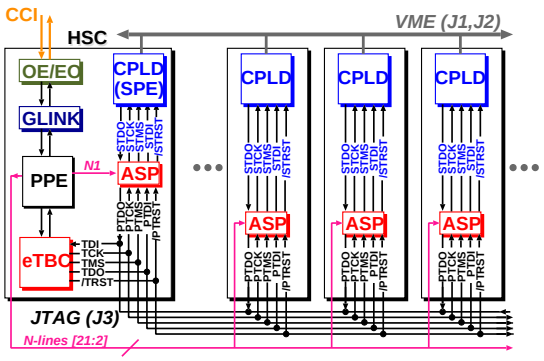

Figure 5: JTAG bus of the J3 backplane in a remote crate

One of the CPLDs is selected using either N-line or special protocol supported by ASP. The CPLD embedded on HPT module is Xilinx XC95288XL [5].

In this test, the eTBC was fully controlled with instructions via CCI/HSC. All the JTAG access to the CPLDs were confirmed and we could verify and reconfigure the configuration data of CPLD using the eTBC and JTAG bus. The software supports SVF data to be configured.

E Measurement of Bandwidth

The response time of the HSC module (T_{RC}) has been measured. T_{RC} is defined as the time between the output of the G-LINK Rx (instruction) and the input of the G-LINK Tx (response) in the HSC module, and is measured with 1ns accuracy. The measured values of T_{RC} are summarized in Table 2.

Instruction	Action at	T_{RC} (nsec) [clk]
idle	PPE	122 [5]
setVMEA	SPE	244 [9]
configVME (read)	SPE+VME	496 [20]
configeTBC	PPE+eTBC	620 [25]

Table 2: Response time of the HSC module

T_{RC} of the SPE is longer than that of the PPE because the PPE has an arbiter and it costs about four clocks for the arbitration of instructions. Additional 11 clocks of "configVME" is due to the VME read cycle. T_{RC} of "configeTBC" includes the response of the eTBC.

Considering the propagation in 90m optical links and G-LINK chips, the bandwidth can be estimated to be 1 MB/sec. In the current design of the SSW module, the total size of FPGA configuration is 18 MB/crate; the total time of FPGA configuration/read-back is estimated to be 18 sec. This estimation allows the CCI/HSC system to perform an excellent watchdog beside the FPGAs with much enough polling frequency and to provide quick reconfigurations for failed FPGAs. In the end-cap muon trigger, the system-wide SEU rate is roughly estimated to

be a couple of upsets every hour, but this rate is acceptable in the remote control system.

V Development for Final Version

In this prototype version, the PPE on the HSC module is implemented with CPLD, but it will be implemented with ASIC in the final version to be tolerant against radiation effects.

In this August, PPE ASIC have been designed and fabricated using 0.35μm full-custom CMOS. The core size is 4.9mm $\times$ 4.9mm; the IC is packaged with PQFP144. The ASIC will be delivered in the end of December.

VI Conclusion

We have developed a remote control system for on-detector VME modules of the ATLAS endcap muon trigger. The introduced HSC (remote controller) and CCI (local interface) modules are connected with G-LINK based optical links and mediates between the local host and the on-detector slave modules. The local host can communicate with the on-detector modules using a instruction set defined with G-LINK words through the CCI/HSC.

The CCI/HSC system can control and configure HPT and SSW modules. In particular, this control system is well adequate for FPGA-embedded modules whose configuration date are susceptible to SEUs. Once a SEU is detected, the target FPGA is instantly reconfigured via the VME bus using byte-based configuration scheme. In case CPLD-base VME controllers on the HSC and slave modules loose their functionalities, these are configurable with JTAG managed by the CCI/HSC.

Prototypes of the HSC module, backplane of the remote crate, and the CCI module have been implemented. These modules have been built using CPLDs and performance tests have been done. We found that read/write access was successful in both the VME and JTAG buses.

The band width of the control system has been estimated on the basis of measurement of HSC access time. The estimated band width is 1 MB/sec. Though the CCI/HSC system has not only the polling task for SEU watch but controls and configuration for on-detector modules, the estimated band width is well adopted for the ATLAS end-cap muon trigger system.

VII Acknowledgements

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The HSC and CCI modules have been implemented from Mitsui Zosen Systems Research Inc. (MSR). Our special thanks are expressed to the staff of MSR for their help and advice.

The PPE ASIC has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo with the collaboration by Rohm Corporation and Toppan Printing Corporation.

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