Optical Link Evaluation for the CSC Muon Trigger at CMS

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Abstract

The CMS Cathode Strip Chamber electronic system consists of on-chamber mounted boards, peripheral electronics in VME 9U crates, and a track finder in the counting room [1]. The Trigger Motherboard (TMB) matches the anode and cathode tags called Local Charged Tracks (LCT) and sends the two best combined LCT's from each chamber to the Muon Port Card (MPC). Each MPC collects data representing muon tags from up to nine TMB's, which corresponds to one sector of the CSC chambers. All TMB's and the MPC are located in the 9U*400 mm VME crates mounted on the periphery of return yoke of the endcap muon system. The MPC selects data representing the three best muons and sends it over optical links to the Sector Processor (SP) residing in the underground counting room. The current electronics layout assumes 60 MPC modules residing in the 60 peripheral crates for both muon endcaps and 12 SP's residing in one 9U VME crate in the counting room.

Due to the high operating frequency of 40.08MHz and the 100 m cable run from the detector to the counting room, an optical link is the only choice for data transmission between these systems. Our goal was to separately prototype this optical link intended for the communication between the MPC and SP using existing commercial components. Our initial design based on the Agilent HDMP-1022/1024 chipset and Methode MDX-19-4-1-T optical transceivers was reported at the 6th Workshop on Electronics for LHC Experiments [2] a year ago. Data transmission of 120 bits representing three muons at 40 MHz would require as many as twelve HDMP chipsets and 12 optical transceivers on a single receiver card. This solution has disadvantages such as relatively large power consumption and component areas on both the transmitter and receiver boards. Studies of the later triggering stages also show that a reduction in the number of bits representing three muons can be made without compromising the system performance. The new list of bits is shown in Table 1.

Table 1: Data delivered from a Muon Port Card to Sector Processor

Signal	Bits per 1 muon	Bits per 3 muons	Description
Valid Pattern Flag	1	3	"1" when data is valid
Half-strip ID [7..0]	8	24	½ strip ID number
Quality [7..0]	8	24	ALCT+CLCT+ bend quality
Wire ID [6..0]	7	21	Wire group ID
Accelerator muon	1	3	Straight wire pattern
CSC ID [3..0]	4	12	Chamber ID in a sector
BXN [1..0]	2	6	2 LSB of BX number
Spare	1	3	
Total	32	96	

Now only three links rather than the six in our previous design are needed for communication between the Muon Port Card and Sector Processor. Another improvement is to serialize and deserialize the data at 80Mhz with a lower power chipset and use small form factor (SFF) optical modules for a more compact design. Test results evaluating the Texas Instruments TLK2501 [3] gigabit transceiver and Finisar FTRJ-8519-1-2.5 [4] optical module as well as the functionality of our evaluation board are presented.

I. Data Serializer and Optical Module

Among several high speed data serializers available on the market, the Texas Instruments TLK2501 [3] is one of the most attractive. It performs both serial-to-parallel and parallel-to-serial data conversion. The transmitter latches 16-bit parallel data at a reference clock rate and internally encodes it using a standard 8B/10B format. The resulting 20-bit word is transmitted differentially at 20 times the reference clock frequency. The receiver section performs the serial-to-parallel conversion on the input data, synchronizes the resulting 20-bit wide parallel word to the extracted reference clock and applies the 8B/10B decoding. The 80MHz to 125MHz frequency range for the reference clock allows us to transfer data at 80.16Mhz which is exactly double the LHC operation frequency of 40.08Mhz.

The TLK2501 transceiver has a built-in 8-bit pseudo-random bit stream (PRBS) generator and some other useful features such as a loss of signal detection circuit and power down mode. The device is powered from +2.5V and consumes less than 325mW. Parallel data, control and status pins are 3.3V compatible. The TLK2501 is available in a 64-pin VQFP package and characterized for operation from –40C to +85C.

A Finisar FTRJ-8519-1-2.5 2x5 pinned SFF transceiver was chosen for the optical transmission. It provides bidirectional communications at data rates up to 2.125Gbps (1.6Gbps simplex mode transmission is required in our case). The laser technology is an 850 nm multimode VCSEL and allows fiber lengths up to 300 m. The transceiver operates at extended voltages (3.15V to 3.60V) and temperature (-10C to +85C) ranges and dissipates less than 750mW. One advantage of the FTRJ-8519-1-2.5 module over similar optical transceivers available from other vendors is a metal enclosure for lower electromagnetic interference.

II. Design Implementation

A simplified block diagram of the evaluation board is shown on Figure 1. It consists of two TLK2501 and Finisar optical transceiver links with control logic based on an Altera EP20K100EQC240 PLD. The PLD provides VME access to the 16-bit transmitter and receiver data busses as well as the control/status signals of both TLK2501 devices. In addition to the VME A24D16 slave interface, it contains: 256-word deep input and output FIFO buffers, two delay buffers, a 16-bit PRBS generator, error checking logic and 2 16-bit error counters. Since the PRBS data is not really a random, but a predetermined sequence of ones and zeroes, the data could also be checked for errors by comparison to an identical, synchronized PRBS generator.

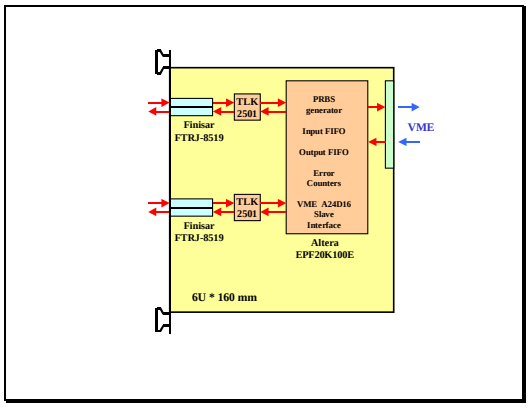

Figure 1: Evaluation Board Block Diagram

There are three modes of board operation. In mode 1, every TLK2501 transmitter can internally generate an 8-bit PRBS and send it to either another TLK2501 receiver or loop it back to its own receiver input. In mode 2, a 16-bit PRBS is generated by the PLD for both TLK2501 transmitters simultaneously. Two variable depth buffers, adjustable from a front panel, are used to delay the PRBS data inside the PLD for comparison with the receiver data. The main control PLD can count the number of errors using two separate (for modes 1 and 2) 8-bit counters which are accessible from VME. Error counting can also be implemented and displayed with an external event counter connected to the Receive_Error output signal.

In mode 3, random programmable data (up to 256 16-bit words) can be loaded into a FIFO buffer from VME and sent out as an 80Mhz burst to both TLK2501 transmitter sections upon a specific VME command. The data from both receivers is then captured into two FIFO input buffers which can be read from VME.

III. PROTOTYPING RESULTS

Two evaluation boards were built and tested in spring 2001. All tests were done in simplex configuration over 100 m optical cable. No PRBS data errors occurred during 3 overnight tests for both PRBS sources (modes 1 and 2).

Another part of our test was evaluation of the latency due to data serialization/deserialization and encoding. The datasheet [3] specifies that the transmit latency is between 34 and 38 bit times, and the receive latency is between 76 and 107 bit times. At 80Mhz these numbers correspond to a link delay (excluding cable delay) of 69 to 91 ns. Our measurements conducted at room temperature and 2.5V power for both TLK2501 devices indicated that the total link latency is between 76 and 82 ns, or more than three bunch crossings. While the exact value is different at each link initialization in increments of the serial bit clock (625 ps), it has never varied by more than the 6 ns total.

The receive and transmit latencies are essentially fixed once the link is established. However, due to silicon process variations and such implementation variables as supply voltage and temperature, the exact delay may also vary slightly. An additional offset of about 2ns was seen when one chip was externally heated to a point uncomfortable to the touch. One TLK2501 was socket mounted for investigation of chip-to-chip variations. No significant difference between 6 chips has been seen.

A receiver reference clock is required on power-up reset, but unlike the Agilent HDMP-1024 receiver it does not need to be of a frequency slightly different from the frame rate. Automatic recovery from loss of synchronization will require periodic transmission of the "Idle" synch character. The resynchronization takes only 2 frames rather than ~2ms required for the Agilent HDMP-1022/1024 chipset.

IV. RADIATION TEST

The goal of the test was to determine how well the TLK2500/TLK2501 serializers and Finisar optical transceivers are able to tolerate the radiation environment and the integrated dose expected at LHC during 10 years of operation. Specifically, the potential for Single Event Latch-ups (SEL) and Single Event Upsets (SEU) in these CMOS devices due to the high flux of secondary neutrons is of concern.

Based on simulations reported in references [5] and [6], the Total Ionizing Dose (TID) for the inner CSC chambers during 10 years of operation is below 10 kRad and the neutron fluence (for E > 100 KeV) is below 10^{12} cm^{-2}. On the periphery of the return yoke (where Muon Port Cards will be located) these numbers are approximately one order in magnitude less. The SEU cross-section is quite independent of the neutron energy above about 100 MeV. While the expected energy distribution at the LHC has a sizable population below this level, we chose a convenient beam energy of 63 MeV to simulate the effect of the neutron environment at the LHC. Since the strong interactions responsible for the energy deposition are independent of the baryon type, our tests were conducted with a 63 MeV proton beam at the Crocker Nuclear Laboratory cyclotron at the University of California, Davis (UCD).

During irradiation the optical evaluation board was positioned perpendicular to the beam which was focused to irradiate only one TLK2500/TLK2501 chip or Finisar optical module at a time. The board was set to transmit PRBS data through 100 m of fiber to a second board located outside the beam area where data transmission errors due to Single Event Upsets were counted. Three serializer chips were exposed up to approximately 270 kRad total dose each, with no permanent damage. No SEL was detected.

At 63 MeV, 1 rad = 7.4×10^6 protons cm^{-2} for silicon. Therefore, assuming strong isospin symmetry for SEU's, 270 Krad is equivalent to 2.1×10^{12} cm^{-2} neutron fluence or well above the expected levels for the peripheral electronics. The two TLK2501 devices produced 12 and 19 data errors due to SEUs while the older TLK 2500 device produced 78. These results are summarized in Table 2. While no errors where observed during the exposure of 2 Finisar optical modules, both devices failed permanently at about 70 kRad, also well above the expected TID. Combining the results for the three chips, no SEL was seen for a fluence of 6.0×10^{12} protons cm^{-2}.

Table 2: Measured SEU Cross Sections for TLK2500/2501 serializers

Device	Proton Fluence (10^{12} cm^{-2})	Dosage (kRad)	Number of SEUs	SEU Xsection (10^{-12} cm^{2})
TLK 2501 #1	1.8	230	12	6.7
TLK 2501 #2	2.1	270	19	9.0
TLK 2500 #1	2.1	260	78	37.1

V. Conclusion

We have built and tested, in a radiation environment, an evaluation board that comprises the two main elements of an optical data link: a TLK2501 gigabit serializer/deserializer and a Finisar FTRJ-8519-1-2.5 optical transceiver. Acceptable data error rates were observed in testing the link at 80MHz using 8/16-bit PRBS test sequences and programmable patterns. We believe the components of the link can be used for the MPC and SP designs at the CSC Trigger System. Our evaluation board itself can be used as a source of test data for the next SP prototype.

VI. References

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