Electronics Commissioning Experience at HERA-B

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Abstract

The readout of HERA-B has been unified to a large extend. Only the HELIX and ASD8 chips with corresponding readout electronics were used and the data acquisition is constructed entirely with Sharc DSPs. This approach minimized the work load and was successful. The feedback of the ASD8 digital outputs to the analog inputs caused oscillations and the efforts to solve this problem still continued in the commissioning phase. The electronics of the sophisticated hardware trigger was commissioned successfully while some problems remain with the self-made 900 Mbit optical data transmission.

I Introduction and Overview

HERA-B is a fixed-target experiment at the HERA storage ring at DESY, Hamburg [1]. Protons interact with thin target wires of different materials. The wires and hence the rate of interactions are steerable. A silicon vertex detector (VDS) is located downstream of the target. A dipole magnet with tracking chambers inside and after the magnetic field follow. Because of the anticipated particle flux and radiation damage the tracking chamber are divided into an inner part with high track density (ITR, micro strip gas chambers with gas electron multiplier foils) and an outer part (OTR, honeycomb drift chambers). Kaon identification is performed with a ring imaging Cherenkov detector (RICH). An electromagnetic calorimeter (ECAL) and a muon detector (MUON) allow for lepton identification. A special set of three layers of tracking chambers (HighPt) are foreseen inside the magnetic field. Their signals allow fast triggering on tracks with large transverse momentum.

Table 1 gives an overview over the applied detector technologies, readout chips, front-end technologies and whether the subdetector is used by the hardware trigger (FLT). With the exception of the ECAL only two readout chips were applied (HELIX and ASD8) and consequently only two versions of front-end electronics had to be developed.

The TDCs for the ASD8 digitization are on the detector while the data of the HELIX chips are digitized in the trailer. The latter is always accessible in a low radiation

area and houses in addition all components of the data acquisition (sect. VII) and of the hardware trigger (sect. VI).

HERA-B was largely assembled by the end of 1999 and commissioning took place in 2000. The goal of measuring CP violation in the neutral B meson system was not reached. The shortcuts due to problems with the electronics and some of the experiences gained during the construction are described in this article. For a detailed description of the electronics components itself the reader is referred to the references.

From September 2000 to July 2001 the accelerator was shut down for a luminosity upgrade for the collider experiments H1 and ZEUS. HERA-B has used this time to solve most of the identified problems.

II VERTEX DETECTOR AND INNER TRACKER

The Vertex Detector (VDS) and the Inner Tracker (ITR) both use the HELIX readout chip [2]. Hence most of the electronics like the digital control signal generation (including their optical transmission to the detector), the analog optical data transmission to the trailer and the digitization of the data is common for both systems. The low voltage power supplies and the technique of programming the HELIX chips differed.

The VDS was fully commissioned by 2000 [3]. For the electronics an important feature of the HELIX was used intensively for monitoring: the analog data is stored internally in a pipeline and upon a trigger the data together with the pipeline location is available at the output. By comparing this location from all chips the synchronization of the VDS can be guaranteed.

In 1998 a first version of the optical transmission for the digital control signals was installed using commercial components. The receivers were located in a low radiation area under the magnet. Particles hitting the receiver's pin diode generated spurious digital signals because of low switching threshold. Consequently within minutes of operation parts of the VDS became asynchronous. The self-made receiver for the analog optical signals in conjunction with a comparator did not show this problem and is used instead.

During the 2000 operation several HELIX chips ceased functioning correctly. The fraction increased with time from about 1% at the beginning to 4% at the end. Most of

 $^{^1\}mathrm{The\ TDC}$ chip could be operated in a binary readout mode for MUON, RICH and HighPt.

subdetector	${ m technology}$	readout chip	$_{ m chn}$	digitization	data transm. to trailer	used by FLT
VDS	silicon microstrip	HELIX	150k	FADC	analog optical	no
ITR	MSGC with GEM	HELIX	130k	FADC	${ m analog\ optical}$	yes
OTR	honeycomb drift	ASD8	120k	TDC	LVDS digital	yes
RICH	Cherenkov + PMT	ASD8	28k	binary(TDC)	LVDS digital	no
MUON	${ m tube, pad, pixel}$	ASD8	30k	binary(TDC)	LVDS digital	yes
HighPt	pad,pixel	ASD8	25k	binary(TDC)	LVDS digital	yes
ECAL	shashlik	$_{\mathrm{PMT}}$	8k	ADC	analog coaxial	yes

Table 1: Characterization of the readout electronics for all subdetectors.

these chips were however not broken. Several procedures were tried to revive them (changing the phase between signals, turning them off/on) with varying success. Because of the redundancy of layers in the VDS these losses did not seriously affect the tracking efficiency. A clear understanding of the problem is not yet reached but recently some problems in the download software were found which explain some observations.

The Inner Tracker [4] was delayed by two years because of radiation hardness problems of the MSGC technology. The 2000 run was thus its first commissioning period. The initial grounding scheme asked for one central point per chamber as a "reference ground" to avoid ground loops. The backside of the MSGC, the PCBs with the HELIX chips and other boards had a ground connection to this point. Further optimization studies showed that a massive direct ground connection between the MSGC and the HE-LIX PCB and using a large surface ground bar with short connections is much more favorable. Especially when the prompt digital trigger outputs of the HELIX (open collector) are activated the new grounding reduces crosstalk of the digital outputs to the analog inputs substantially. Modifications on the HELIX and a reduction of the collector pull-up voltage reduces the crosstalk further.

The low voltage power supplies have a "power factor correction" (PFC) circuit to ensure that the phase between current and voltage is not distorted by the device under load. While these power supplies have been operated in the lab routinely for long time the PFC broke repeatedly during the 2000 operation in the experiment. It is known from other HERA experiments that the 240 Volt power lines have spikes in the experimental halls close to the accelerator. It was therefore advised to add filters and ferrite rings to reduce spikes in the power lines. Whether this cures the PFC failures is not yet known but seems likely.

III THE ASD8 COMMISSIONING

The ASD8 [5] is used by the gaseous detectors (Outer Tracker, Muon detector and HighPt detector) and by the RICH detector (for PMT signal readout). It consists for each of 8 channels of a differential input amplifier, a two-stage shaper, a discriminator with externally pro-

grammable threshold and an open collector differential output stage. The shaping time is below 10 nsec.

Figure 1 shows the OTR on-detector electronic components as an example [6]. The anode wire is at high voltage and connected via a coupling capacitor to one ASD8 input. The second ASD8 differential input is connected to the cathode, i.e. to the ground of the chamber. The connection between the analog ground of the ASD8 board and the chamber ground was found to be very important for noise reduction, especially the Copper-Beryllium springs which hold the board at the chamber make good contact.

Another problematic item is the crosstalk (feedback) between the digital output of the ASD8 and its analog input. The size of this effect depends on the exact configuration and the number of the cables and hence can not be easily estimated in the lab. Operation of the ASD8 at a threshold with large hit efficiency is however impossible without special efforts.

The subdetectors have followed different strategies to reduce the crosstalk. All groups use shielding over the first meters of the twisted-pair cables from the ASD8 to the TDC. In most configurations a good connection of the cable shield to the digital ground of the ASD8 is sufficient while for some HighPt chambers this method is not adequate. Instead the connection is made with a 50 Ω resistor. A possible explanation of this behavior is that the phase of the feedback to the analog ASD8 input is changed by the resistor and thus a constructive interference and oscillations are avoided. In case of the Muon detector [7] large efforts went into the routing of the cables and spacers were added to avoid crosstalk from one cable to the next.

All chambers could be operated in 2000 with hit efficiencies well above 90% but for the Muon pad chambers the above mentioned efforts were not sufficient. Each Muon pad is connected to a preamplifier mounted directly on the chamber. The signal is then driven by a differential ECL line driver via a 3 m twisted-pair cable to the inputs of the ASD8. In the original design the backside of the pad is floating. Connecting this plane to ground reduces the noise substantially but the signal size is deteriorated as well such that the hit efficiencies are limited to around 90%. Since the pad chambers were too noisy (oscillating) without this modification almost all modules were modified in the con-

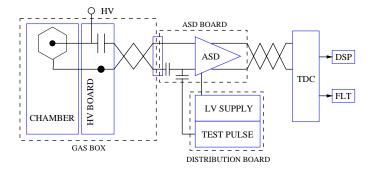


Figure 1: Schematic of the on-detector electronics of the OTR.

struction phase. The unmodified ones as well as some others with poor grounding (about 20% of the channels) were noisy in 2000.

Recently test beam measurements were performed to find a reliable solution. The most promising one is to exchange the preamp and some modules have been modified in Hera-B .

In the 2000 commissioning an additional source of feedback to the analog input of the ASD8 was observed. The TDC board has digital outputs for the connection to the hardware trigger (FLT in figure 1) and when those cables were plugged ASD8 oscillations were observed. In this case the crosstalk could occur via spikes on the TDC ground.² Ferrite rings were added on the cables and the driver strength of the TDC signals was reduced. Test measurements indicate sufficient suppression of the feedback after these modifications.

IV OTR HIGH VOLTAGE CHANNELS LOSS

During the 2000 run about 0.5% of the OTR anode wires developed a "short" and had to be disconnected. This corresponds to a rate of one per 7 hours. Because of the grouping of HV channels about 8

The HERA luminosity shutdown was used to disassemble all chambers and the cause for the shorts were identified: remnants from the soldering of filter capacitors on the backside of the HV board became conductive with time. This problem was not observed in the pre-series production since the soldering technique applied at that time was different. In addition the time constant of this problem is 50000 hours and it would have been difficult to discover the failure with the pre-series boards in any case. By now all 14000 affected capacitors have been replaced and the losses are an order of magnitude smaller.

V ECAL Noise

The signals from the electromagnetic calorimeter are transmitted with (8000) coaxial cables to the ADC boards in the trailer. The calorimeter is floating with respect to its frame in the experimental area and the ground is defined via the connections of the cable shielding. Each signal is terminated at both ends with $50~\Omega$ to avoid reflections.

During last year's running an excess of noise was observed corresponding to a voltage of a few mV at the input of the ADCs. This noise limited the resolution of the ECAL but had litte impact on the pretrigger performance. The origin of the noise was traced back to different ground levels of the readout crates in the trailer and hence different ground levels along a coaxial cable. Via the 50 Ω termination on the PMT side any ground bounce will couple to the signal line and hence create noise. All terminators were exchanged on the PMT side by 10 k Ω resistors and first measurements indicate a sufficient suppression of the noise.

VI THE HARDWARE TRIGGER

The main thrust of Hera-B was to find CP violation in the decay channel $B^o \to J/\Psi \, K_S$. Since the anticipated rate of 5 proton interactions every 96 nsec is large, a sophisticated hardware trigger (First Level Trigger) [8, 9] was designed to reduce the event rate to 50 kHz, a level which can be handled by the data acquisition and a PC farm for further processing.

The basic idea is to detect both electrons or both muons from the J/Ψ decay, calculate their momenta and the invariant mass. The search starts with a pre-trigger for electrons (looking for ECAL towers above threshold) and for muons (calculating coincidences in the pad chambers of the last two superlayers).

The "work horse" of the trigger is the track finding unit (TFU). There are 72 TFUs in the entire system, typically 10 per superlayer of the tracking chambers. The TFUs of one layer receive the hit information of the corresponding chambers for every bunch crossing. In addition they receive messages from the TFUs of the previous layer and transmit messages to the TFU of the next layer. A message contains the current parameters of track candidates and their uncertainties. From the incoming message the TFU calculates a region-of-interest where the track should have passed through the superlayer and use the information from the chamber to search for confirmation hits in three stereo views.³ If found the track parameters will be updated and a new message will be sent to the next TFU layers. If no confirmation hit is found (in one or more stereo views) no output message will be generated.

²The pull-up resistors for the open collector outputs of the ASD8 are located on the TDC board with a pull-up voltage of 1.25 Volt. The 2 mA current per channel flows through one of the wires of the twisted-pair cable to the ASD8 and back via the ground connection of the power supplies to the TDC. Obviously any disturbance on the ground level and/or pull-up voltage will couple to the ASD8. A LVDS driver on the ASD8 board would have been a more robust solution but impossible to implement at the time the problem was discovered.

 $^{^3\,\}mathrm{There}$ are two layers of tracking chambers per stereo view and the OR is used in the trigger.

The search direction is opposite to the particle direction and starts with the pre-triggers at the downstream end of the detector. It ends at the chamber closest to the magnet. At this point the track parameters are well determined and the momentum can be calculated (with a track parameter unit) assuming that the track comes from the target. For two tracks the invariant mass can be determined (with the trigger decision unit). The trigger hence consists only of 3 different types of boards and the total processing time including the pre-triggers is less than 10 μ sec. Its data input is 1 Tbit/sec from the tracking chambers and at design rate about 500 million track candidates per second are followed through the hardware. The rate reduction should be at least 200. Hence the 10 MHz bunch crossing frequency is reduced to a trigger rate of 50 kHz.

The TFU is the most complicated board of Hera-B (23000 solder pads). The hardware and firmware is designed such that software tests allow rigorous debugging of the entire board and the detailed identification of problems like bad solder points. These boards were tested for one week before they arrived at DESY and showed no problems.

The large amount of data transmitted from the tracking chambers to the trigger (1 Tbit/sec) is realized with about 1500 self-made 900 Mbit optical links [10]. At the time of the design there was no commercially available solution at this speed available. Our design uses the Autobahn spanceiver from Motorola to serialize a 20 MHz 32-bit wide input. The serial (differential PECL) Autobahn output is transmitted with a VCSEL from the experiment to the trailer. The optical receiver converts the light back into a serial (differential PECL) signal and a second Autobahn recovers the parallel data.

The requirement of the hardware trigger is that close to 100% of these data links have to work perfectly since a single missing hit causes inefficiencies of the trigger. Unfortunately about 5% of the links were periodically unstable, i.e. had a large bit error rate. Inefficiencies were nevertheless avoided since the TFU hardware could artificially set all hits to "1" for the identified links. The most relevant data link problems were due to instabilities of the VC-SEL (changes of the light output and poor eye pattern), mechanical problems with the ST-connectors and the fact that the duty cycle of the serial bit stream varies which reduces the stability of the transmission line.

Recently remotely programmable DACs have been added to adjust the amplitude and offset of the VCSELs. Thus some of the problems should be solved. However the data transmission remains a worry for the next data taking.

The muon pre-trigger [11] finds track seeds by calculating coincidences of the pad (and pixel) chambers signals of the last two superlayers. Since several pad modules were unstable and individual channels became noisy for some time during the operation, those channels contributed largely to the coincidence rate and had to be masked. The identification was relatively easy because of a build-in feature of the hardware: a small fraction of the coincidence messages were not only sent to the hardware trigger but also written to a VME accessible register. The online software was hence able to locate those channels quickly and mask them online without stopping the data acquisition.

The online masking is an involved task since the updated mask has to be stored in a database and the information of the new version has to be distributed to all PCs of the Second Level Trigger farm. In total the online software consists of about 20 different processes running on 10 different computers. About 10 man years have been invested in the software (including offline monitoring) which almost equals the effort for building the hardware (15 man years).

For the ECAL pre-trigger [12] online masking was also needed. Here the origin was a different one: the quality of the commercially produced boards was very poor which caused long delays and for the installed boards bit errors in the cluster energy. Hence local hot towers were observed and had to be masked.

VII THE DATA ACQUISITION

While the hardware trigger is processing hits of a given bunch crossing the detector front-end keeps the full data in a pipeline. When a trigger is issued the digitized event is stored in the Second Level Buffers (SLB) with a depth of 270 events. The maximum event input rate is 50 kHz. The Second Level Trigger (a farm of 240 PCs) then accesses the event data via the Switch from the SLBs and performs a partial event reconstruction based on the tracks found by the hardware trigger [13]. Another process (called Event Controller) keeps track of the free buffers on the SLB and the idle PCs.

The Event Controller, the SLBs and the Switch are realized with Sharc DSPs from Analog Devices. Each Sharc has six 40 MB/sec input ports, a 32-bit bus for Sharc-to-Sharc connections, a 40 MHz CPU and 4 Mbit dualported memory. For HERA-B a custom made VME board with 6 DSPs was developed of which about 200 are in use. The board worked reliably.

The challenge is to guarantee that no message from the Second Level Trigger to the SLBs and back is lost, i.e. to back pressure messages and not to loose any interrupt on a Sharc. For speed consideration Assembler was used for the Switch programming while the language C was used elsewhere [14].

The advantage of the unified hardware approach for the data acquisition is the easy connectivity in the entire experiment and the minimal amount of man power needed for development (6 man years) and maintenance.

⁴The duty cycle is almost identical to the occupancy since the Autobahn simply serializes the input data stream.

The maximum bandwidth of the Switch is 1 GB/sec and the limit on message rate is 2.6 MHz. This is according the specifications and the same is true for the SLBs and the Event Controller.

VIII SUMMARY

HERA-B was largely completed at the end of 1999. The electronic commissioning in 2000 revealed some surprises (like the feedback from the TDC-FLT connection to the ASD8). Prior to the installation and during the commissioning oscillation problems of the ASD8 readout chip caused problems and delays. Perfect grounding could reduce the noise in most cases to an acceptable level. For the Muon pad system this could only be accomplished by grounding the backside of the pads which let a smaller hit efficiency. During the HERA shutdown most of these problems could be fixed or reduced and for the next data taking period a large improvement is expected.

The electronic of the hardware trigger was working reliably, especially the TFUs. The only exception is the optical data transmission from the tracking chambers to the trigger which remains problematic for future running.

The data acquisition and the front-end electronics (FADC boards for the HELIX digitization and the TDC boards for ASD8 digitization) were largely unified in the experiment and worked successfully.

The example of the trigger shows that the hardware design has to support debugging and online monitoring. High quality software tools are needed for commissioning and the amount of man years equals the time used to build the hardware.

Let me conclude with two personal recommendations. The experience shows that many small design mistakes can have a large impact on the quality of the experiment. To find them regular reviews by experts from other experiments would help. Although this is a big effort the knowledge about problems and solutions would spread fast within the HEP community. One example is the usage of open collector outputs. They should be avoided and be replaced by LVDS signals.

REFERENCES

- [1] E.Hartouni et al., HERA-B Design Report, DESY-PRC 95/01, (1995).
- [2] W. Fallot-Burghardt et al., *HELIX128S-2 Users Manual*, HD-ASIC-33-0697, http://www.asic.kip.uni-heidelberg.de/feuersta/projects/Helix/index.html.
- [3] C.Bauer et al., Status of the Hera-B Vertex Detector, Nucl. Instr. Meth. A447 (2000) 61.
- [4] W.Gradl, Nucl. Instr. Meth. A461 (2001) 80-81;
 T.Hott, Nucl. Instr. Meth. A408 (1998) 258-265.

- [5] M.Newcommer et al., IEEE Trans. Nucl. Sci. NS-40 (1990) 690.
- [6] K.Berkhan et al., Large System Experience with the ASD8 Chip in the HERA-B Experiment, Proceedings of the 5th Workshop on Electronics for LHC, Snwomass 1999.
- [7] V.Eiges et al., The Muon Detector at the HERA-B Experiment, Nucl. Instr. Meth. A461 (2001) 104-106.
- [8] T.Fuljahn et al., Concept of the First Level Trigger for HERA-B, IEEE Trans. Nucl. Sci. NS-45 (1998) 1782-1786.
- [9] M.Bruinsma, D.Ressing at al., these proceedings.
- [10] J.Gläß et al., Terabit per Second Data Transfer for the HERA-B First Level Trigger, Proceedings of IEEEE Conference on Realtime Systems, pp 38/42, Valencia, Spain, June 2001.
- [11] M.Böcker et al., The Muon Pretrigger System of the HERA-B Experiment, IEEE Trans. Nucl. Sci. NS-48 (2001) TNS-00118-2000.
- [12] C.Baldanza et al., The HERA-B Electron Pre-Trigger System, Nucl. Instr. Meth. A409 (1998) 643.
- [13] J.M.Hernandez et al., HERA-B Data Acquisition System, Proceedings of IEEEE NSS-MIC conference, Lyon, France, November 2000.
- [14] HERA-B Collaboration, Digital Signal Processor Software for the HERA-B Second Level Trigger, Proceedings of the Conference on Computing in High Energy Physics, Chicago, August 1998, http://www.hep.net/chep98/PDF/109.pdf.